THREE PHASE STATE ESTIMATION TECHNIQUES FOR NETWORK VOLTAGE UNBALANCE ASSESSMENT

Shambavi Manmatharajan (EE-149291A)

Dissertation submitted in partial fulfilment of the requirements for the Degree Master of Science in Electrical Engineering

Department of Electrical Engineering

University of Moratuwa Sri Lanka

June 2018

DECLARATION OF THE CANDIDATE & SUPERVISOR

I declare that this is my own work and this dissertation does not incorporate without acknowledgement any material previously submitted for a Degree or Diploma in any other University or institute of higher learning and to the best of my knowledge and belief it does not contain any material previously published or written by another person except where the acknowledgement is made in the text.

Also, I hereby grant to University of Moratuwa the non-exclusive right to reproduce and distribute my dissertation, in whole or in part in print, electronic or other medium. I retain the right to use this content in whole or part in future works (such as articles or books).

Signature:

Date:

The above candidate has carried out research for the Masters Dissertation under our supervision.

Signature of the supervisor: Date

Signature of the supervisor: Date

DEDICATION

To my parents for earning an honest living and for supporting and encouraging me to believe in myself. I dedicate this thesis to my family for nursing me with affections and love and their dedicated partnership for success in my life.

ACKNOWLEDGEMENTS

Firstly, I would like to express my sincere gratitude to my supervisor Dr Upuli Jayatunga for the continuous support for my Msc study and related research, for her patience, motivation, and immense knowledge. Her guidance helped me during the period of research and writing of this thesis. I could not have imagined having a better advisor and mentor for my research.

Besides my advisor, I would like to thank progress review panel and, for their insightful comments and encouragement, but also for the hard questions which incented me to widen my research from various perspectives.

Lastly, I should thank many individuals, friends and colleagues who have not been mentioned here personally in making this educational process a success.

ABSTRACT

Voltage unbalance is an important aspect of power quality. Unbalance can damage power equipment in a power system network, affect the operation of sensitive customer equipment and increase losses. Conventional Power system state estimation (PSSE) which assumes the network to be fully balanced does not capture the information related network voltage unbalance. Although, the single line representation of the network is good enough for most of the cases when it comes to transmission level, there can be certain locations in the power system, especially in the distribution network, which are prone to high voltage unbalance (VU) levels over which network operators wish to have full three-phase details in real time. To address this issue, completely switching into three phase model of the network which will add a significant computational burden, is not a feasible solution at all.

As a feasible remedy, this thesis introduces a novel methodology for voltage unbalance state estimation extending the conventional state estimation which can be selectively applied only for the locations of interest to capture the information related to network voltage unbalance, with minimum additional computational effort. The proposed three phase estate estimation make use of Singular Value Decomposition method to work out the estimation of three phase voltages and hence the complex voltage unbalance factor (VUF) at the locations of interest.

Proposed methodology is verified using IEEE 4 bus and 14 bus test networks simulating them using a three phase unbalanced power flow program written in MATLAB environment.

TABLE OF CONTENTS

DECLARATION OF THE CANDIDATE & SUPERVISOR I						
DEDICATIONII						
ACKNOWLEDGEMENTSII						
A	ABSTRACTIV					
	TABLE OF CONTENTS					
L	IST O	F FIGURES				
		F TABLES				
L	IST O	F ABBREVIATIONS	VII			
1	IN	TRODUCTION	1			
	1.1	MOTIVATION OF THESIS	1			
	1.2	THE AIM OF THIS PROJECT	2			
	1.3	APPROACHES AND METHODOLOGY	3			
	1.4	THESIS OUTLINE	4			
2	LĽ	FERATURE REVIEW	5			
	2.1	GENERAL OVERVIEW OF VOLTAGE UNBALANCE (VU)	5			
	2.2	QUANTIFICATION OF VOLTAGE UNBALANCE				
	2.3	SOURCES OF VOLTAGE UNBALANCE AND EFFECTS				
	2.4	MITIGATION OF VOLTAGE UNBALANCE	10			
	2.5	VOLTAGE UNBALANCE EMISSION ASSESMENT	11			
	2.6	POWER QUALITY STATE ESTIMATION	13			
	2.7	WEIGHTED LEAST SQUARES METHOD (WLS)	14			
	2.8	SINGULAR VALUE DECOMPOSITION	16			
	2.9	OBSERVABILITY ANALYSIS				
	2.10	HISTORY OF POWER SYSTEMS STATE ESTIMATION				
	2.11	DISTRIBUTION SYSTEM STATE ESTIMATION (DSSE)	20			
3	TH	IEORETICAL FORMULATIONS OF THE VOLTAGE UNB	ALANCE			
S	ТАТЕ	ESTIMATION	21			
4	AP	PLICATION OF PROPOSED FORMULATION FOR STAN	DARD			
Т		YSTEM				
	4.1	IEEE 4 BUS SYSTEM				
	4.2	IEEE 14 BUS SYSTEM ANALYSIS				
	4.3	System Observability Analysis				
5	CC	ONCLUSIONS AND RECOMMANDATIONS				

	5.1	Conclusions	
	5.2	RECOMMANDATIONS	
6	REI	FERENCES	
7	API	PENDIX 1	41
8	API	PENDIX 2	42
9	API	PENDIX 3	43

LIST OF FIGURES

Page

Figure 2.1 Examples of balanced and unbalanced three-phase voltages	5
Figure 2.2 Sequence Component Torques of Induction Machine	9
Figure 2.3 Network with pre-existing unbalance and unbalance level at the point of	
evaluation1	12
Figure 2.4 Unbalance level and unbalance emission at the POE 1	3
Figure 2.5 State Estimation Techniques and estimated quantities 1	8
Figure 3.1: Three-Bus Interconnected Network2	21
Figure 3.2 General algorithm of SVD state Estimation	24
Figure 4.1 IEEE 4 bus test system 2	26
Figure 4.2 Estimated Voltages	27
Figure 4.3 Estimated Voltage Error 2	27
Figure 4.4 IEEE 14 standard bus system2	28
Figure 4.5 Estimated Voltage at busbar 2	29
Figure 4.6 Estimated Phase A voltage in Case 1,33	60
Figure 4.7 Estimated Phase B voltage in Case 1,33	0
Figure 4.8 Estimated Phase C voltage in Case 1,3 3	1
Figure 4.9 Magnitudes and angles of VU factors at different bus bars	2
Figure 4.10: Error between the VUF calculated through Load Flow and Estimation	
Methodology	32

LIST OF TABLES

Page

Table 4. 1:Transformer Details	27
Table 4.2: Estimated Voltages &Load flow Output	28
Table 4.3: Measurement placement & Performance of SVD	30
Table 4.4: Estimated Voltages in all six cases	34
Table 4.5 Busbars and node numbers	34

LIST OF ABBREVIATIONS

Abbreviation	Description
VU	Voltage Unbalance
SE	State Estimation
SVD	Singular value decomposition
DSSE	Distribution System State Estimation
VUSE	Voltage Unbalance State Estimation