CMOS LEAKAGE POWER REDUCTION AND DATA RETENTION

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Degree of Master of Science in Electronics and Automation

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The Above Candidate has carried out research for the masters thesis under my supervision.

Name of the supervisor: Dr. S. Thayaparan

Signature of the supervisor: Date:

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Abstract

As silicon technology scaling, leakage power dissipation has become the most significant component from all CMOS power dissipation mechanisms. Minimum Leakage Vector(MLV) is used as a combinational logic leakage power reduction technique when a system is in standby mode. Compared to MLV, though an excellent leakage power reduction can be achieved with power gating technique it has some drawbacks like higher retention time and system state loss.

In this thesis we combine MLV and power gating techniques to achieve more leakage power reduction compared to MLV while mitigating prior mentioned drawbacks of power gating.

Instead of full chip power gating, we developed a simple algorithm which runs in linear time to identify the prospective locations for power gating once combination logic is fed with its MLV. The algorithm was implemented in tcl language and run on top of design compiler shell for a synthesized netlist.

Flip flops and input ports were modified to feed MLV in standby mode while facilitating for partial power gating within the flops without losing flop state to retain the system state back in active mode.

Flop modifications were extended to feed MLV in scan mode also so that scan mode leakage reduction can also be achieved while successful scan shifting carrying out.

Our implementations were tested with four selected ISCAS89 benchmarks using fast spice simulations with synopsys XA. We were able to achieve 30%-40% additional leakage power reduction compared to standalone MLV. The measured wake up time was always less than 0.25ns for all benchmarks while with standalone power gating this is more than a nano second or couple of nano seconds . Successful operation in scan mode and state retention of flops after standby mode were also verified. Rough estimate in area increment due to newly added infrastructure was also carried out.