DEVELOPMENT PLATFORM FOR MOTOR CONTROLS

A dissertation submitted to the
Department of Electrical Engineering, University ofMoratuwa
in partial fulfillment of the requirements for the
degree of Master of Science in Industrial Automation

by

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Abstract

By P. R. D. Dayananda
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Department of Electrical Engineering

Speed control of induction motor has become a famous topic in the industrial automation field during the past decade. Due to the rapid growth in power electronics, this field has been grown for a great extent. There are many algorithms currently available for speed control of induction motors, while every algorithm has its relative merits over other. In different situations, it's desirable to use different algorithms. In normal inverters available in the market, most of the time one algorithm is implemented, which is hard-coded in the circuit. This project is about design of a programmable induction motor drive which is capable of implementing different algorithms in one system. Currently it has been developed as a test bench for machines laboratory where different algorithms such as Six Step, Sinusoidal PWM and Constant VIf control are available in the same system with user selectable mode. The system is reprogrammable, so it's possible to include some new algorithms such as trapezoidal PWM in future as further development of this project.

Two types of microcontrollers are used in order to produce the control signals for the inverter. One is Object Oriented PIC (OOPic) and other is PIC16F767, in which there are 3 inbuilt hardware PWM modules with 10-bit resolution available. Six step algorithm is implemented using the OOPic & the sinusoidal PWM with *Vlf* control in implemented using PIC16F767. There is a new speed sensor designed using Hall IC which is very cheap & accurate in operation. This is designed as a low cost alternate method of speed sensing instead of 'Using high cost encoder or photo electric sensors. The sensor feedback signal processing & display of speed also implemented in OOPic.

A driver circuit was very much needed in between the controller and the inverter for several reasons. One is to provide optical isolation from logical ground and the power ground. Other one is to provide a sufficient dead time in upper & lower switch signals. Also a voltage which is capable of switching on an IGBT was needed from the driver circuit. An IGBT module-which consists of converter & inverter circuit is used as the main switching device to produce variable frequency, variable voltage sinusoidal output.

Many challenges were faced while carrying on the project, which gave us a valuable experience by having hands on experience with different ICs, power electronic devices & microcontroller programming. The major issues and challenges faced and the solutions are included in this report. Also a detailed discussion about various components & functionalities is included with the test results. This project report will be a very useful document to anybody interested in designing control systems and power electronic circuit design.

DECLARATION

The work submitted in this dissertation is the result of my own investigation, except where otherwise stated. It has not already been accepted for any degree, and is also not being concurrently submitted for any other degree.

UOM Verified Signature

P. R. D. Dayananda

I endorse the declaration by the candidate.

UOM Verified Signature 07/09/09

Dr. Sisil Kumarawadu

CONTENTS

ACKNOWLEDGMENTS

This project is an academic requirement of the M.Sc. We wanted to do a project that relates with Automation. My project is "***Development Platform for Motor Controls***" and the project supervisor is Dr. Sisil Kumarawadu. My sincere thanks go to my Project supervisor Dr. Sisil Kumarawadu for allowing us do this project and guiding us.

Many challenges were faced while designing the power electronic circuits and the controllers. Finding solutions to the many issues, which were encountered, really built a strong link between the power electronics and Electrical drives principles, which we learnt especially in throughout the course.

Next we thank Dr. J. P. Karunadasa, the head of the Electrical Engineering Department and other staff members of the Department for imparting us the knowledge required to do this project and their comments and suggestions during presentations were also very useful.

We have the pleasure of thanking all the non-academic staff members in the department laboratories and administration division who honestly supported me.

Again we take this an opportunity to thank everyone whose names were not mentioned, for all the support given in many ways to accomplish this project successfully.

LIST OF FIGURES

1. Introduction

1.1 Background and Motivation

Smooth speed control of an Induction motor had been a major problem in the early industry, difficulty in controlling speed has led the industry to go for other options like DC motors. However, with development of microcontrollers and power electronic devices there is a tendency to go for power electronic Invertors recently. But available inverters are expensive, consist of more hardware and things are hard coded. Still, such available speed controllers do not provide the customer flexibility to select a desired control algorithm. This project, "Development Platform for Motor Controls" is developed as a test bench which can be used in the machines lab for Electrical Engineering students.

This project is developed as a system where different types of motor controlling algorithms are available and the system can be upgraded for some new algorithms in future. This introduces a method for flexible motor speed controlling in the industry and works as a low cost variable speed drive as well.

1.2 Importance of the project

In this project, a new controller OOPic is used to produce the some control signals. By using different types of microcontrollers in the market, this project has been developed as a test bench where students will be able to get a practical experience how the smooth control of electrical drives can be achieved by combining Software, Electronic and Electrical engineering concepts. Further, they can visualize waveforms of control signals generated by the microcontroller using the oscilloscope, and how they vary when the speed changes, what are the inherited features of this control techniques both pros and cons, and how these control techniques physically affect the motor's performance. The test bench is visual layout to observe how different types of components are collaborated with each other to accomplish the overall task. And further, it can be used there to verify how the PWM signals are generated, the dead band time clarification by watching the control signals in the oscilloscope.

1.3 Organization of the report

- First chapter is a brief introduction to the project and it includes the background, motivation for the work, importance or the requirement of such development and the objectives of the project design.

- Second chapter presents project overview and it contains project life cycle, time line, requirement analysis, component ratings and a block diagram of the final design.

- Third chapter describes the project implementation and it is divided into the main areas of the project such as control circuit, driver circuit, sensor design & interface design. It covers the implementation method, the problems faced during implementation & the solutions taken.

- Fourth chapter contains the final system details. It contains the final system's panel image, Circuit fitting image & sensor mounting images. It also contains the cost analysis of the project.

- Fifth chapter is the conclusion, which discusses about the results, the conclusions taken from that & the things that could not have been implemented due to several reasons such as time constraint. Also the future improvement of the system discussed.

- The programming codes, circuit diagrams drawn in Orcad are included in the annexure.

1.4 Objectives

The industrial automation is a new field which is improving very rapidly everyday. The advent of new advance power electronic technologies is helping to lower the energy consumption largely. When considering about energy savings in the automation industry, variable speed drives play a big role. As the production rate heightens, the number of processing machines increases and is subject to high consumption of energy. Hence with this high energy consumption and high electricity cost, it is required to take necessary measures to reduce the energy consumption, improve energy efficiencies. Induction motors are identified as a high potential target for energy consumption in the industry. In many cases the speeds supplied by the motor are not inline with the requirements. Due to this reason, the variable speed drive systems are now replacing the older gear systems. Water pumps, blowers, conveyor motors, electric lifts etc are just a few places where three phase variable speed drives are used today. Nevertheless, the issue is that the conversion cost for this is somewhat expensive, therefore not allowing small industries to go for that option regardless it is critical to survive in today's competitive environment.

So we identified this problem and designed a programmable induction motor drive as a test bench. The objective of this project is defined as follows:

- ***Generating different types of control signals in one system***

  Since this is designed as a test bench, the main objective was to implement different types of motor controlling algorithms in one system which can be upgraded for some new algorithms in future.

- ***Cost optimization***

  Currently available products in the market are having a price which is not affordable by everyone. So we decided to make the system with less cost, but with all functionalities expected as a variable speed drive.

- ***Provide protection mechanisms for the motor & controller***

  This is another feature expected in the industry to be implemented in the motor drives. Over voltage protection, line to line voltage protection, over current protection & optical isolation are the main mechanisms that were decided to implement in the system.

- ***Design of a speed sensor which is low in cost with required accuracy***

  Currently available speed sensing mechanisms like optical encoders are very much accurate and very much expensive as well. So we have decided to design a speed sensor with required accuracy. We decided to use a Hall IC for this purpose as this has high accuracy, lower cost & small in size.

1.5 Background Study

1.5.1 V/F control Mechanism

The V/F control is the salient control mechanism for the induction motor speed control. The ***base speed*** of the induction motor is directly proportional to the supply frequency and inversely proportional to the number of poles in the motor. Since the number of poles is fixed by design, the best way to vary the speed of the induction motor is by varying the supply frequency. The torque developed by the induction motor is directly proportional to the ratio of the applied voltage and the frequency of supply. By varying the voltage and the frequency, but keeping their ratio constant, the torque developed can be kept constant throughout the speed range. This is exactly what V/F control tries to achieve.

The typical torque-speed characteristic of the induction motor, supplied directly from the main supply is shown below.

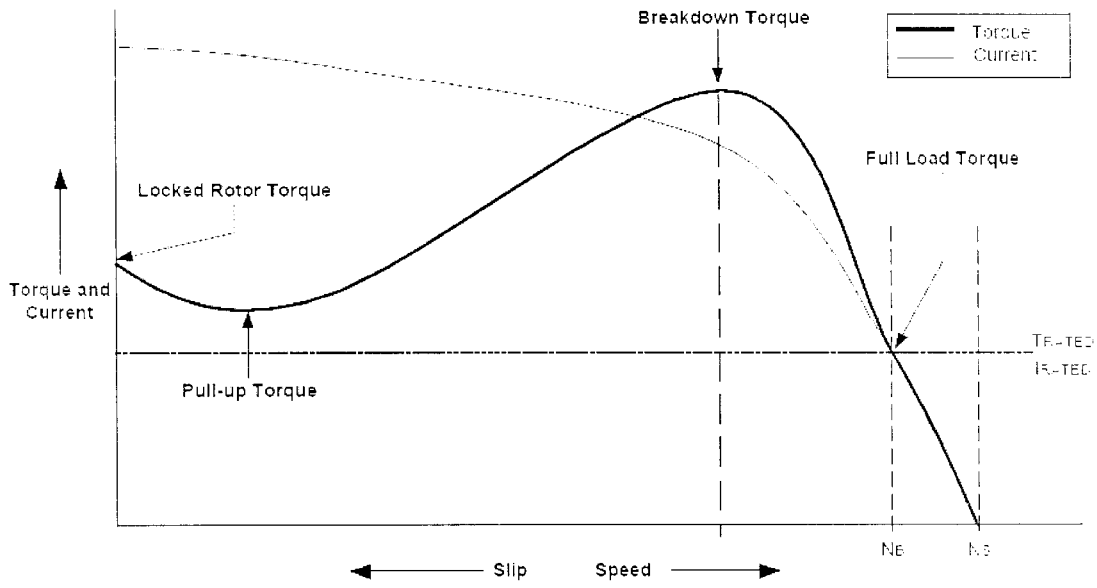


Figure 1.01: Torque Speed characteristics

The main features in the V/F control mechanism.

- The starting current requirement is lower.
- The stable operating region of the motor is increased. Instead of simply running at its base rated speed, the motor can be run typically from 5% of the synchronous speed up to the base speed. The torque generated by the motor can be kept constant throughout this region.
- At base speed, the voltage and frequency reach the rated values. As shown in the *figure 1.02*, the motor can be run beyond the base speed by increasing the frequency only, without changing the applied voltage beyond the rated voltage. This results in the reduction of torque.

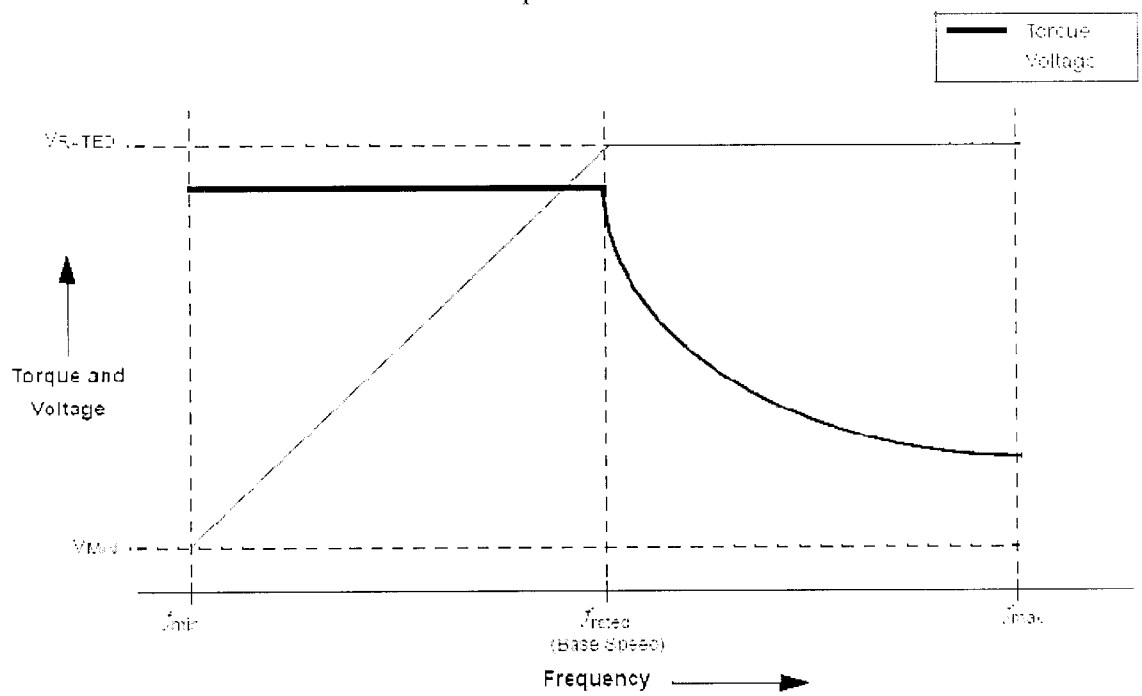


Figure 1.02: V/f characteristics

1.5.2 Six Step and Sinusoidal PWM Generation

The six switches (IGBTs) of the inverter are switched in six steps such that a resultant sinusoidal waveform is applied across the motor windings. For this purpose, the total period is divided into six equal periods, in each period two one sided switches & one other side switch will be ON.

The six step algorithm is easy to implement compared to sinusoidal one, but has some disadvantages. The main disadvantage of six step algorithm is that it can be used to change the output frequency only. Output amplitude can be controlled by only changing the DC-link voltage. But in six step, harmonics of order three and multiples of three are absent from the line to line and voltage. In order to control the output voltage, PWM technique can be used. The sinusoidal PWM generation is done by comparing a saw tooth waveform of high frequency with sinusoidal control signal with desired frequency. But here the magnitude and the frequency of the output signal can be changed by changing the magnitude and the frequency of the sinusoidal wave form.

2. Overview of the project

2.1 Project Life Cycle

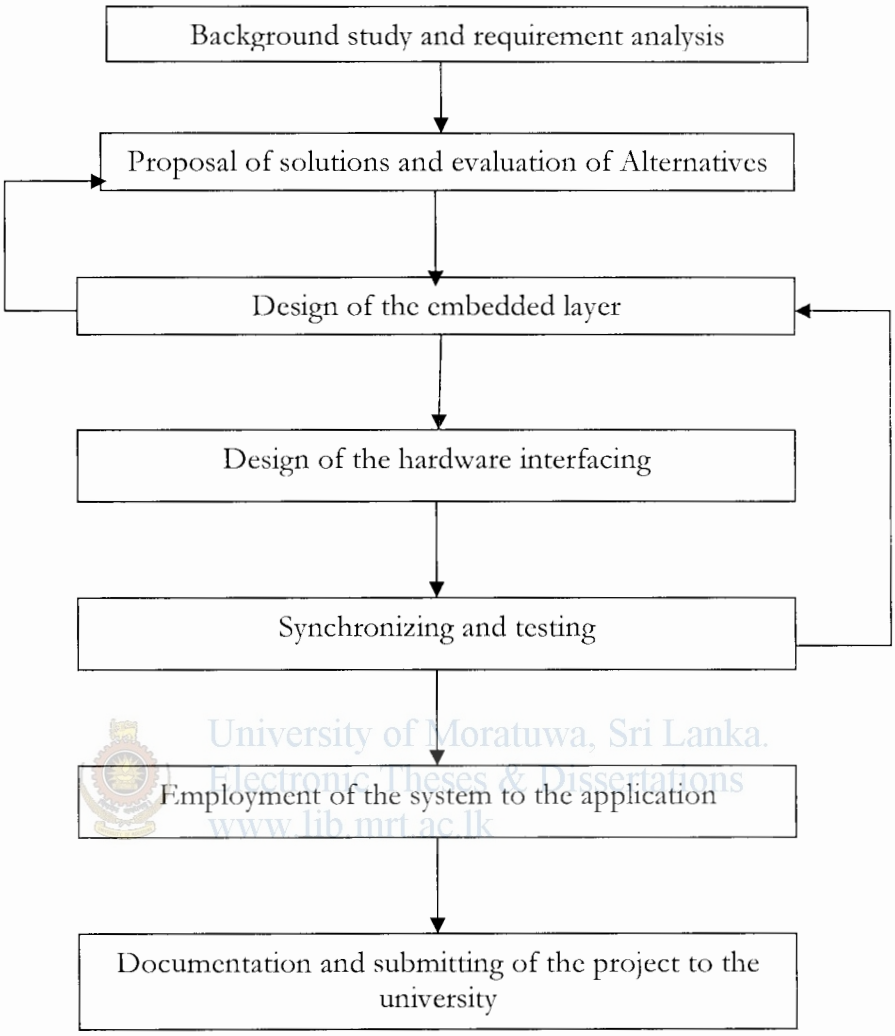


Figure 2.01: Project Life cycle

2.2 Project timeline

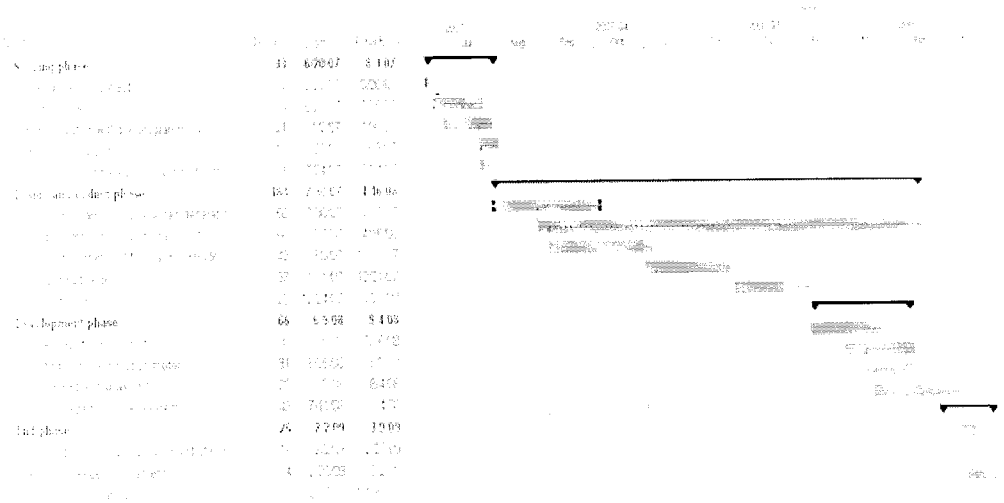


Figure 2.02: Project Time line

2.3 Design Requirements

Parameters of the application for which the drive design is based on are as follows.

$V_{rated} = 240\,V$ Motor is in delta connection

Power = 370 W

Power factor = 0.76

Rated speed=1360 rpm

Rated frequency=50 Hz

2.4 Calculations

According to the parameters of the selected motor for which requires drive design, the required DC bus voltage, hence required transformer capacity, and voltage are calculated.

With 5% of allowable over voltage margin of rated voltage 240V, the maximum required rms voltage is set to 252V.

$$V_{max,rms} = 240 \times 105\%$$

$$= 252V$$

- For Sinusoidal PWM Signals

Thereby maximum peak voltage required was derived.

$$V_{max,pk} = V_{max,rms} \times \frac{\sqrt{2}}{\sqrt{3}} = 252 \times \frac{\sqrt{2}}{\sqrt{3}} = 206.76V$$

Assuming a maximum of 0.9 amplitude modulation ratio, the maximum DC bus voltage was derived

$$V_{dc} = \frac{V_{max,pk} \times 2}{m_a} = \frac{205.76 \times 2}{0.9} = 457.24V (\approx 460V)$$

- For the Six-step PWM Signals
  Thereby, the maximum DC bus voltage was derived

$$V_{dc} = \frac{V_{mx,rms} \times \sqrt{3}}{\sqrt{2}} = \frac{252 \times \sqrt{3}}{\sqrt{2}} = 308.64V(310V)$$

2.4.1. Required Variac Calculation

A three phase rectifier included in this rectification which is encapsulated in IGBT Module. So, to get the required output dc voltage from the three phase rectifier a variac is used before the converter to reduce the supply voltage.

$$V_{LL,\ variac\ Output} = \frac{V_{dc,\ rectifier}}{1.35}$$

For sinusoidal PWM

$$V_{LL,\ variac\ Output} = \frac{460}{1.35} = 341V$$

Variac tapping position$= \frac{341}{400} = 85.25\%$

For six-step PWM

$$V_{LL,variac\ Output} = \frac{310}{1.35} = 230V$$

Variac tapping position$= \frac{230}{400} = 57.5\%$

The rated current of the motor is calculated from the other name plate parameters of the motor.

$$I_{rated} = \frac{370}{\sqrt{3} \times 240 \times 0.76} = 1.17A$$

Taking the starting current of about 6~9 times the rated current
I starting, max =7.03A

2.5 Frequency Selection

According to the name plate data, the maximum supply frequency that can be applied to the motor is 50Hz. To implement the v/f control, 5 to 50 Hz frequency range is being used.

In switching frequency selection, due to the relative ease in filtering harmonic voltages at high frequencies, it is desirable to use as high a switching frequencies as possible expect for one drawback. It is switching losses in the inverter switches increase proportionally with the switching frequency f_s. Therefore, in most applications, the switching frequency is selected to be either less than 6 kHz or greater than 20 kHz to above the audible range. If the optimum frequency turns out to be somewhere in the 6-20 kHz range, then the disadvantage of no audible range, then the disadvantages of increasing it to 20kHz are often outweighed by the advantage of

no audible noise with of 20 kHz or greater. Therefore, in 50 Hz type applications, the fundamental frequency of the inverter output may be required to be as high as 200 Hz. In our case, 2 kHz switching frequency was used.

2.6 Component Selection

2.6.1. Selection of IGBT Module

When using IGBT modules, it is important to select models which have the voltage and current ratings most suited for the intended application. In the selection of IGBT module, all six IGBTs and the converter circuits are considered. That is an N series IGBT module where all are inbuilt. The new package design has the connection terminals molded together with the casing, thereby reducing not only the number of parts needed for assembly but also the internal wiring inductance.

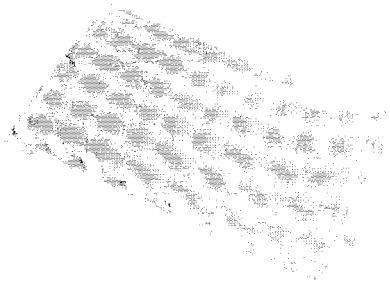


Figure 2.03: Encapsulated IGBT Module (7MBR15NF120)

Voltage rating

An IGBT must have a voltage rating that is suitable for dealing with the input voltage of the unit in which it will be installed. The voltage rating of an IGBT module must be selected by considering the input voltage to the IGBT. This IGBT module has 1200V collector to emitter and $\pm 20V$ across gate to emitter.

Current rating

An increase in the IGBT module's collector current will cause a rise in the $V_{ce(sat)}$ and the static power dissipation loss. At the same time the switching loss will grow, and as a result the module's temperature will rise. Despite the heat generated by the static loss and switching loss, the elements switching temperature should be maintained below 150 degree Celsius. Our IGBT module is selected by keeping the collector current at or below the maximum rating for the reasons, since this also reduces operation costs. This IGBT module has 15A collector to emitter current.

2.6.2. Converter Selection

The converter also is inbuilt inside 7MBR15NF120. A three phase rectifier included in this rectification. The terminals are molded together with the casing.

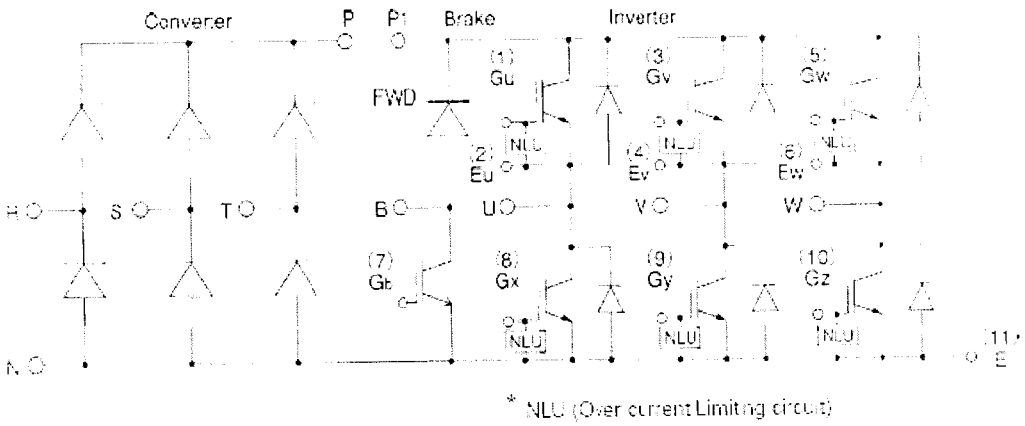


Figure 2.04: Internal diagram of 7MBR15NF120 IGBT Module

2.6.3. Object Oriented PIC (OOPic)

A new microcontroller called Object Oriented PIC (OOPic) is used to produce the six step waveforms. This module can be programmed using object orientation concept that is; all the methods or parameters have to be accessed through objects. There are preprogrammed multitasking Objects in the library of highly optimized Objects to do all the work of interacting with the hardware. The program can be written in Basic, C, or Java syntax styles to control the Objects. During operation, the Objects run continuously and simultaneously in the background while the scripts run in the foreground telling the objects what to do.

Another unique feature of OOPic is the Virtual Circuits capability. These are software equivalence of an electronic circuit connecting together Objects in various ways. This allows the Objects to pass data to each other in the background, not taking much processing power from the microcontroller.

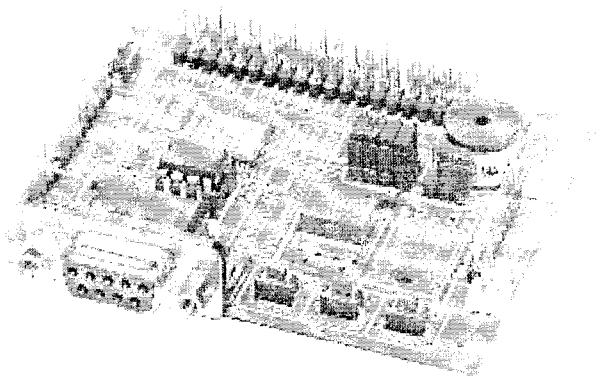


Figure 2.05: OOPic Hardware Module

- I^2C Network compatible
- Compact size
- Separate I/O pins to drive LCD displays
- Can be easily programmed using Serial or Parallel port
- A Power Good LED to show the status of the EEPROM clock
- Multiple power outputs available for different types of sensors
- External EEPROM can be connected

2.6.4. 16F767 Microcontroller

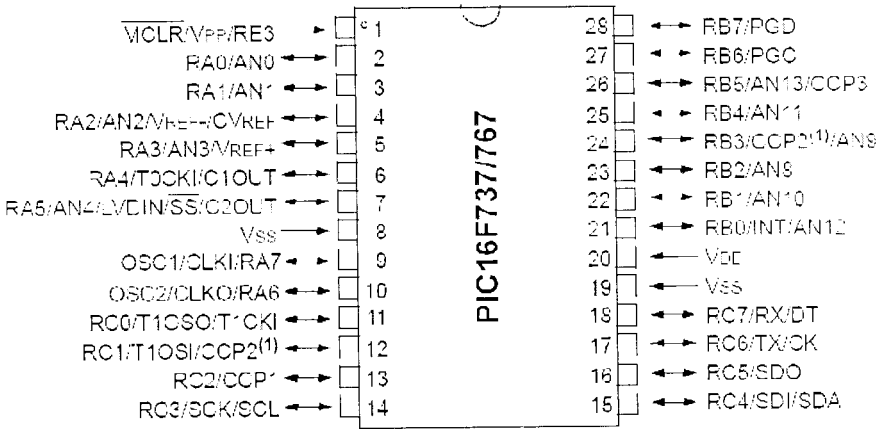


Figure 2.06: Pin diagram of PIC16F767

Main Features:

- 3 inbuilt hardware PWM modules with 10-bit resolution
- 8K flash program memory
- 16 Interrupts
- 20MHz Operating frequency (Oscillator)
- 3 Timers – Timer0, Timer1, Timer2
- 11 Analog to digital conversion modules with 10-bit resolution
- 28 pin DIP configuration

Special Peripheral Features:

- Two 8-bit Timers with Prescaler
- 16-bit timer/counter with Prescaler
- Three Capture, Compare, PWM modules:
  - Capture is 16-bit, max. Resolution is 12.5 ns
  - Compare is 16-bit, max. Resolution is 200 ns
  - PWM max. Resolution is 10 bits
- Power-on Reset (POR), Power-up Timer (PWRT) and Oscillator Start-up Timer (OST)
- Programmable Code Protection
- In-Circuit Serial Programming (ICSP) via two pins

2.6.5. IR21094 IC

The gate drive IC is a product of IR part named IR21094 which is a high speed and high voltage IGBT driver with single input control signals.

Features

- Floating channel designed for bootstrap operation
  Fully operational to +600V (V_{offset})
- Gate drive supply range from 10 to 20V (V_{out})
- Under voltage lockout for both channels
- 3.3V, 5V and 15V input logic compatible
- Shut down input turns off both channels

- Internal 540ns dead-time, and programmable up to 5us with one external RDT resistor

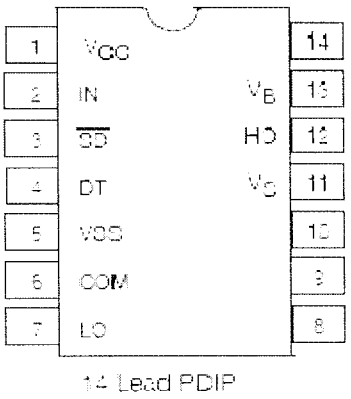
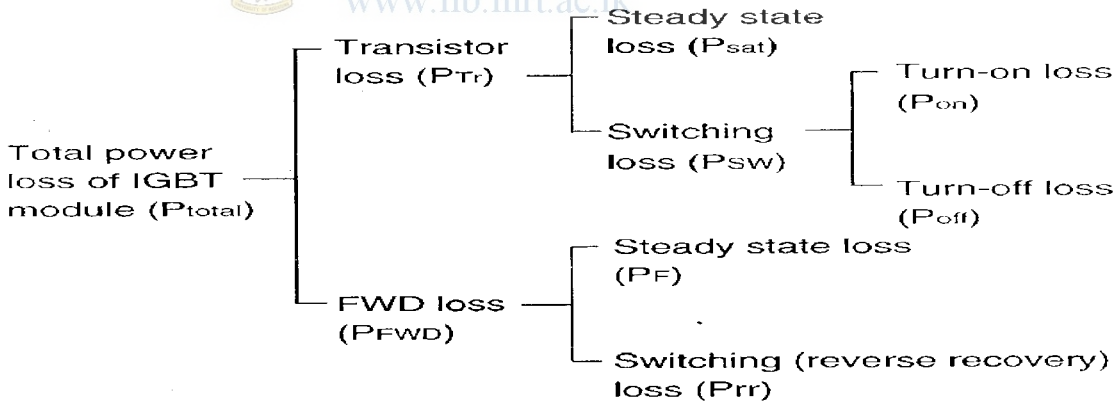


Figure 2.07: Pin diagram of IR21094

2.7 Heat Sink Design

When the power devices such as IGBT are in operation it produces the temperature at the junction. Therefore the IGBT junction temperature must be within the acceptable limit. Therefore to design a better cooling system we need to calculate the power loss in the IGBT module. Therefore we need to remove the heat dissipated on the IGBT module as efficiently as possible. Otherwise the IGBT module heated up to a high temperature. Therefore to avoid such abnormal situation we need to assemble a heat sink with the proper value. Therefore the selection of the heat sink is very important. The power loss calculation is given below.



IGBT power dissipation loss (W) = Steady state loss+ Turn-on loss + Turn-off loss

$$= [t1/t2 * Vce(sat) * Ic] + [fc * (Eon + Eoff)]$$

$$FWD\ Power\ Dissipation\ loss\ (W) = Steady\ Power\ Dissipation\ Loss\ (W) + Reverse\ Recovery\ Loss$$

$$= [(1-(t1/t2)) * I_F * V_F] + [fc * Err]$$

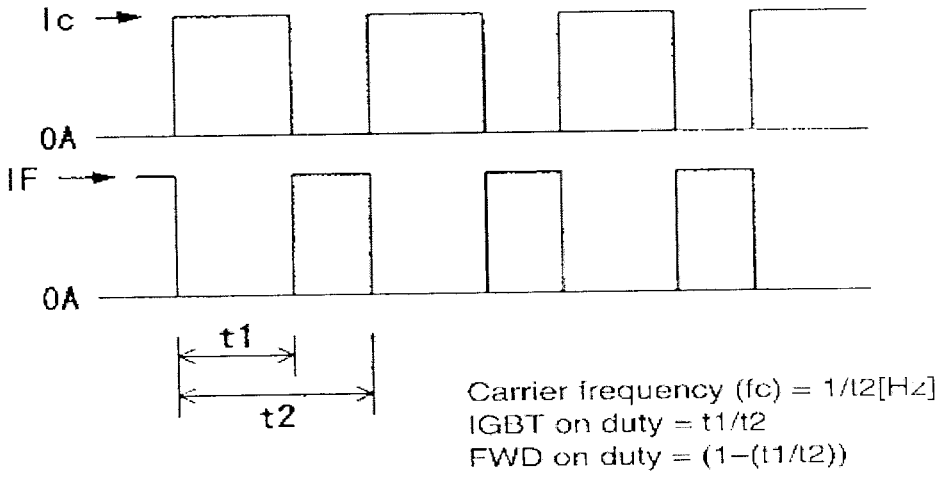


Figure 2.08: Duty Cycles in one leg two IGBTs

As the maximum allowable junction temperature of an IGBT module is fixed, an appropriate heat sink must be designed to keep it at or below this value. When designing appropriate cooling, first calculate the loss of a single IGBT module then based on that loss, select a heat sink that will keep the junction temperature within the required limits.

If the IGBT module is not sufficiently cooled, the junction temperature may exceed the junction temperature during operation and destroy the module.

According to the above two equation the values of the variables have found which is given below.

$\frac{t_1}{t_2} = 0.9, \quad f_c = 2kHz, \quad V_{ce} = 3.3V, \quad I_C = 10A$

$V_f = 1.5V, \quad I_f = 5A$

$E_{on} = \frac{1.0mJ}{cycle} \quad E_{off} = \frac{1.8mJ}{cycle} \quad E_{rr} = \frac{0.75mJ}{cycle}$

E_{on} = 1.0mJ / cycle E_{off} = 1.8mJ / cycle E_{rr} = 0.75mJ / cycle

The IGBT power dissipation loss $= 0.9 \times 3.3 \times 10 + 2 \times 1000 \times (1.0 + 1.8) \times 0.001$

$= 35.3W$

FWD power dissipation loss $= 0.1 \times 1.5 \times 5 + 2 \times 1000 \times 0.75 \times 0.001$

$= 2.25$

The total power loss $= 35.3 + 2.25 = 37.55$

The thermal resistance between the heat sink and the ambient air will be calculated as follows.

T_j = W (R_{th}(j-c) + R_{th}(c-f) + R_{th}(f-a)) + Ta.....(A)

T_j - Maximum junction temperature (125 °C)

W - Total power loss (88.4 W)

$R_{th(j-c)}$ - Thermal resistance between junction and case (1.04 °C/W)
$R_{th(c-f)}$ - Thermal resistance between case and the heat sink (0.05 °C/W)
$R_{th(f-a)}$ - Thermal resistance between the heat sink and ambient air
Ta - Ambient temperature (25 °C)

According to the equation (A),

$$125 = 37.55\left(1.04 + 0.05 + R_{th,\ heatsink}\right) + 25$$

$$Thereby, R_{th,\ heatsink} = 1.57^{\circ}C/W$$

2.8 System Block diagram

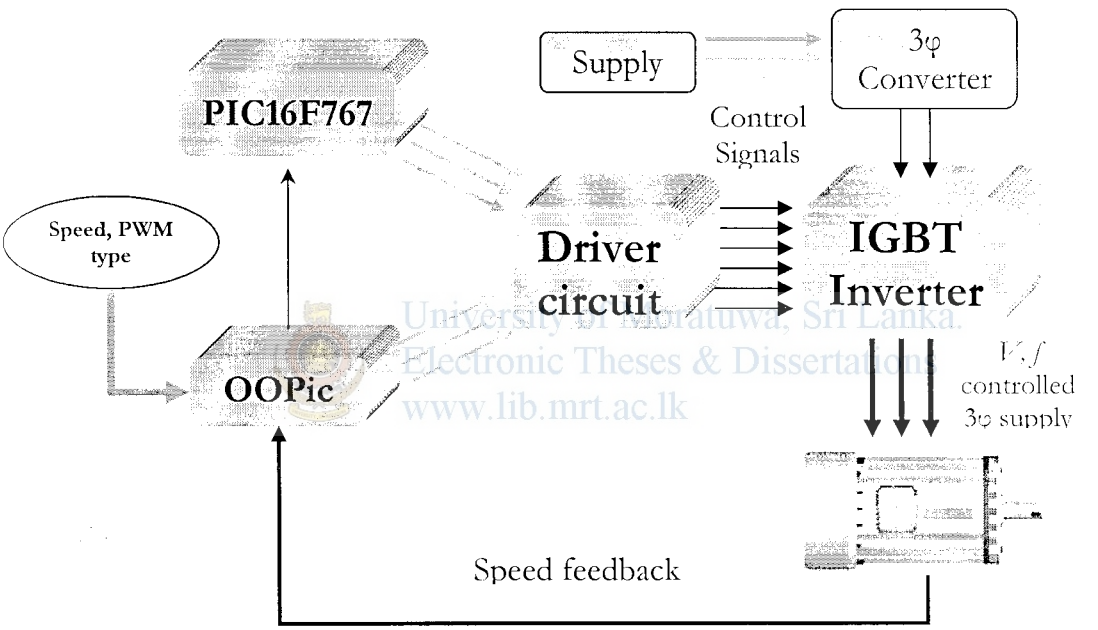


Figure 2.09: System Block diagram

3. Implementation

The complete system can be divided into six main sections as Main Control Circuit, Driver circuit, Converter & Inverter Circuit, Power supply circuit, Sensor Design and Interface Design. These things are explained in the following sections.

3.1 Main Control Circuit

The main control circuit is the important part of the system, which produces the control signals according to the algorithm. These control signals are used to switch ON/OFF the 6 IGBTs in the inverter. In this system, there are two types of algorithms implemented, one is Six Step and the other is sinusoidal PWM with V/ f control. To implement these, two microcontrollers are used.

- *OOPic Microcontroller*:- This produces the Six Step control signals, get the sensor feedback and Display the speed on LCD
- *PIC 16F767 Microcontroller*:- This produces the sinusoidal PWM signals for the 3 phases using the inbuilt 3 hardware PWM modules

3.1.1 Six Step Inverter Design

MATLAB implementation of Six Step Inverter Design

MATLAB Program


```
t = [0:6];
a = [3,6,3,-3,-6,-3,5];
b = [3,-3,-6,-3,3,6,3];
c = a - b;
subplot(3,1,1)
stairs(t,a)
title('Phase a')
axis([0 7 -10 10])
subplot(3,1,2)
stairs(t,b)
title('Phase b')
axis([0 7 -10 10])
subplot(3,1,3)
stairs(t,c)
title('Phase a - b')
axis([0 7 -10 10])
hold on
```

MATLAB Output

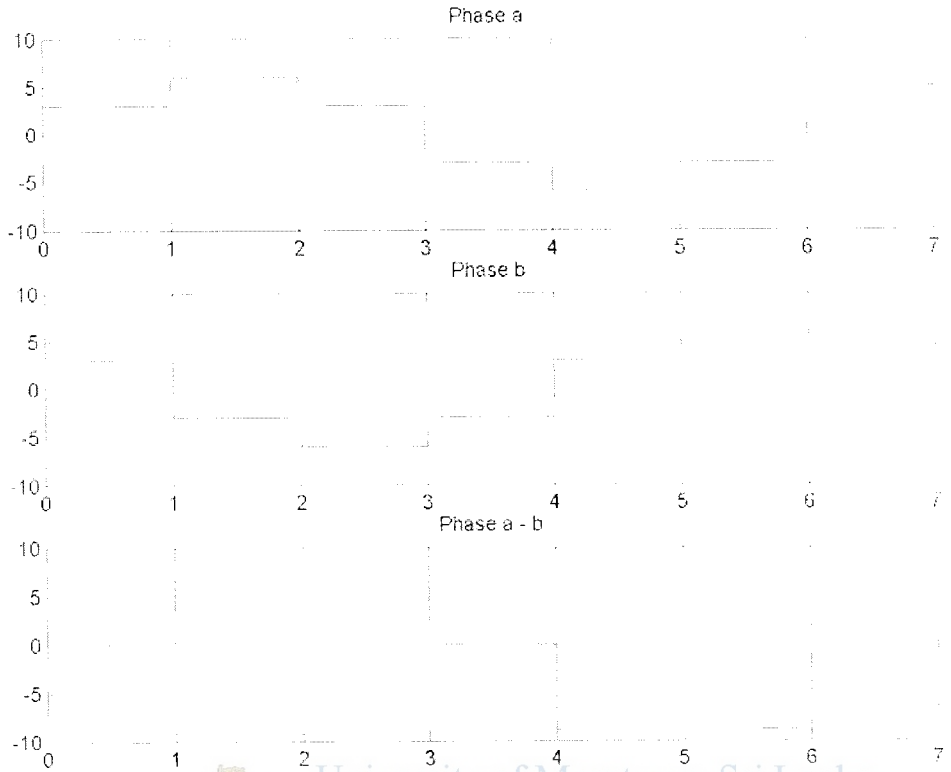


Figure 3.01: Six-step MATLAB output

Physical Design

This is a simple algorithm compared to sinusoidal PWM technique. As there are six steps in the phase voltage waveform, it is called Six Step Inverter.

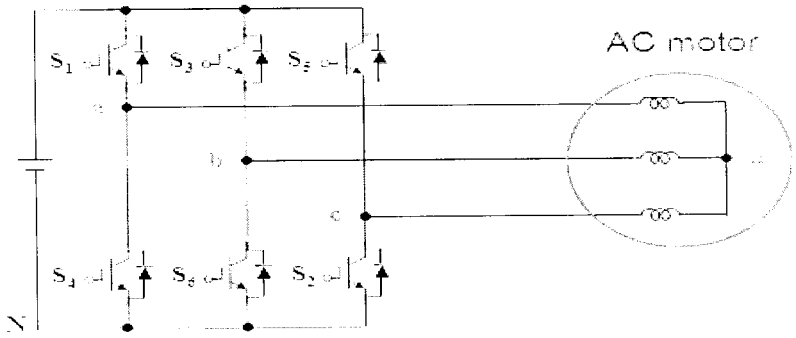


Figure 3.02: Inverter with six IGBT switches

As shown in the figure 3.03 the six switches (IGBTs) of the inverter are switched in a way such that a resultant sinusoidal waveform is applied across the motor windings. For this purpose, the total period is divided into six equal periods, in each period two one sided switches & one other side switch will be ON. For example, if S1 & S3 are ON, S5 will be in OFF state. The complete pattern is as follows:

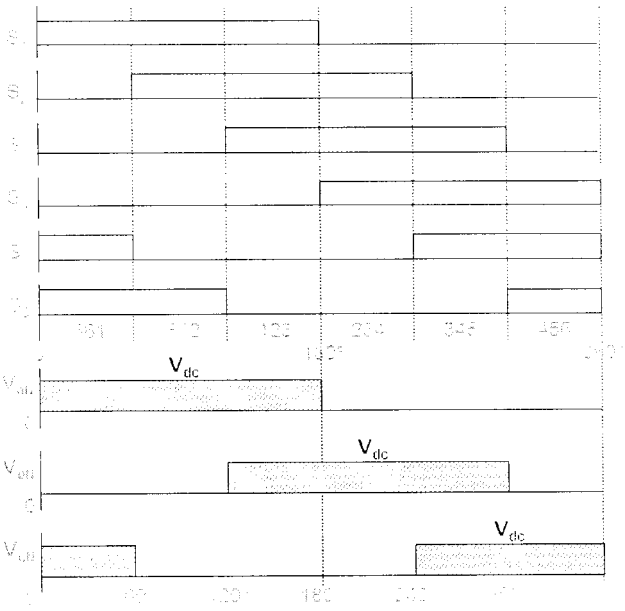


Figure 3.03: Six-step switching signal patterns

3.1.2 Implementation of Six Step Algorithm in the system

Six step algorithm is implemented in OOPic microcontroller. OOPic is used as the main controller. When the six step mode is selected, OOPic will produce variable frequency six step signals based on the potentiometer position. When the stop key is pressed, DC braking technique is used to stop the motor. This is achieved by supplying constant DC voltage to two coils only. The magnetic field generated by the coil will oppose the revolution. As the position of the potentiometer changes, it is converted into digital using 8 bit A/D converter of the OOPic microcontroller. This digitized value is used to change the period, thereby the period of six steps. In parallel with this, OOPic will process the feedback signal coming from the hall sensor and display it in the LCD. When the sinusoidal mode is selected, OOPic will send a signal to the PIC to activate it and it continues to sense the speed and display the speed.

The main disadvantage of six step algorithm is that it can be used to change the output frequency only. Output amplitude can be controlled by only changing the DC-link voltage (V_{dc}). But in six step, harmonics of order three and multiples of three are absent from both the line to line and the line to neutral voltages and consequently absent from the currents. In order to control the output voltage, PWM technique can be used. Among those many different PWM switching schemes, sinusoidal PWM technique is the most common method.

3.1.3 PWM Techniques

While the 3Φ 6-step inverter offers simple control and low switching loss, lower order harmonics are relatively high leading to high distortion of the current wave unless significant filtering is performed. PWM inverter offers better harmonic control of the output than 6-step inverter.

The dc input to the inverter is chopped by switching devices in the inverter. The amplitude and harmonic content of the ac waveform is controlled by the duty cycle of the switches. Various PWM techniques include:

- ✓ Sinusoidal PWM (most common)
- ✓ Selected Harmonic Elimination (SHE) PWM

- ✓ Space-Vector PWM
- ✓ Instantaneous current control PWM
- ✓ Hysteresis band current control PWM
- ✓ Sigma-delta modulation

3.1.4 Sinusoidal PWM method

MATLAB implementation of Six Step Inverter Design

MATLAB Program

```
n=9; %n = (carrier / modulation) frequency
fc=540; %carrier frequency
m=0.5; %m = (fundamental peak amplitude / carrier peak amplitude)
% tp = n/fc % triangular wave pulse wave length
ii=[];
tt=[];
val=[];
t_s=(n/fc)/n; % 1/9 of fundamental lamda
for i = 1:n,
   ii = [ii i];
   a = (2*pi*i/n);
   t = (1-m*sin(a))/(2*fc);
   t = t + t_s*(i-1);
   tt = [tt t];
   val = [val 5];
   ex_t = t_s*i;
   tt = [tt ex_t];
   val = [val -5];
end
subplot(2,1,1); stairs(tt,val) ,axis([0 0.02 -6 6])
x=0:0.1:65;
subplot(2,1,2); plot(sin(x)) ,axis([0 65 -1 1])
```

MATLAB Output

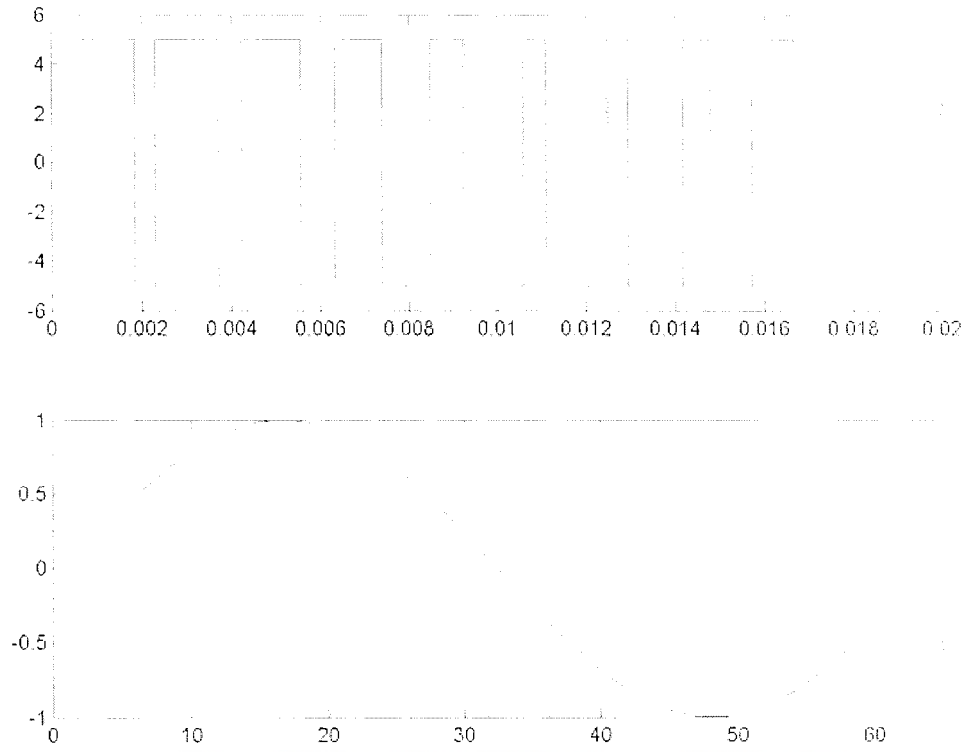


Figure 3.04: Sinusoidal PWM method MATLAB output

Physical Design

The most common PWM approach is sinusoidal PWM. Here, three reference sinusoidal signals with 120° shifted each other are compared with a triangular signal of high frequency. The relative levels of the two waves are used to control the switching of devices in each phase leg of the inverter.

As shown in figure 3.05, when the sinusoidal signal is greater than the triangular signal then the upper switch of the corresponding inverter leg is switched ON, and when the triangular is greater than the sinusoidal signal, the lower switch of the leg is triggered.

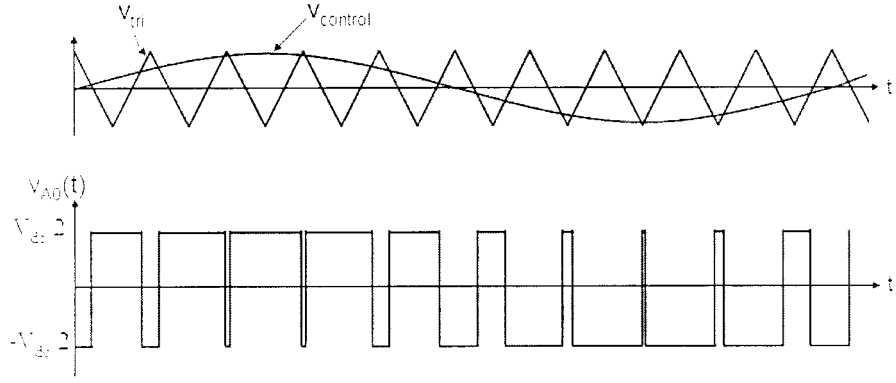


Figure 3.05: Sinusoidal PWM Technique

Here, the triangle waveform switching frequency (f_s) is called as the carrier frequency and the control signal frequency (f_c) is called as modulation frequency.

Frequency modulation ratio, $m_f = f_s / f_c$

Amplitude modulation ratio, $m_a = V_c / V_{tri}$

Important considerations:

- ✓ Normally $m_a < 1$
- ✓ Switching losses are high at high switching frequencies
- ✓ Switching frequency should be kept less than 6kHz or greater than 20kHz
- ✓ If $m_f < 21$, Asynchronous PWM should be avoided. That means, the value of m_f should be an odd integer.
- ✓ If $m_f > 21$, Asynchronous PWM can be implemented, but should be avoided at lower frequencies.
- ✓ Over-modulation ($m_a > 1$) gives higher output voltage, but causes the output voltage to contain many more harmonics in the sidebands as compared with the linear range ($m_a < 1$)

3.1.5 Implementation of sinusoidal PWM in the system

PIC 16F767 was selected as the microcontroller for the purpose of implementing the sinusoidal PWM technique in the system. This microcontroller has 3 PWM modules which can issue PWM signals, where the duty cycle can be changed. Those 3 PWM signal are used to send the switching signals to IGBT inverter.

The control program was written by MikroC, in which all the power and flexibility provided by ANSI C, accompanied with the most advanced IDE on the market. The source code of the PWM controller is available in the Annexure.

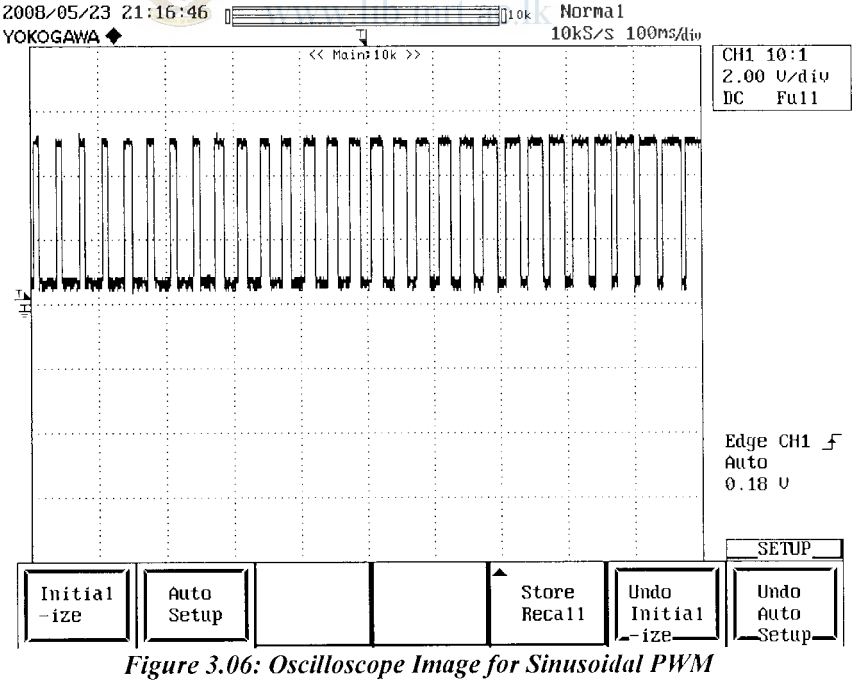


Figure 3.06: Oscilloscope Image for Sinusoidal PWM

3.1.6 Control Algorithm of sinusoidal PWM

The control signals are produced using the three 10-bit PWM modules inbuilt in the 16F767 microcontroller. The duty cycle of each PWM module is varied individually to generate a 3-phase AC waveform. As shown in the figure 3.07, three offset variables are used to get a 120° phase shift. Sine waveform is produced by

accessing a sine table stored in an array. Sine table is made for angles 90° to 270°. These values are repeatedly accessed to get the sine values of other angles. For example, the value for 0° is same as the value of 180° and the value for 50° is same as the value of 130°.

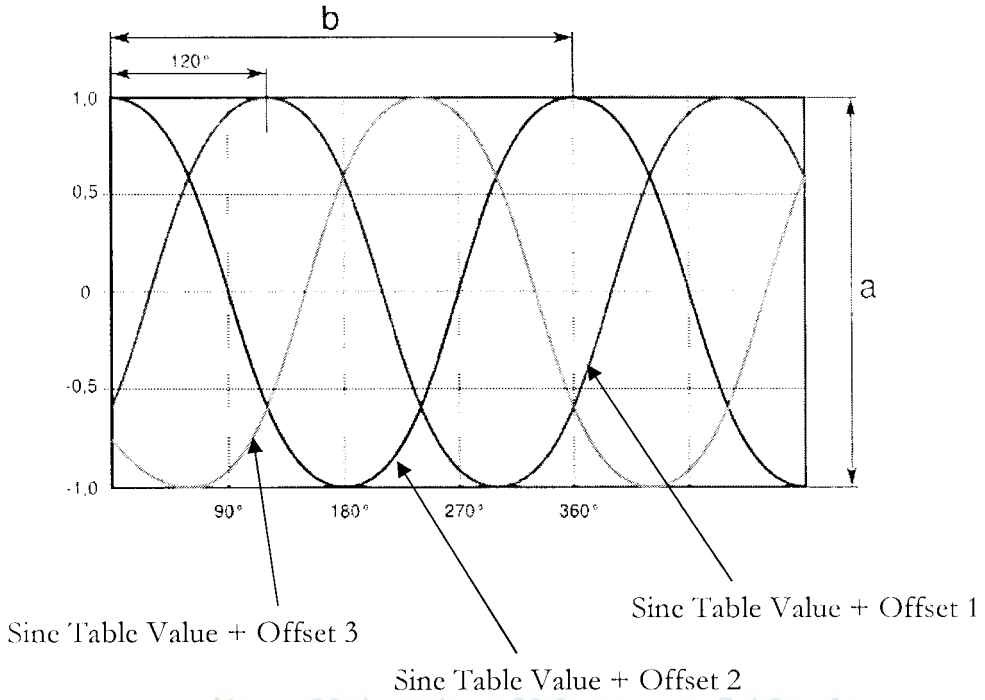


Figure 3.07: Three phase implementation Synthesis

The microcontroller uses the speed change potentiometer's Analog to Digital converted results to calculate the PWM duty cycle and thus, the frequency and the amplitude of the supply to the motor. Voltage level is changed by changing the duty cycle value only. That means, when the duty cycle is high, the resultant dc voltage is high. When the duty cycle is set to half value, the output will be half of the supply. The upper eight bits of the PWM's duty cycle is set using the register CCPRxL, while the lower two bits are set in bits 4 and 5 of the CCPxCON register. The PWM frequency is set using the Timer2 Period register (PR2). Since all of the PWMs use Timer2 as their time base for setting the switching frequency and duty cycle, all will have the same switching frequency.

Timer1 is used to change the frequency of the PWM output. Timer1 is a 16-bit hardware module available in the PIC16F767. By changing the Timer1 reload value, the frequency is changed. The Timer1 reload value is based on the potentiometer's ADC result, the main clock frequency (F_{OSC}) and the number of sine table entries. There are 19 values stored for the half cycle. So altogether there are 36 samples for one cycle. As explained earlier, 120° phase shift is achieved through accessing three offset registers, where each of these registers will point to one of the values in the table. These offsets will be updated in a way to get a sinusoidal waveform, after each Timer1 overflow. The Timer1 overflow is set as an interrupt for the microcontroller. In addition to that, there will be an interrupt when the ADC is completed.

After every Timer1 overflow, the PWM duty cycles are updated based on the potentiometer setting & sine table value. Then the offset values are updated in order to get a sine waveform. The sine table value is multiplied with the frequency input to

find the PWM duty cycle and is loaded to the corresponding PWM duty cycle register. Subsequently, the offset registers are updated for next access.

After updating the duty cycle and the offset values, ADC results are processed. When the conversion is completed, there will be an interrupt created. When an A/D interrupt occurs, the new frequency setting of pot is checked with the older value. If those two are different, the new value is used to calculate the current frequency. Also the time step required for unit change is calculated according to the acceleration / deceleration time. Then the Timer1 reload value is calculated based on the pot setting.

Finally Run / Stop key & Forward / Reverse key are checked for change in position. If the stop key is pressed, DC braking technique is used. That is, only two coils will be ON with constant DC voltage. The magnetic field generated by the coil will try to brake the shaft in each revolution. If the motor direction key is pressed, first the motor will be stopped & then PWM1, PWM2 and PWM3 duty cycle values will be loaded to PWM2, PWM1 and PWM3 duty cycle registers respectively. This is somewhat similar to interchanging the AC input lines of the motor. The duty cycle will remain the same until the next Timer1 overflow occurs, as shown in *Figure 3.08*. The frequency of the new PWM duty cycle update determines the motor frequency and the value loaded in the duty cycle register determines the amplitude of the motor supply.

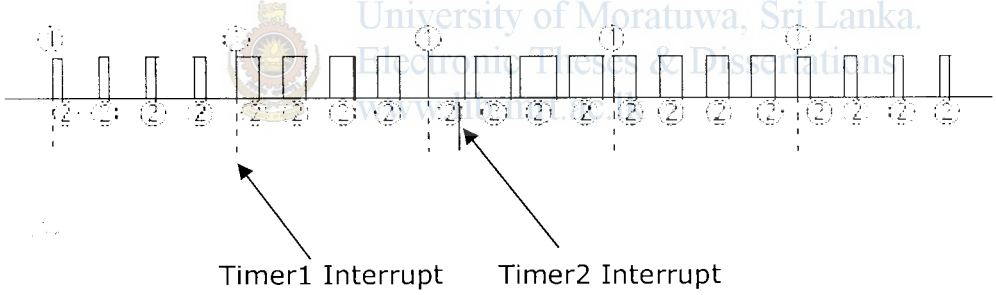


Figure 3.08: Duty cycle change with Timer1

PWM Duty Cycle = Frequency Setting of the pot x Sine table value Read

$$Timer1\ Reload\ Value = FFFFh - 2 \times \left(\frac{\frac{F_{osc}}{4}}{sine\ Sample\ per\ Cycle \times Timer1\ Prescaler \times Value\ of\ AN1} \right)$$

3.1.7 Acceleration and Deceleration

Acceleration and deceleration time can be changed in the program. Currently it is set to 3s. The current motor frequency and the required user frequency which is set through the potentiometer are compared. If these two are different, then the current frequency is changed step by step until it reaches the new frequency. The time to

change the current frequency by one step is calculated in software, depending upon the difference and the acceleration and deceleration parameters in the program.

3.1.8 Program Flowchart

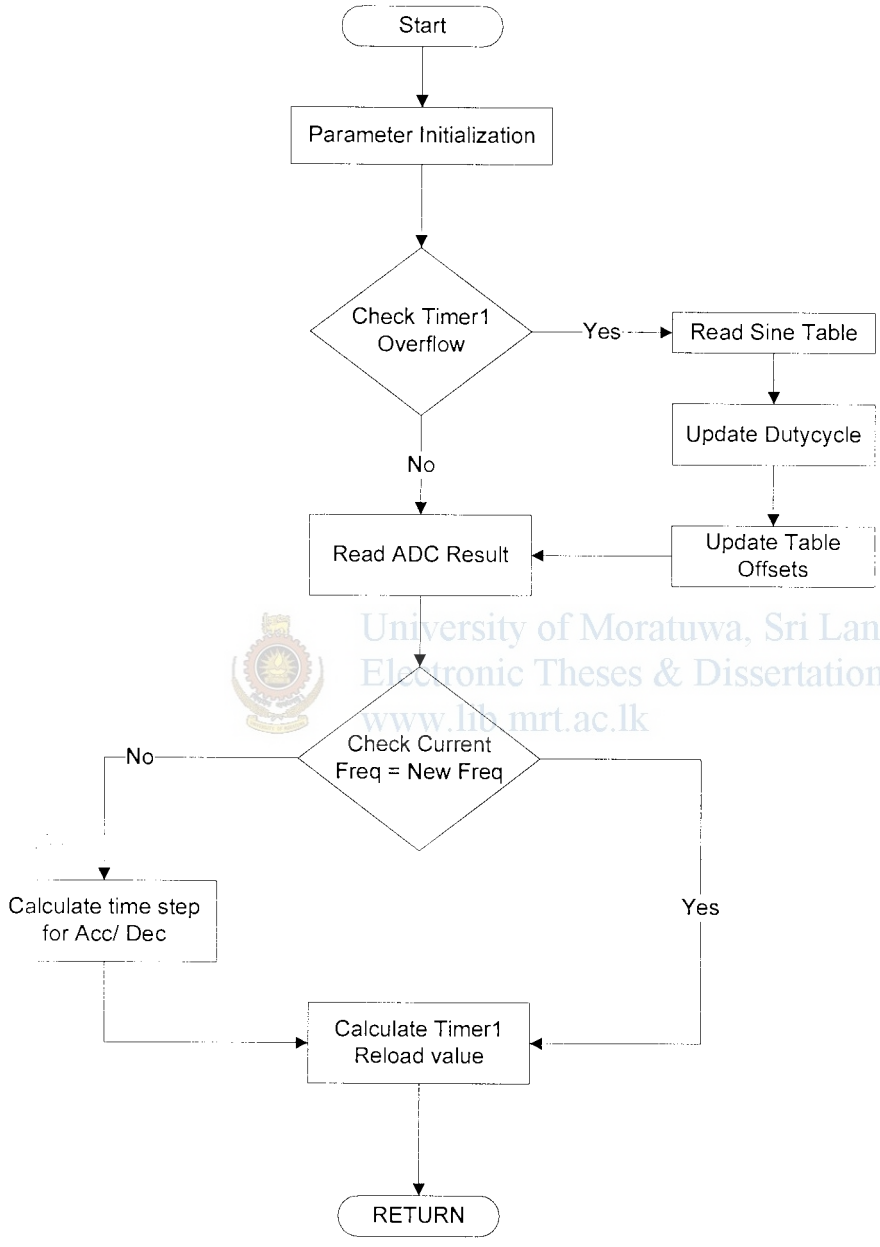


Figure 3.09: Program Flowchart

3.2 Driver Circuit of IGBT Module

3.2.1 Introduction

It is important that drive circuit design is closely linked to the protection circuit design such as,

- Over current protection
- Over voltage protection
- Provide electrical isolation

The design of the drive circuit ultimately determines the performance of the IGBT. The characteristics of the IGBT change in accordance with the conditions of the drive circuit.

Drive circuits consist of a forward bias voltage section to turn the IGBT on and a reverse bias voltage section to accelerate and maintain turn-off.

3.2.2 Drive Circuit Design

The first step of the circuit design was to design the IGBT gate drive circuit with appropriate ratings which matches the selected frequency of operation and voltages. The purpose of the drive circuit is to provide

- Optically isolated control signals
- Inverting the control signals
- Producing dead band time in the control signals
- Increase the voltage of control signal to 10-15V

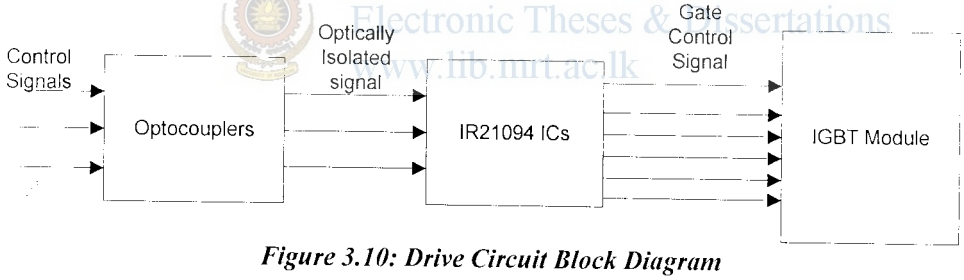


Figure 3.10: Drive Circuit Block Diagram

The PWM control signals generated by PIC are sent to Opto-Couplers which will optically isolate the Drive circuit and IGBTs from the PIC controller circuit to maintain a separate power ground in the IGBT side and logic ground in the controller side.

Using a single isolated signal, IR21094 IC produces two inverted signals with proper dead band timing. As the gate voltage of IGBT must be 10-15V higher than the drain voltage, this IC generates the control signal with this voltage using an external 15V DC supply.

As this is a three phase PWM control, three 6N135 Opto-Couplers and three IR21094 ICs are used to produce the three phase control signals. The operation of the drive circuit is shown in figure 3.10.

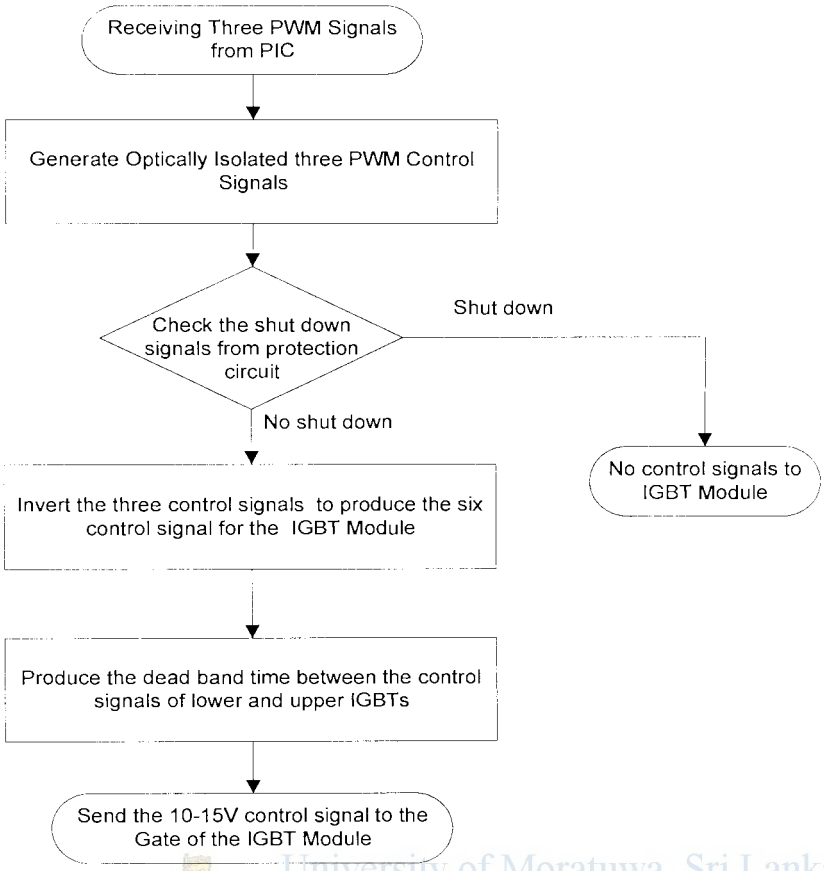


Figure 3.11: Flowchart of Drive Circuit Design

3.2.2.1 Optocoupler Isolation

In electronics, an opto-isolator is a device that uses a short optical transmission path to transfer a signal between elements of a circuit, typically a transmitter and a receiver, while keeping them electrically isolated. Since the signal goes from an electrical signal to an optical signal back to an electrical signal, electrical contact along the path is broken.

For inverter circuits and the like, it is necessary to electrically isolate the IGBT from the control circuit. Unlike an isolated transformer, the optocoupler

- Separate power ground and logic ground
- Provides significant protection from serious over voltage conditions
- Withstand fast switching signals
- Allows DC coupling
- Also, the optocoupler does not limit the output pulse width

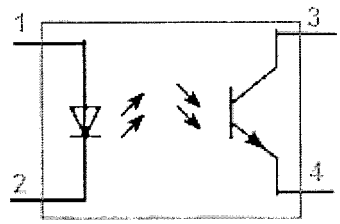


Figure 3.12: Schematic diagram

Simply, when an electrical signal is applied to the input of the optocoupler, its LED lights, its light sensor then activates, and a corresponding electrical signal is generated at the output. The simplified diagram of an optocoupler is shown in figure 3.12 to illustrate the basic operation.

Optocoupler Selection

To get the optical isolation, first it was decided to use PC816 optocoupler which is a low cost locally available one with the following features:

- Current transfer ratio ($I_f = 5mA$, $V_{ce} = 5V$)
- Rise time (typical 4 μs and maximum 18 μs)
- Fall time (typical 3 μs and maximum 18 μs)

The following figure 3.13 shows the rise time and fall time observed using an oscilloscope.

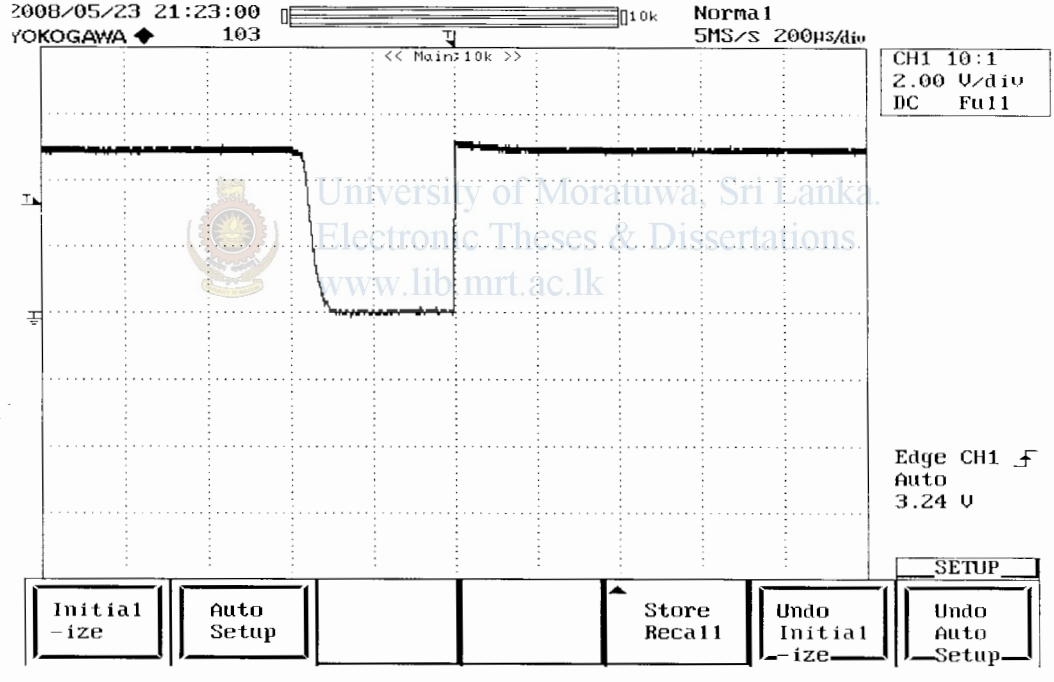


Figure 3.13: PC816 Optocoupler oscilloscope Images

As the rise time was too small to compare with fall time, two separate diagrams were derived to observe the values. According to the oscilloscope images, the rise time is less than 1.5µs and fall time is less than 100 µs.

The rise time and fall time were comparably large with the duration of 20 kHz switching signals and this can be used with only in higher frequency application (one pulse width $\leq 100\,\mu s$ (switching frequency $\geq 10\,kHz$). Less frequency values cannot be used.

Due to these bottlenecks, a decision was taken to select 6N135 series IC which has some robust features as given below even though it was not available in the local markets. Ultimately, 6N135 was imported.

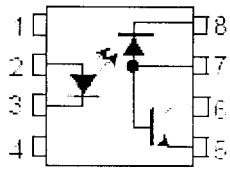


Figure 3.14: 6N135 Schematic Diagram

Features

- Isolation voltage 2500Vrms (min.)
- High speed: tpHL, tpLH = 0.5μs (typ.) (RL = 1.9kΩ)
- Rise time (typical 1 μs and maximum 1.5 μs)
- Fall time (typical 0.2 μs and maximum 1.5 μs)

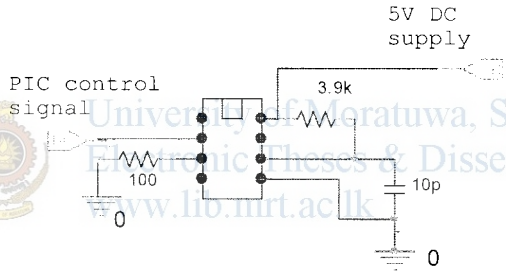


Figure 3.15: 6N135 Circuit Diagram

The figure 3.16 shows isolated signals of 6N135 observed using an oscilloscope.

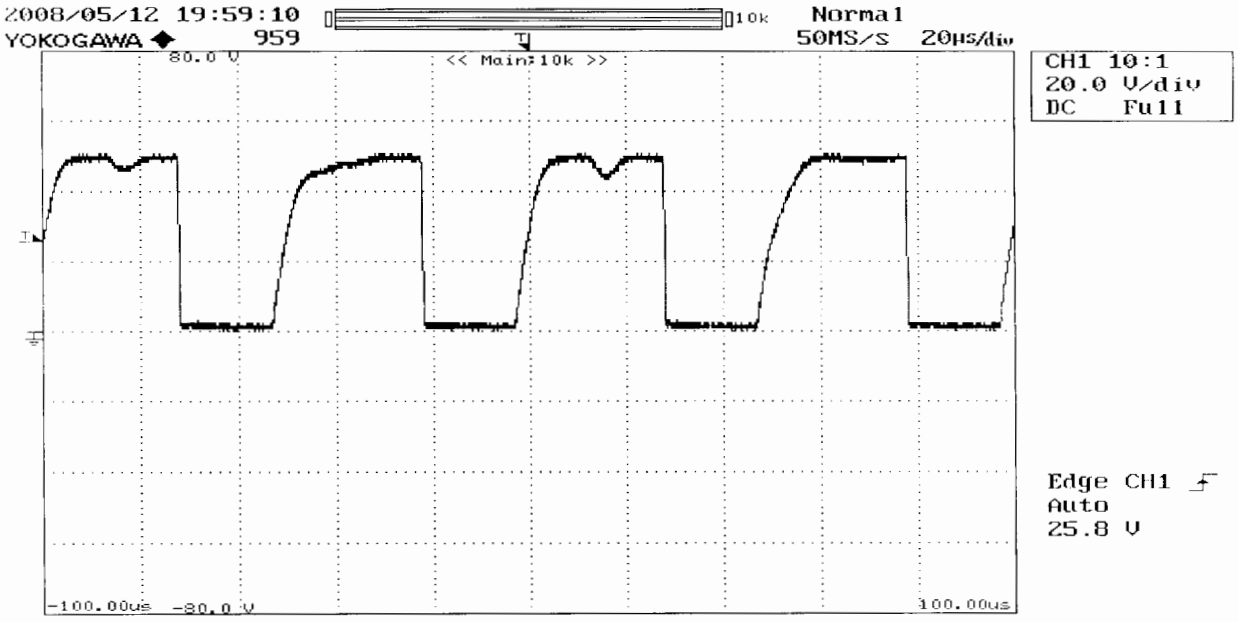


Figure 3.16(a): 6N135 Optocoupler oscilloscope Image (Pulse Stream)

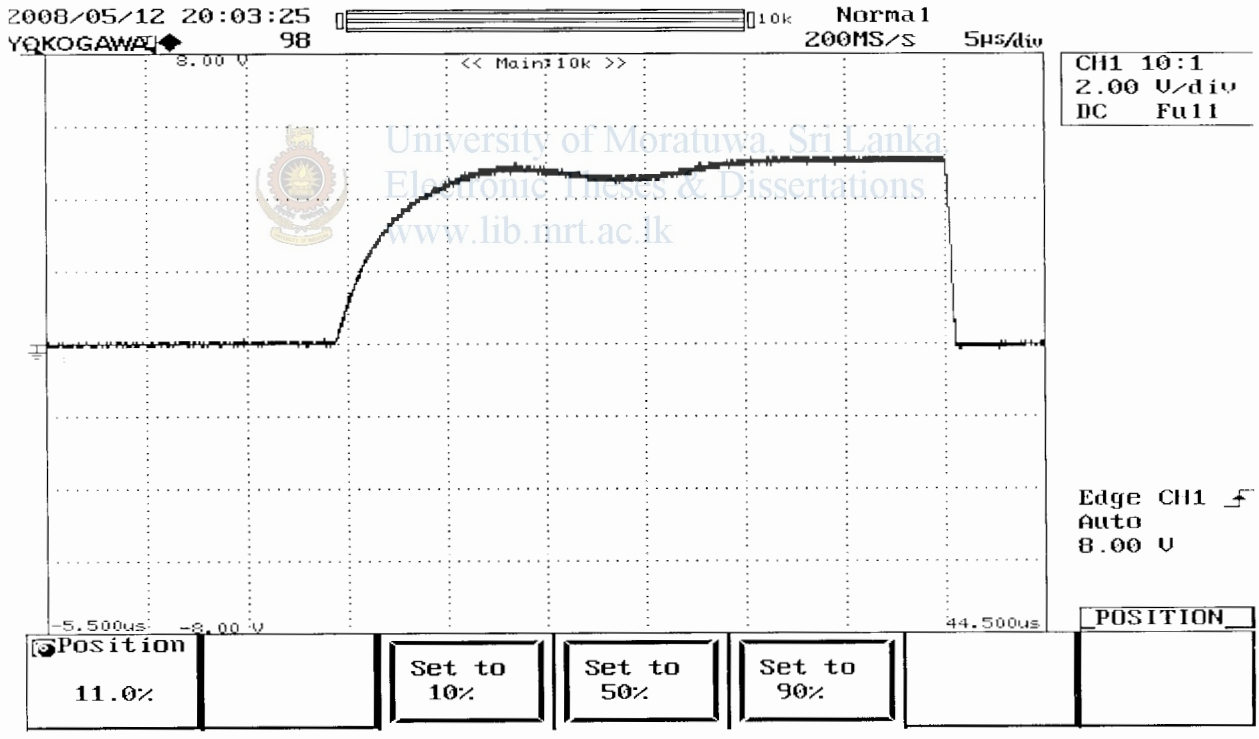


Figure 3.16(b): 6N135 Optocoupler oscilloscope Image (Single Pulse)

The rise time is less than 5µs and the fall time is 1µs. It is acceptable in comparing with switching signals. Furthermore, this way turn-on and turn-off characteristics determined by gate resistance can be set separately, so it is commonly used to ensure the best settings.

3.2.2.2 Control signal inversion and Dead band time generation

The power of the control signal produced by optocoupler is not sufficient to drive the gate of IGBTs. The power required to energies the gates varies with the Dc bus voltage significantly from about 50mA to about 500mA. So the drive ICs should be capable of delivering this current to the gates without affecting its performance.

IR2110

The gate drive IC is a product of IR part named IR2110 which is a high speed IGBT driver with independent high and low side input signals.

Features

- Floating channel designed for bootstrap operation
  Fully operational to +500V (V_{offset}), Tolerant to negative transient voltage dV/dt immune
- Gate drive supply range from 10 to 20V (V_{out})
- Under voltage lockout for both channels
- 3.3V logic compatible (Separate logic supply range from 3.3V to 20V and Logic and power ground ±5V offset)
- Cycle by cycle edge-triggered shutdown logic
- ton/off (typ.) 120 & 94 ns

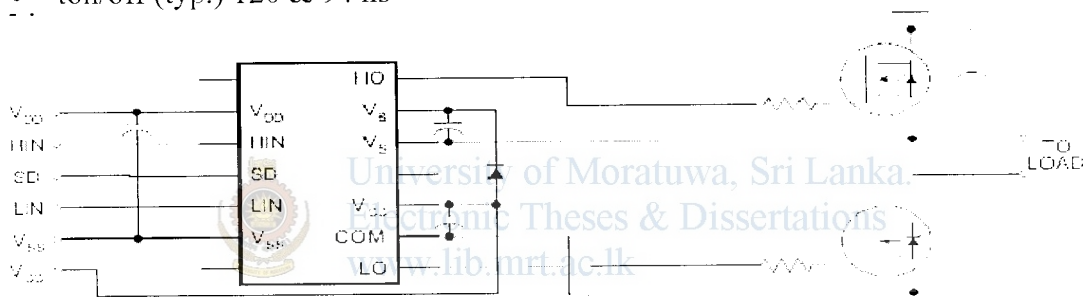


Figure 3.17: IR2110 Connection diagram

IR21094 IC

The gate drive IC is a product of IR part named IR21094 which is a high speed and high voltage IGBT driver with single input control signals.

Features

- Floating channel designed for bootstrap operation
  Fully operational to +600V (V_{offset})
- Gate drive supply range from 10 to 20V (V_{out})
- Under voltage lockout for both channels
- 3.3V, 5V and 15V input logic compatible
- Shut down input turns off both channels
- ton/off (typ.) 750 & 200 ns
- Internal 540ns dead-time, and programmable up to 5us with one external RDT resistor

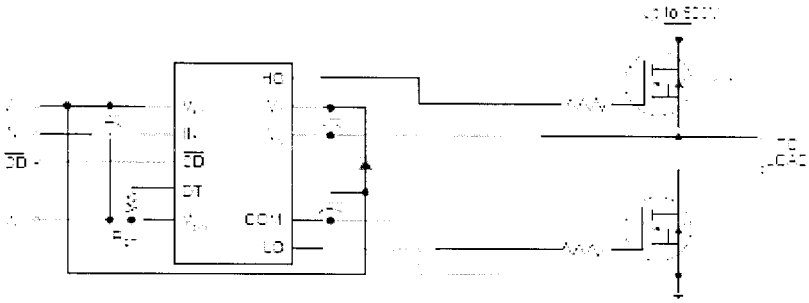


Figure 3.18: IR21094 Connection diagram

An isolated supply is connected between the pin COM and V_S. Typically the pins HO and LO are connected to the upper side device and lower IGBTs respectively, as shown in figure 3.18 (Complete three phase circuit is given in Annexure). The high side channel will switch the output (HO) between the positive of this supply and its ground in accordance with the input command. C_{Boot} is the bootstrap capacitor connected in RHS of IC which level shift the voltage at Vs by 10-15V.

Gate voltage must be 10-15V higher than the drain voltage. This is because, being a high side switch, such gate voltage would have to be higher than the DC Bus voltage, which is frequently the highest DC voltage available in the system. Therefore the high gate signal has to be always 10-15V higher than voltage at point "N" which may go up to the DC bus voltage. The so-called two IR ICs will be able to give this increased gate control signals.

IR2110 IC needs two control input signals (direct and inverted signals) and just only increases the gate voltage 10-15V range in the IC output signals. In addition to that, both ICs have protection shut down capabilities. But, IR21094 uses only one direct input signal and easily produce the two output signals with variable dead band time.

So in order to reduce the cumbersome of using extra circuit to invert the signals and to produce dead band time, IR21094 IC was selected even though it was not available in the local markets but it was imported.

Dead-band time

Because of finite turn-on time and turn-off time of switches, there should be a blanking time (t_d) after switching one switch off in a leg before switching on the other switch in the same leg. The blanking time will increase or decrease the output slightly depending on the direction of the load current.

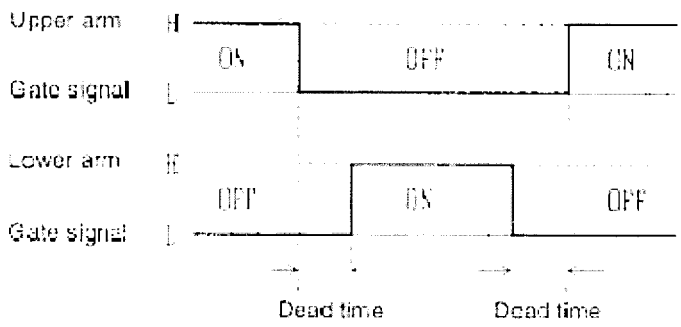


Figure 3.19: Dead band time signals

Need of Dead Band Time

It is important to be careful with dead times that are too short, because in the event of a short circuit in the upper or lower arms, the heat generated by the short circuit current may destroy the module.

If the two signals were perfectly complementary, then there would be a momentary short circuit between the DC bus positive and negative terminals. This occurs when the two signals change their state from 0 to 1 and vice versa.

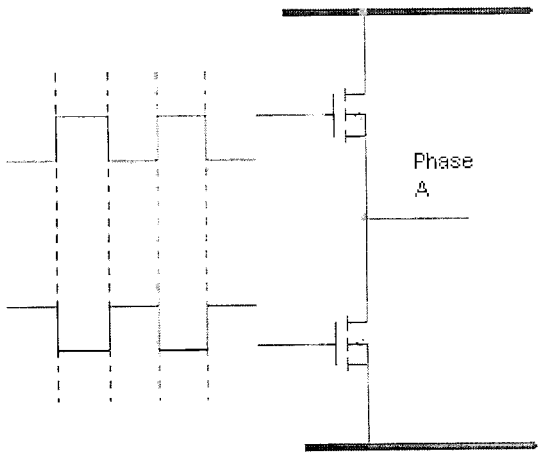


Figure 3.20: Inverted Control Signal

This causes the short circuiting of the DC Bus drawing a high amplitude current spike from the source. When this process is repeated at a very high frequency, it would cause the switches to heat unnecessarily leading to a probable damage to them.

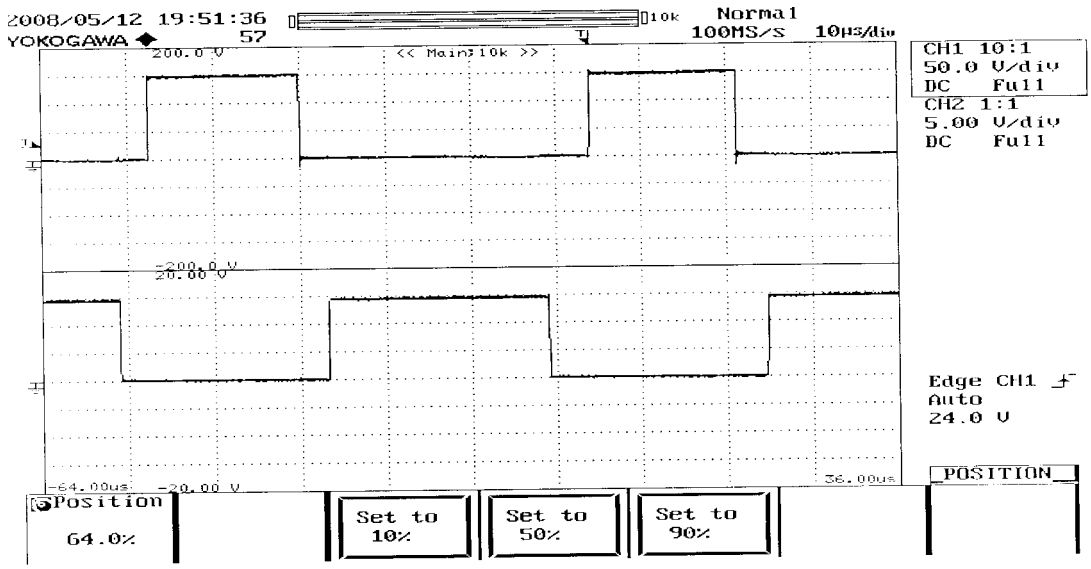


Figure 3.21(a): Dead band time observation using Oscilloscope (Pulse Stream)

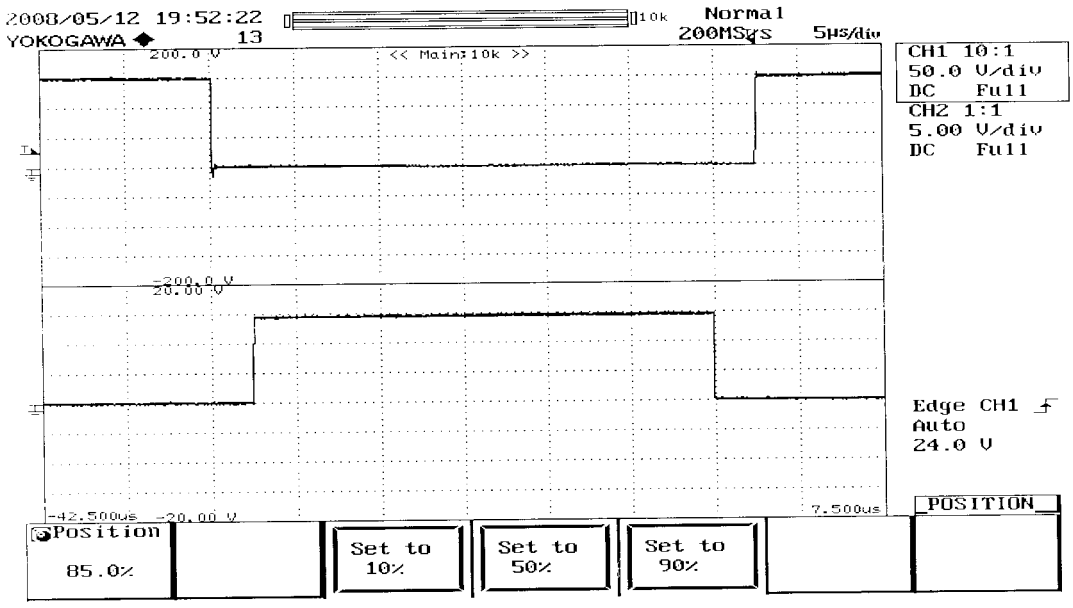


Figure 3.21(b): Dead band time observation using Oscilloscope (Single Pulse)

The dead band timing should be higher than 3 μs to Fuji type IGBT modules. According to the above observation, the dead time set to is acceptable. It can be increased by changing the R_{DT} resistor in figure 3.18.

3.2.3. Designing protection circuits

Since IGBT modules may be destroyed by over current, over voltage, or some other abnormal conditions, it is necessary to design protection circuits. It is important when designing these circuits that a module's characteristics are fully taken into consideration, since an inappropriate circuit will allow the module to be destroyed. (For example, the over current cut-off time may be too long or the capacitance of the Snubber circuit's capacitor may be too small.)

3.2.3.1. Short circuit (over current) protection

In the event of a short circuit, first the IGBT's collector current will rise and then, once it has reached a certain level, the C-E voltage will shoot up. Depending on the device's characteristics, during a short circuit, the collector current can be kept at or below a certain level. However, the IGBT will still continue to be subjected to a heavy load of high voltage and high current, and therefore this burden must be removed as soon as possible. The amount of time allowed between the start of a short circuit until the current is cut off, is limited by the IGBT's short circuit withstand capability. Short-circuit withstand capability is 15micro second minimum

In general, the higher the supply voltage or temperature rises, the lower the short-circuit withstand capability.

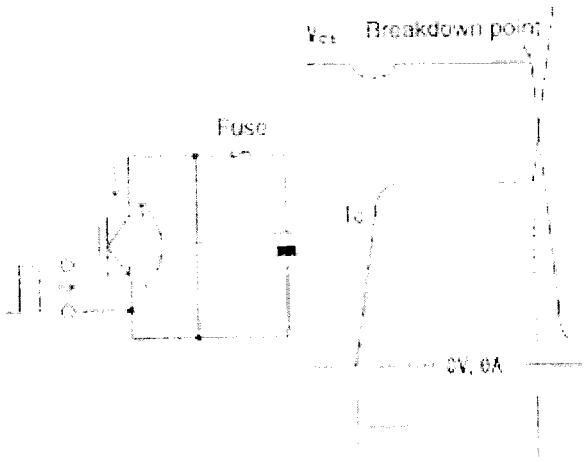


Figure 3.22: Short circuit withstand capability

The most difficult challenge in producing an IGBT was making gate controlled over current protection possible.

Detection in the circuit

The figure 3.23 shows the insertion methods for over current detectors, and the below table lists the features of the various methods along with their detection possibilities. After determining what kind of protection is necessary, select the most appropriate form.

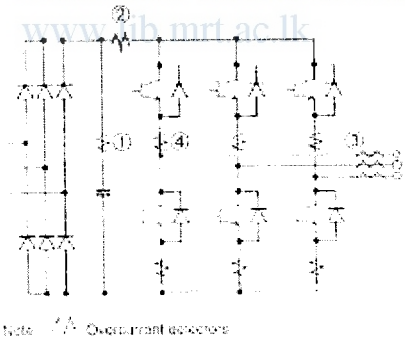


Figure 3.23: Over current detector insertion methods

Detection insertion position	Features	Detection function
Inser[illegible] in line with smoo[illegible]g capacitor	• AC current transformer available • Low detection precision	• Arm short-circuit • Series arm short-circuit • Short in output circuit • Ground fault
Inser[illegible] at inverter inpu[illegible]	• Necessary to use DC current transformer • Low detection precision	• Arm short-circuit • Series arm short-circuit • Short in output circuit • Ground fault
Inser[illegible] at inverter outp[illegible]	• AC current transformer available for high frequency output equipment • High detection precision	• Short in output circuit • Ground fault
Inse[illegible] in line with swit[illegible]	• Necessary to use DC current transformer • High detection precision	• Arm short-circuit • Series arm short-circuit • Short in output circuit • Ground fault

Figure 3.24: Over current detector insertion positions and functions

As stated previously, in the event of short-circuit, the IGBT must be disabled as soon as possible. Therefore, the delay from over current detection to complete turn-off in each circuit must be made as short as possible.

Since, an IGBT turn off very quickly, if the over current is shut off using an ordinary drive signal, then the collector-emitter voltage will rise due to the inductive kick, and the IGBT may be destroyed by over voltage (RBSOA destruction). Therefore, it is recommended that when cutting off the over current that the IGBT must be turned off gently (soft turn-off).

Detection using Vce (sat)

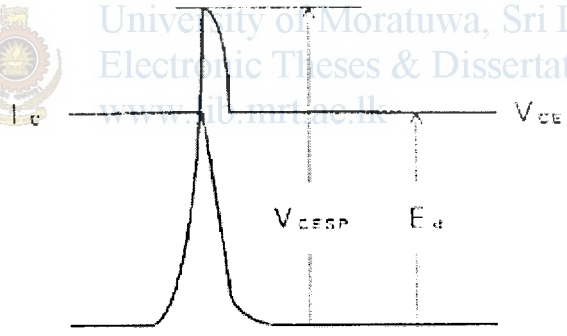
This method can protect against all of the short-circuit types listed in the above table. Operations from over current detection to protection are done on the drive circuit side. This offers the fastest protection possible.

Fuji Electric's gate driver ICs have the same kind of protective circuit built in, thereby simplifying the drive circuit design.

3.2.3.2. Over voltage protection

Over voltage causes

Due to the high switching speed of IGBTs, at IGBT turn-off or during FWD reverse recovery, the current change rate is very high. Therefore, the inductance of the wiring surrounding the module can cause a turn-off surge voltage.



Vce: IGBT collector-emitter voltage
Vcesp: Turn-off surge voltage peak value
Ic: IGBT collector current

Figure 3.25: Turn-off current and wave forms

The turn-off surge voltage peak can be calculated as follows:

Vcesp= Ed+ (L*dIc/dt)

dIc/dt-maximum collector current change rate at turn-off

If Vcesp exceeds the IGBT's C-E (Vces) rating, then the module will be destroyed.

Gate Over voltage protection

It is necessary that IGBT modules, like other MOS based elements, are sufficiently protected against static electricity. Also, since the G-E absolute maximum rated voltage is $\pm 20V$, if there is a possibility that a voltage greater than this may be applied. Then as a protective measure it is necessary to connect a zenner diode between the gate and emitter as shown in below figure 3.26.

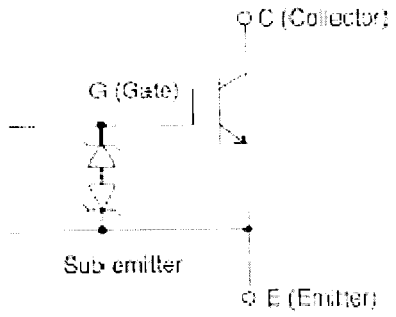


Figure 3.26: G-E over voltage circuit protection circuit

3.2.4. Consideration of Drive circuit implementation / points of caution

1. Optocoupler noise ruggedness

As IGBTs are high speed switching elements, it is necessary to select an optocoupler for drive circuit that has high noise ruggedness. Also, to prevent malfunctions, the wiring from different sides was not allowed to cross. Furthermore, in order to make full use of the IGBT's high speed switching capabilities, we recommend using an optocoupler with a short signal transmission delay.

2. Wire connection between drive circuit and IGBT

When connecting IGBT modules in parallel, due to the gate circuit's wiring inductance and the IGBT's input capacitance, as the gate voltage rises a parasitic oscillation may occur. Therefore, in order to prevent this oscillation, a gate resistor (47Ω) was connected in series to each of the modules gates. If the connection between the drive circuit and the IGBT is long, the IGBT may malfunction due to gate signal oscillation or induced noise.

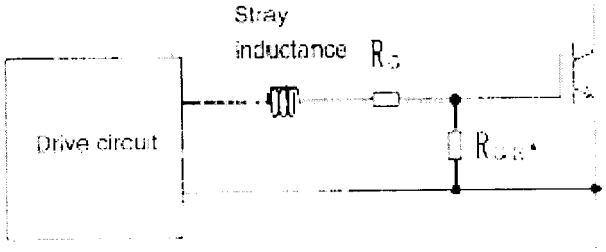


Figure 3.27: Gate signal oscillations counter measure

3.3 Power Supply Unit

There are 3 main DC power supplies require in the power supply unit.

- DC supply before the optical isolation
- DC supply after the optical isolation

3.3.1. DC supply before the optical isolation

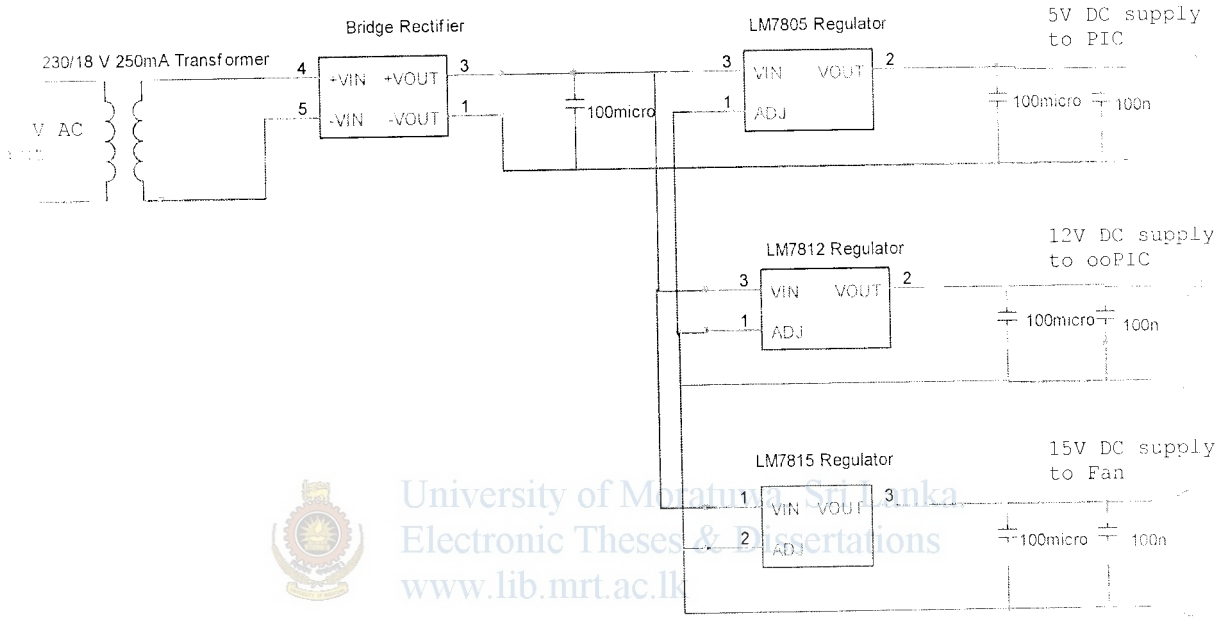


Figure 3.28: DC supply before isolation

3.3.2. DC supply after the optical isolation

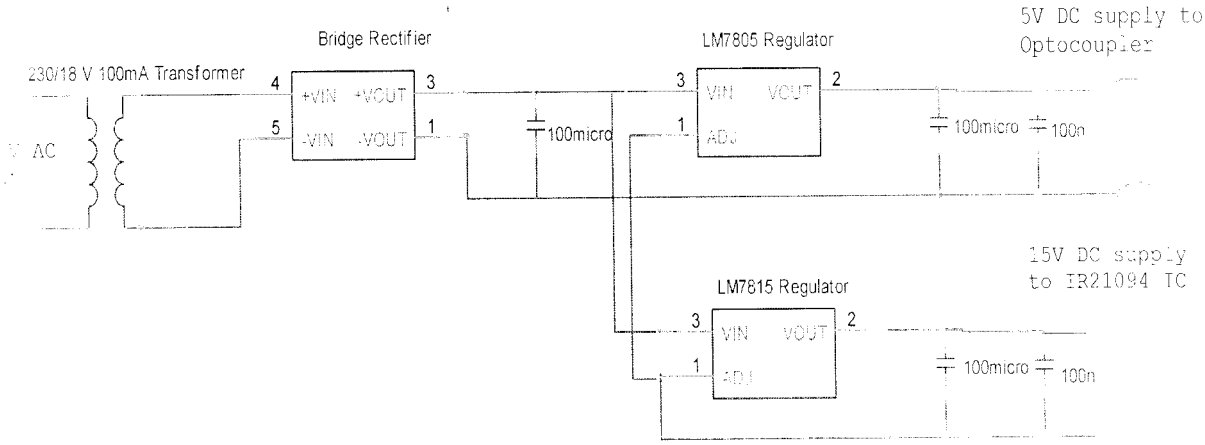


Figure 3.29: DC supply after isolation

3.4 Sensor Design

Sensors are critical component in a motor control system. Normally there are sensors detect the speed, current, voltage, position, and direction of the rotating motor. Recent advancements in sensor technology have improved the accuracy and reliability of sensors, while reducing the cost. Many sensors are now available that integrate the sensor and signal-conditioning circuitry into a single package. These sensors are used in the control loop and to improve the reliability by detecting fault conditions that may damage the motor.

3.4.1 Speed sensor design using Hall Effect sensor

In this programmable induction motor project, speed is the main controlling parameter and it is important to measure the speed correctly and control it accordingly. For this purpose, we employed a hall sensor to generate pulses once each rotation and this pulse type signal is used to count the speed in the microcontroller and displays it in the LCD in rpm units. Hall Sensor was selected for this purpose as it gives required accuracy and performance with very low cost.

The operating principle of a hall sensor is that, it will induce a perpendicular voltage when a sufficiently strong magnetic field comes close to the sensor. This voltage is some times proportional with the field strength but a switch type IC was selected to get the pulses. Hall element is used to sense the change in flux in the gap between a magnet and a notch in a rotating shaft or a passing ferrous gear tooth. The main advantage of Hall Effect tachometers is that they are a non-contact sensor that is not limited by mechanical wear. Hall Effect switches consist of sensor and sensor conditioning circuit in a small IC packages. The circuitry inside the sensor typically consists of a comparator or Schmitt trigger to provide a digital output signal that can be directly connected to the microcontroller.

Sensor output voltage can be varied as needed because it depends on the supply voltage. One drawback in hall sensors is that its accuracy changes greatly with the variation of the temperature; anyhow it is not a significant factor in our project.

3.4.2 The Hall phenomenon

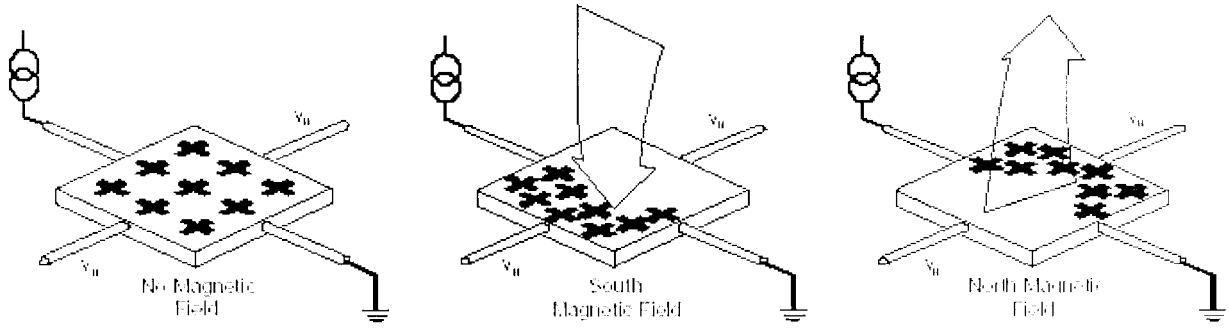


Figure 3.30: Hall Effect phenomena

Hall voltage = σ*B, where σ is the sensitivity in volts / Gauss and B is applied field in Gauss.

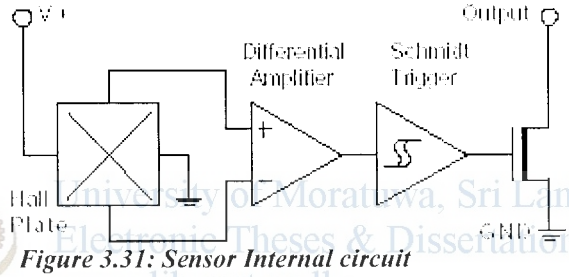


Figure 3.31: Sensor Internal circuit

The hall switch is a normally off device and when a magnetic field comes close to the semi conductor plate electrons and the positive halls are separated into two sides inducing a net cross voltage across the semiconductor material. Direction of this voltage is determined on which pole (south or north) is brought close to the hall element. In our particular sensor, manufacturer has specified to use the south pole of the magnet.

Since this small voltage is not sufficient to drive a considerable current, it is amplified by a differential amplifier. This voltage gives a triggering for a switch like a BJT or an IGBT device, hence with suitable external circuit configurations this phenomenon can be used to obtain a signal for a microcontroller or any other controlling application. There are two types of functions; linear sensors and digital sensors. In digital sensors, a Schmitt trigger has been employed to obtain a pulse type signal where as in digital appliances needed.

Following are oscilloscope images showing the digital hall sensor output pulses at two speeds, each one pulse represents one rotation. First diagram shows the waveform when motor runs at 170 rpm and second image represents about a 60 rpm speed.

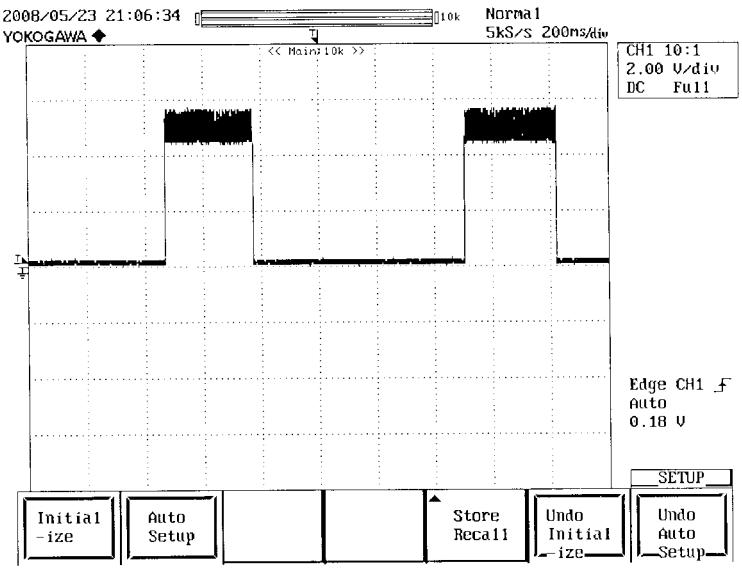


Figure 3.32: Sensor pulse waveform

- One problem faced is that when a magnet field is not present sensor shows a high voltage state, and when a magnet field is present close to the sensor it shows the low voltage state simply because this is the transistor Emitter to Collector voltage.

- A considerable voltage difference develops across the external resistor, but that cannot be sensed in the microcontroller at once because voltages at both ends are floating; therefore either side cannot be connected to the ground pin.

- So the solution found by using an external NOT gate to invert the V_{CE}. This signal was directly fed to the microcontroller. The result is displayed in the LCD and the value is updated continuously with the operation.

3.4.3 Sensor Mounting

Hall sensor with connections to the OOPic microcontroller is permanently mounted on the stator and in an additional rotor the magnet is fixed as shown in the *Figure 3.33*

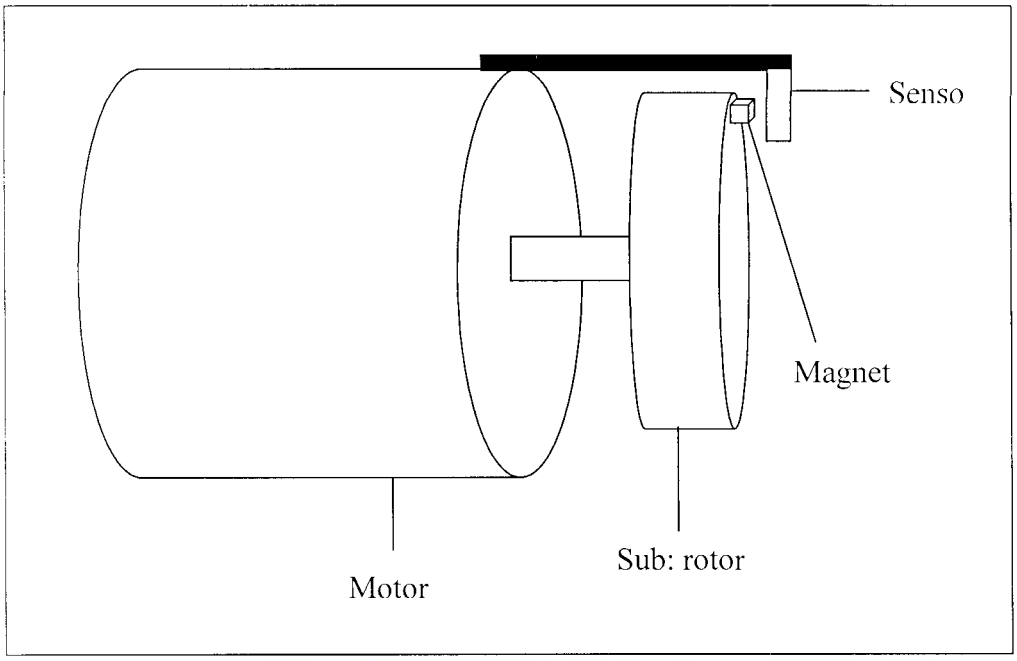


Figure 3.33: Sensor mounting on the motor

Many sensing applications will need high quality magnets to optimize air gaps and provide stable fields over wide temperature ranges. A magnet must have sufficient flux density to generate the desired linear sensor output, at the working air gap required by the application. Other considerations are the temperature coefficient of the magnet and its coercive force. Coercive force is basically the measure of a magnet's ability to retain its magnetic force when subjected to a strong demagnetizing field. The larger a magnet's coercive force, the less susceptible it is to being demagnetized.

Considering ease of application and testing done with the sensor we decided to use a cylindrical shaped Iron-Chromium magnet.

3.4.4 Speed Display

When the magnet comes close to the sensor a pulse signal is given to the OOPic. Then it calculates the speed in rpm's based on the time in-between two consecutive pulses. The frequency is the inversion of the time period.

An LCD was selected to display the speed of the motor. The speed is continuously displayed in the LCD unit, as explained earlier. A 16x1 LCD with 74780 chipset compatible was selected for this purpose. An object called oLCD in ooPIC is used to configure and communicate with the LCD after connecting with suitable input and output terminals in the OOPic hardware as shown in *Figure 3.34*.

Pin	Symbol	Level	Function
1	Vss	--	GND (0V)
2	Vcc	--	Supply Voltage for Logic (+5V)
3	Vo	--	LCD Driving Voltage
4	RS	H/L	H : Data L : Instruction Code
5	R/W	H/L	H : Read L : Write
6	E	H,H->L	Enable Signal
7	DB0	H/L	Data Bus Line
8	DB1	H/L	
9	DB2	H/L	
10	DB3	H/L	
11	DB4	H/L	
12	DB5	H/L	
13	DB6	H/L	
14	DB7	H/L	
15	LEDA	--	LED Power Supply
16	LEDK	--	

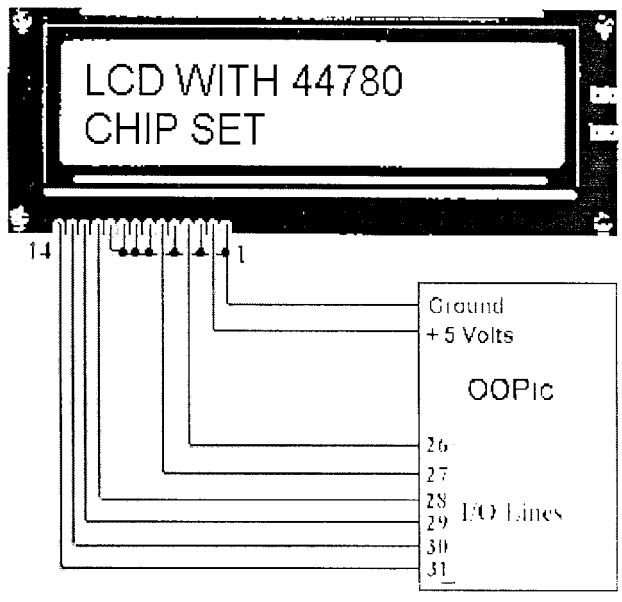


Figure 3.34: 44780 chipset LCD pin diagram and OOPic connections

4 System Details

4.1 Test panel or the User Interface

User interface is designed as a panel where students can easily carry out practical. Panel includes items such as potentiometer, selection switch, Start / Stop switch and Forward / Reverse switch. Panel was designed to assure maximum safety for the users.

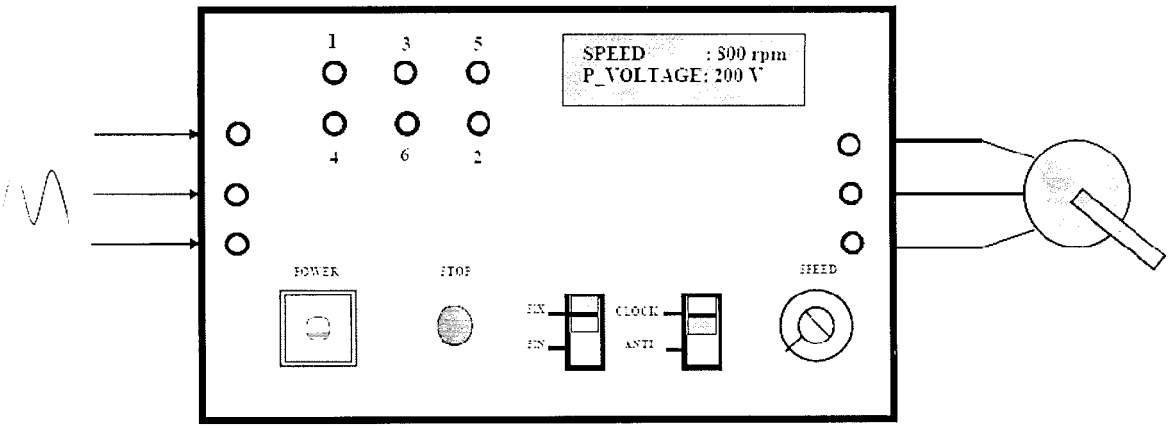


Figure 4.01: User Interface

Features of the system interface panel

- Power on / off button
- Red button to brake the motor instantly
- Selection buttons to select waveform type (six step, Sinusoidal) and rotation (clockwise and anticlockwise)
- Potentiometer to adjust the speed
- LCD panel to display the speed
- Six Test points to observe the driver circuit output waveforms
- Panel is open able to see the inside hardware connections and to communicate with the microcontrollers

4.2 Cost estimation

Cost estimation of the Induction motor Project				
Module	Component	Price	Number	Cost
Controllers	ooPIC module	10038	1	10039
	PIC16F767 IC	1500	1	1500
	Pic PCB	850	1	850
	Pic programmer	800	1	800
Inverter	Capacitors (450V, 390μF)	350	2	700
	Base circuit	150	1	150
Gate Driver Circuit	IR 21094	950	3	2850
	500mA, 18V Transformer	275	1	275
	50V Rectifier	50	1	50
	Optocoupler	250	3	750
	Regulators	50	3	150
	Printed Circuit Board	850	1	850
Sensor	Hall sensor	300	2	600
Liquid Crystal Display	16×1 LCD	750	2	1500
	Connecting Tape wires	150	1	150
Power supply	500mA, 18V Transformer	275	1	275
	LM78xx Regulators	50	3	150
	Dot board	90	1	90
	Capacitors			20
	50V Rectifier	50	1	50
	Power Pack	550	1	550
Housing	Wood (Mahogani)	200		200
	Test points	2	8	16
	AC terminals and Banana clips	20	8	160
Miscellaneous	Stickers			150
	Plastic board			285
	Circuit wires			160
	Lead wires			80
	Soldering Iron	150	1	150
	Bread board	250	1	250
	Dot board	120	3	360
Total Project Cost				24160

5. Conclusions

This project mainly focused on developing a programmable induction motor drive as a test bench where different types of algorithms can be used to control the speed of an induction motor. Basically the system can be divided into subsystem as control unit, IGBT driver circuit unit and Converter & Inverter unit. The important task was to combine these subsystems into one system where these subsystems are completely different types. That means, the control circuit is dealing with DC 5V system and the Converter & Inverter system is dealing with AC 500V. In between these two, there is driver circuit which will isolate the microcontroller circuit from the high voltage side. Also the driver circuit will add a dead band between high & low side signals.

By involving in this project, I was able to find some practical issues which are not seen in theory. For optical isolation, we can use many types of optocouplers, but we found there is an issue of selecting one with proper rise and fall time. By using different models, it has been found that the 6N135 type optocoupler are very much suitable for this purpose, where it has very small rise time & fall time.

Another issue was found regarding the selection of proper driver IC. Earlier, IR2110 was used where an external circuit was needed to produce the dead band and to invert the signals. But it was found IR21094 IC has these features inbuilt with sharp rising & falling edges.

It was decided in the start to use OOpic microcontroller for producing all control signals. But when we deal with that, it was found it is not suitable for applications with very high time precision requirements. Also only 2 PWM modules were inbuilt there, where we needed 3 to produce three phase sinusoidal waveform. Only six step algorithm, speed detection and user interfacing was implemented using this as a result. So the ooPIC is not a suitable choice for the application of controlling 3 phase induction motor.

Many challenges were faced while carrying on the project. The major issues and challenges I faced and how I overcome those are included in this report. In addition, all the problems I faced were good lessons for me and the hands on experience with various components helped a lot in improving my practical knowledge in these areas.

Annexture

A. Code in ooPIC for speed sensing & displaying

```
Dim A As New oCycleTimeL
Dim B As New oDIO8
Dim C As New oDIO1
Dim freq As New oWord
Dim speed As New oWord
Dim disFreq As oLCD

Sub Main()
  A.IOLine = 1
  A.Operate = cvTrue
  B.IOGroup = 1
  B.Direction = cvOutput
  C.IOLine = 23
  C.Direction = cvOutput
  Call DisplayFrequency ()
End Sub

Sub DisplayFrequency ()
          disFreq.Init
          disFreq.Clear
          disFreq As oLCD(3,1,27,26,cvOn)
  Do
    B.State = A.Duration
    C.State = A.Duration.NonZero
    freq=(283/(256-Duration))*1000
    speed= 60*freq/1000
          disFreq.Locate(1,1)
          disFreq.VString = "Output Frequency:"
          disFreq.VString = Str$(freq) + "Hz"
  Loop

End Sub
```

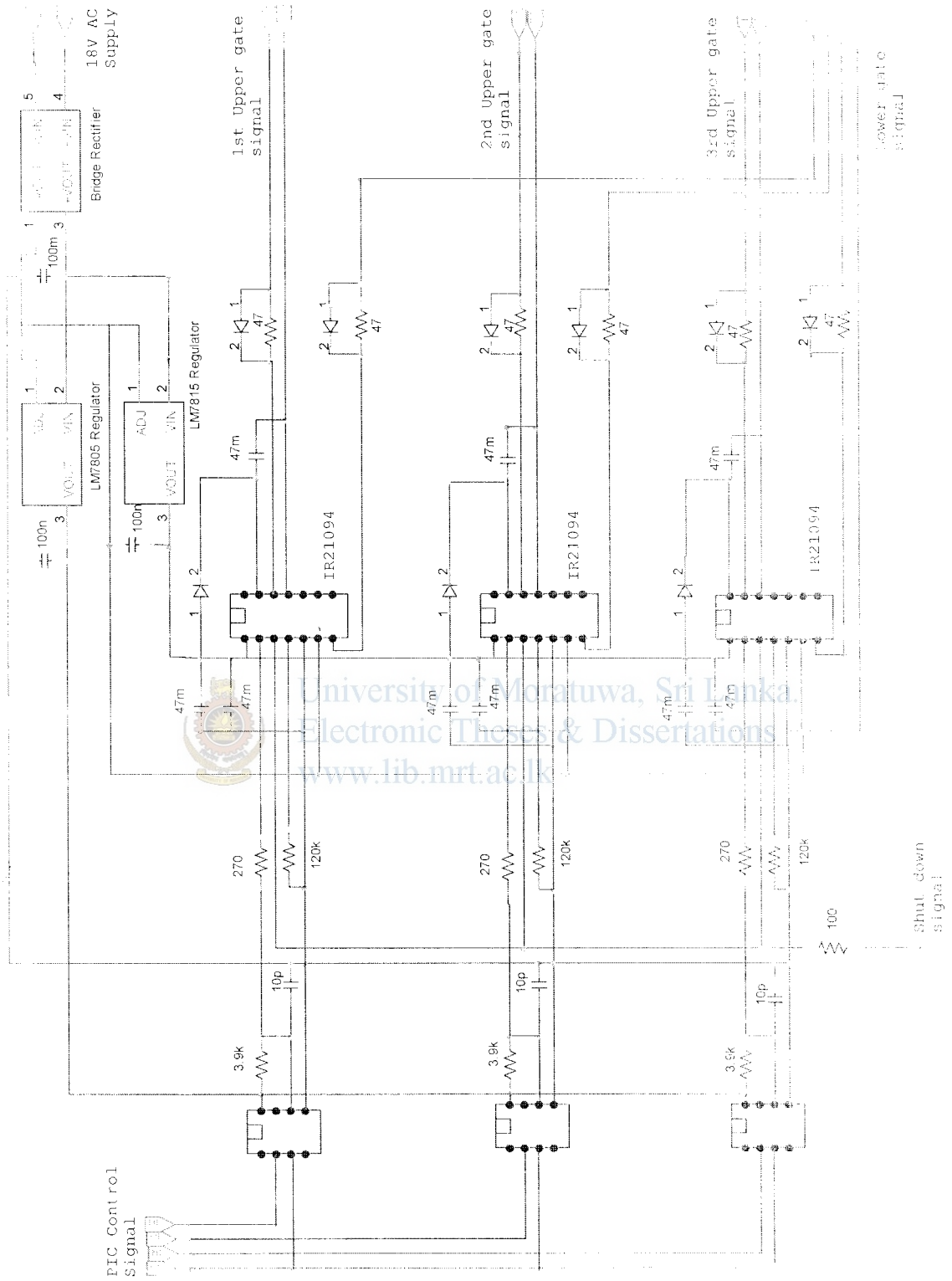
B. MikroC Code for Sinusoidal PWM generation

```
#include <built in.h>

unsigned char sine_table[19] = {0x00, 0x01, 0x07, 0x11, 0x1D, 0x2D,
0x3F, 0x53, 0x69, 0x7F, 0x95, 0xAB, 0xBF, 0xD1, 0xE1, 0xED, 0xF7,
0xFD, 0xFF};
unsigned char
TEMP_LOC, TEMP_LOC_1, TEMP_LOC_2, FREQ_REF_H, FREQ_REF_L,
duty, table_offset1, table_offset2, table_offset3, OFFSET1_FLAG,
OFFSET2_FLAG, OFFSET3_FLAG;
unsigned char
MOTOR_RUNNING = 0, MOTOR_DIRECTION = 0, TIMER1_OV_FLAG = 0,
CHANGE_FREQ = 0;
const unsigned char TIMER1_PRESCALE = 16;
const unsigned long int INSTRUCTION_CYCLE = 5000000;
unsigned long int FREQ_SCALE = (INSTRUCTION_CYCLE/
36)/(TIMER1_PRESCALE/4);

unsigned int SET_FREQ, NEW_FREQ, FREQ_TEMP, TIMER1_VALUE;

void AD_CONV_COMPLETE();
void init();
void SET_ADC_GO();
void UPDATE_PWM_DUTYCYCLES();
void UPDATE_TABLE_OFFSET();
void INIT_MOTOR_PARAMETERS();
void TIMER1_OVERFLOW ();
void CALCULATE_FREQUENCY();
void CONVERT_FREQUENCY();
void BYPASS();

void main(){

  INIT();
  INIT_MOTOR_PARAMETERS();

  while(1){
    if (TIMER1_OV_FLAG != 1) BYPASS();
    else {
      TIMER1_OV_FLAG = 0;
      UPDATE_PWM_DUTYCYCLES();
      UPDATE_TABLE_OFFSET();
      BYPASS();
    }
  }
}

void init() {

  INTCON = 0x00;
  T1CON  = 0x31;
  PCON   = 0x03;
  PIR1   = 0x00;
  PIE1   = 0x00;
  ADCON1 = 0x8C;
  TRISA  = 0x07;

  PIE1.TMR1IE = 1;              // enable Timer1 interrupt
  PIE1.ADIE   = 1;
  INTCON.RBIE = 1;
```

```
    INTCON.PEIE = 1;
    INTCON.GIE  = 1;
}

void BYPASS() {
     SET_ADC_GO();              //START AD CONVERSION

     KEY_CHECK();
}

void interrupt() {
    if (PIR1.ADIF != 0) AD_CONV_COMPLETE();
    if (PIR1.TMR1IF != 0) TIMER1_OVERFLOW();
}

void AD_CONV_COMPLETE(){
     PIR1.ADIF = 0;
     NEW_FREQ = Adc_Read(0);
}

void TIMER1_OVERFLOW (){
    TMR1H = FREQ_REF_H;
    TMR1L = FREQ_REF_L;
    TIMER1_OV_FLAG = 1;
    PIR1.TMR1IF = 0;
}

void INIT_MOTOR_PARAMETERS () {
     TABLE_OFFSET1 = 0x09;
     TABLE_OFFSET2 = 0x03;
     TABLE_OFFSET3 = 0x0F;

     OFFSET1_FLAG = 1;
     OFFSET2_FLAG = 0;
     OFFSET3_FLAG = 0;

     FREQ_REF_H = 0xF9;
     TMR1H = FREQ_REF_H;

     FREQ_REF_L = 0x37;
     TMR1L = FREQ_REF_L;

     TMR0 = 0xB1;
     TIMER1_OV_FLAG = 1;

     PWM1_Init(20000);                      // Set PWM

     PWM2_Init(20000);
     PWM3_Init(20000);

     Pwm1_Start();

     Pwm2_Start();
     Pwm3_Start();
}

void SET_ADC_GO() {
    if (MOTOR_RUNNING != 1) return;
    else {
         if (ADCON0.GO = 1) return;
         CONVERT_FREQUENCY();
```

```
}

CONVERT_FREQUENCY() {
  if (NEW_FREQ != SET_FREQ) {
    CHANGE_FREQ = 1;
    SET_FREQ = NEW_FREQ;
    CALCULATE_FREQUENCY ();
  }


CALCULATE_FREQUENCY () {
FREQ_TEMP = FREQ_SCALE /SET_FREQ;
TIMER1_VALUE = 0xFFFF - FREQ_TEMP;

FREQ_REF_L = Lo(TIMER1_VALUE);
FREQ_REF_H = Hi(TIMER1_VALUE);


UPDATE_PWM_DUTYCYCLES(){

 TEMP_LOC = SET_FREQ * sine_table[table_offset1];
 TEMP_LOC_1 = SET_FREQ * sine_table[table_offset2];
 TEMP_LOC_2 = SET_FREQ * sine_table[table_offset3];

 PWM1_Change_Duty(TEMP_LOC);

 PWM2_Change_Duty(TEMP_LOC_1);

 PWM3_Change_Duty(TEMP_LOC_2);


UPDATE_TABLE_OFFSET(){
 if (OFFSET1_FLAG == 1) {
    if((TABLE_OFFSET1 - 18) < 0 ) TABLE_OFFSET1 ++;
    else OFFSET1_FLAG = 0;
 }
 else {
    TABLE_OFFSET1--;
    if(TABLE_OFFSET1 == 0) OFFSET1_FLAG = 1;
 }

 if (OFFSET2_FLAG == 1) {
    if((TABLE_OFFSET2 - 18) < 0 ) TABLE_OFFSET2 ++;
    else OFFSET2_FLAG = 0;
 }
 else {
    TABLE_OFFSET2--;
    if(TABLE_OFFSET2 == 0) OFFSET2_FLAG = 1;
 }

 if (OFFSET3_FLAG == 1) {
    if((TABLE_OFFSET3 - 18) < 0 ) TABLE_OFFSET3 ++;
    else OFFSET3_FLAG = 0;
 }
 else {
    TABLE_OFFSET3--;
    if(TABLE_OFFSET3 == 0) OFFSET3_FLAG = 1;
 }
```

C. Complete three phase Driver Circuit Diagram



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Email: lahomaw@aol.com and wgd@ece.ubc.ca

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Dept. of Electrical Engineering, University of Moratuwa, Moratuwa, Sri Lanka
Email: nisalO2gelect.mrt.ac.1k, Email: roshan82ggmail.com, erangaldsgyahoo.com, athulaO2gelect.mrt.ac.lk

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University of Bologna, 2 Viale Risogimento, 40136 Bologna, Italia

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Henrik Mosskull, Johann Galic and Bo Wahlberg
Bombardier Transportation, SE-721 73 Västerås, Sweden
S3- Automatic Control, KTH, SE-100 44 Stockholm, Sweden

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D. Wilson
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K.K. Mohapatra, K. Gopakumar, M.R. Baiju, Balarama V. Murty

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Marian P. Kazmierkowski
Institute of Control and Industrial Electronics
Warsaw University of Technology

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Ralph Kennel, Senior Member IEEE, Arne Linder

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Wuppertal University
D – 42097 Wuppertal, Germany

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Peter Mutschler
Darmstadt University of Technology
Department of Power Electronics and Drives
Landgraf-Georg-Str. 4
D-64283 Darmstadt

[22]. FUNDAMENTALS OF DSP-BASED CONTROL FOR AC MACHINES
By Finbarr Moynihan,
Embedded Control Systems Group
Volume 34, Number 06, October, 2000
http://www.analog.com/library/analogDialogue/archives/34-06/dsp/DSP.pdf

TOSHIBA PHOTOCOUPLER GaAℓAs IRED & PHOTO IC

6N135, 6N136

DIGITAL LOGIC ISOLATION.

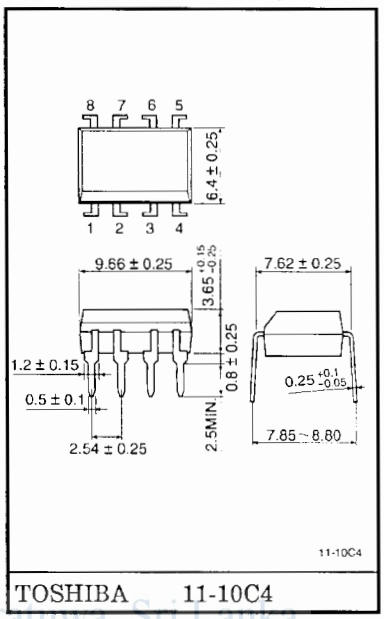
LINE RECEIVER.

POWER SUPPLY CONTROL

SWITCHING POWER SUPPLY

TRANSISTOR INVERTER

Unit in mm



TOSHIBA 11-10C4

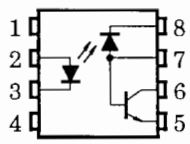
Weight : 0.54g

The TOSHIBA 6N135 and 6N136 consists of a high emitting diode and a one chip photo diode-transistor.

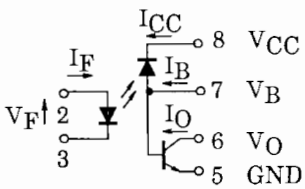
Each unit is 8-lead DIP package.

- Isolation Voltage : 2500V_{rms} (Min.)
- High Speed : t_{pHL}, t_{pLH} = 0.5μs (Typ.) (R_L = 1.9kΩ)
- TTL Compatible
- If Base Pin is Open, Output Signal will be Noisy by Environmental Condition. For This Base, TLP550 is Suitable
- UL Recognized : UL1577, File No. E67349

PIN CONFIGURATIONS



1 : N.C.
2 : ANODE
3 : CATHODE
4 : N.C.
5 : EMITTER
6 : COLLECTOR
7 : BASE, ANODE
8 : CATHODE



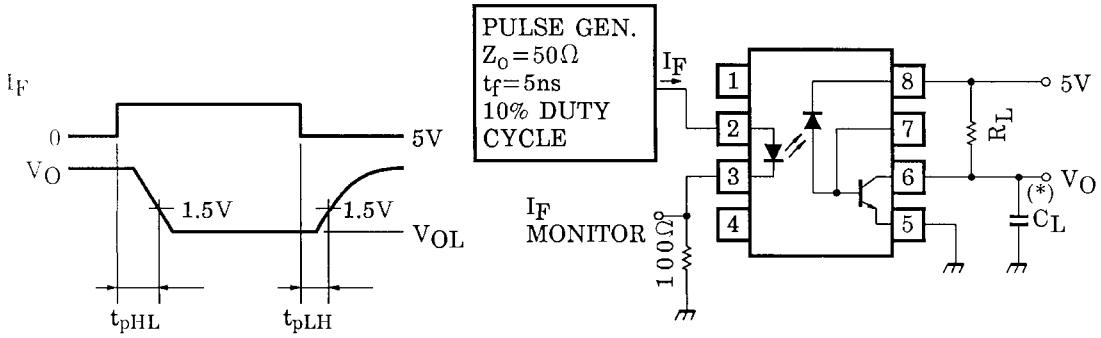
961001EBC2

MAXIMUM RATINGS (Ta = 25°C)

	CHARACTERISTIC		SYMBOL	RATING	UNIT
LED	Forward Current	(Note 1)	I_F	25	mA
	Pulse Forward Current	(Note 2)	I_{FP}	50	mA
	Total Pulse Forward Current	(Note 3)	I_{FPT}	1	A
	Reverse Voltage		V_R	5	V
	Diode Power Dissipation	(Note 4)	P_D	45	mW
DETECTOR	Output Current		I_O	8	mA
	Peak Output Current		I_{OP}	16	mA
	Emitter-Base Reverse Voltage (Pin 5-7)		V_{EB}	5	V
	Supply Voltage		V_{CC}	−0.5~15	V
	Output Voltage		V_O	−0.5~15	V
	Base Current (Pin 7)		I_B	5	mA
	Output Power Dissipation	(Note 5)	P_o	100	mW
Operating Temperature Range			T_{opr}	−55~100	°C
Storage Temperature Range			T_{stg}	−55~125	°C
Lead Solder Temperature (10s)		(Note 6)	T_{sol}	260	°C
Isolation Voltage		(Note 7)	BV_S	2500	V_{rms}

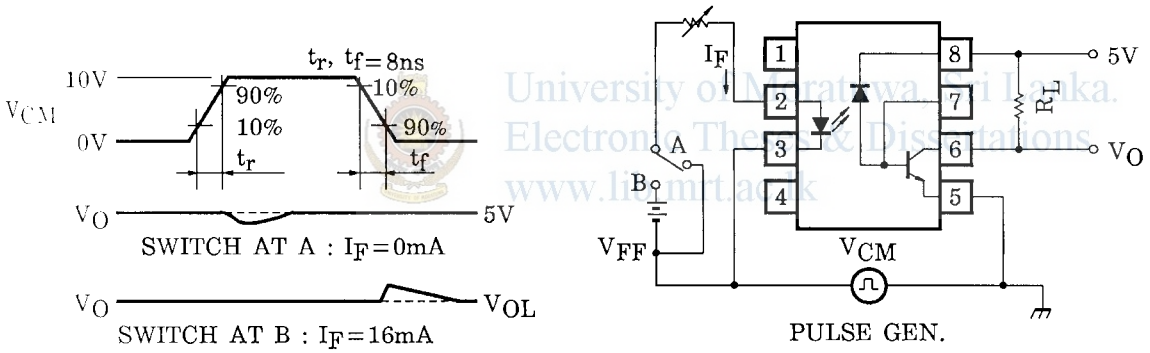
Note 1) Derate 0.8mA above 70°C.
Note 2) 50% duty cycle, 1ms pulse width.
Derate 1.6mA / °C above 70°C.
Note 3) Pulse width 1μs, 300pps.
Note 4) Derate 0.9mW / °C above 70°C.
Note 5) Derate 2mW / °C above 70°C.
Note 6) Soldering portion of lead : up to 2mm from the body of the device.
Note 7) R.H.≦60%, AC / 1min.

TEST CIRCUIT 1.

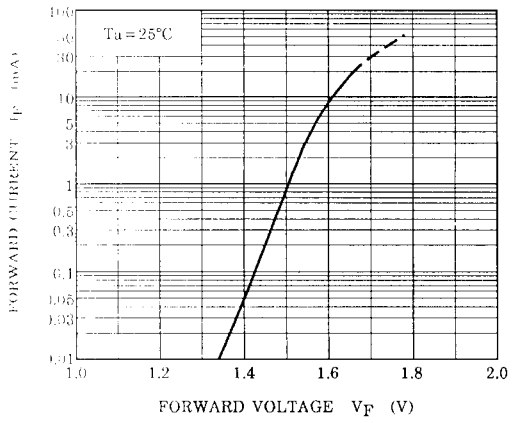


(*) C_L is approximately 15pF which includes probe and stray wiring capacitance.

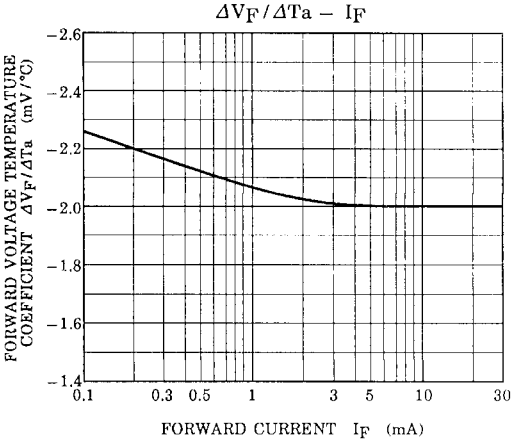
TEST CIRCUIT 2.



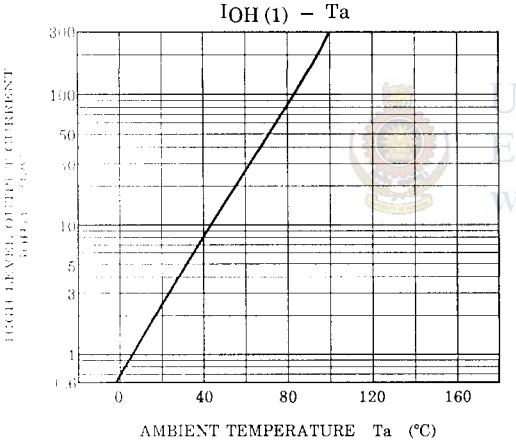
$I_F - V_F$



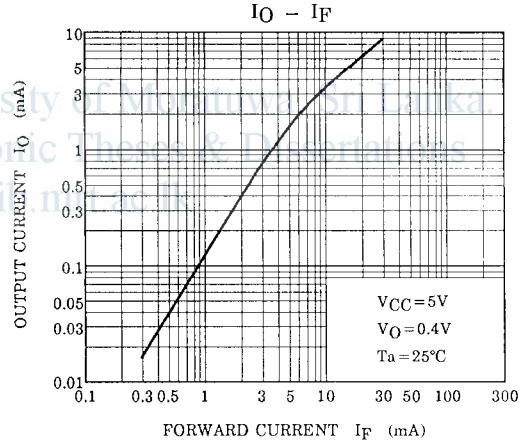
$\Delta V_F / \Delta Ta - I_F$



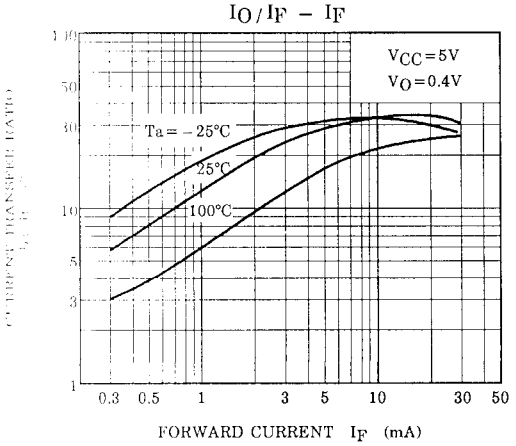
$I_{OH\,(1)} - Ta$



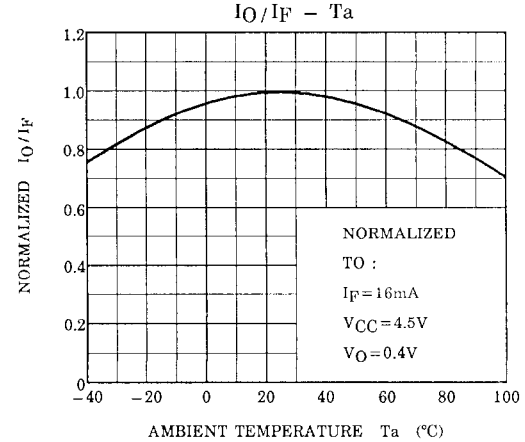
$I_O - I_F$



$I_O / I_F - I_F$



$I_O / I_F - Ta$



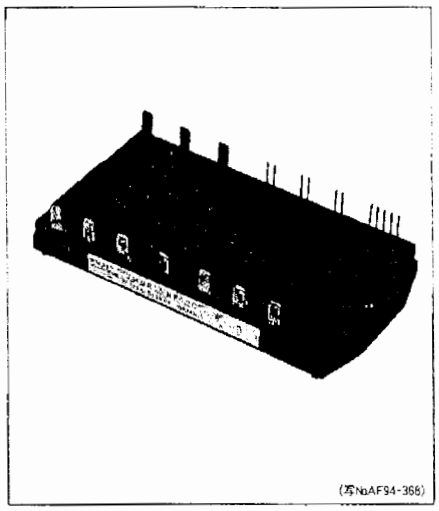
富士半導体ニュープロダクト
Fuji Semiconductor New Products

FUJI ELECTRIC
富士電機

富士IGBTモジュール『Nシリーズ』7MBR15NF120

低損失・高速スイッチング形『Nシリーズ』

1200V/15A/PIM


(弓NbAF94-366)

■特長：Features

- ●高速スイッチング　High Speed Switching
- ●電圧駆動　Voltage Drive
- ●低インダクタンスモジュール構造
  Low Inductance Module Structure
- ●コンバータダイオードブリッジ・ダイナミックブレーキ回路内蔵
  Converter Diode Bridge Dynamic Brake Circuit

■用途：Applications

- ●モータ駆動用インバータ　Inverter for Motor Drive
- ●AC,DCサーボアンプ　AC and DC Servo Drive Amplifier
- ●無停電電源　Uninterruptible Power Supply

■定格と特性：Maximum Ratings and Characteristics

●絶対最大定格：Absolute Maximum Ratings（Tc=25℃）

	Items		Symbols	Condition	Ratings	Units
インバータ部/IGBT INVERTER	コレクタ・エミッタ間電圧		V_{CES}		1200	V
	ゲート・エミッタ間電圧		V_{GES}		±20	V
	コレクタ電流	DC	I_C		15	A
		1ms	I_C pulse		30	
		DC	$-I_C$		15	
	最大損失	One	P_C		120	W
ブレーキ部/IGBT・FWD BRAKE	コレクタ・エミッタ間電圧		V_{CES}		1200	V
	ゲート・エミッタ間電圧		V_{GES}		±20	V
	コレクタ電流	DC	I_C		10	A
		1ms	I_C Pulse		25	A
	最大損失	One	P_C		88	W
	ピーク繰返し逆電圧		V_{RRM}		1200	V
	平均順電流		$I_{F\ (AV)}$		1	A
	サージ電流		I_{FSM}	10ms	50	A
コンバータ部/Diode Converter	ピーク繰返し逆電圧		V_{RRM}		1600	V
	ピーク非繰返し逆電圧		V_{RSM}		1700	V
	平均出力電流		I_O	50/60HZ 正弦波	25	A
	定格サージ電流（非繰返し）		I_{FSM}	T_j=150℃ 10ms	320	A
	定格I^2t（非繰返し）			T_j=150℃ 10ms	512	A^2s
接合部温度			T_j		+150	℃
保存温度			Tstg		−40*1〜+125	℃
絶縁耐圧			V_{ISO}	AC：1min.	AC2500	V
締付けトルク			Mounting*1		1.7	N・m

*1 推奨値：Recommendable value：1.3〜1.7 N・m

●電気的特性：Electrical Characteristics (T_j=25°C)

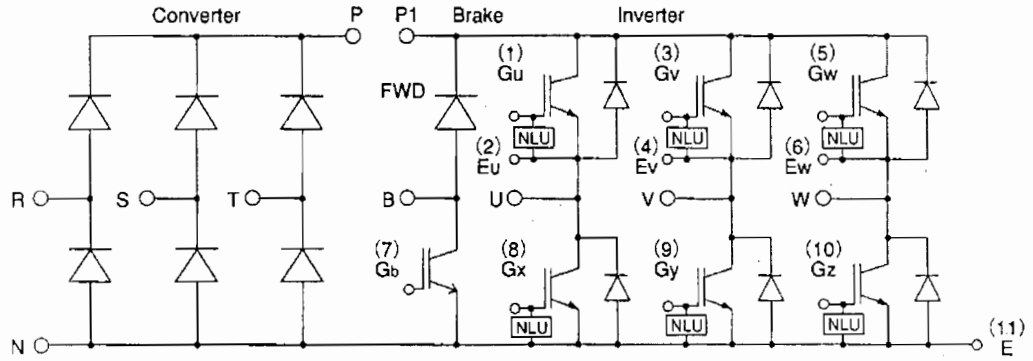
Items		Symbols	Conditions	Characteristics min.	typ.	max.	Units
インバータ部(IGBT) INVERTER	コレクタ・エミッタ間遮断電流	I_{CES}	T_j=25°C, V_{CE}=1200V, V_{GE}=0V			1.0	mA
	ゲート・エミッタ間漏れ電流	I_{GES}	V_{CE}=0V, V_{GE}=±20V			20	μA
	ゲート・エミッタ間しきい値電圧	$V_{GE\ (th)}$	V_{CE}=20V, I_C=15mA	4.5		7.5	V
	コレクタ・エミッタ間飽和電圧	$V_{CE\ (sat)}$	V_{GE}=15V, I_C=15A			3.3	V
	コレクタ・エミッタ間電圧	$-V_{CE}$	$-I_C$=15A			3.0	V
	入力容量	Cies	V_{GE}=0V, V_{CE}=10V, f=1MHz		2400		PF
	スイチッング時間	ton	V_{CC}=600V I_C=15A V_{GE}=±15V R_G=82Ω			1.2	μs
		tr				0.6	
		toff				1.5	
		tf				0.5	
	逆回復時間	trr	I_F=15A, V_{GE}=−10V, −di/dt=50A/μs			350	ns
ブレーキ部 BRAKE (IGBT, FWD)	コレクタ・エミッタ間遮断電流	I_{CES}	V_{CES}=1200V, V_{GE}=0V			1.0	mA
	ゲート・エミッタ間漏れ電流	I_{GES}	V_{CE}=0V, V_{GE}=±20V			100	nA
	コレクタ・エミッタ間飽和電圧	$V_{CE\ (sat)}$	I_C=10A, V_{GE}=15V			3.3	V
	スイッチング時間	ton	V_{CC}=600V I_C=10A V_{GE}=±15V R_G=120Ω			0.8	μs
		tr				0.6	
		toff				1.5	
		tf				0.5	
	逆電流	I_{RRM}	V_R=1200V			1	mA
	逆回復時間	trr				600	ns
コンバータ部 Converter	順電圧	V_{FM}	I_F=25A			1.4	V
	逆電流	I_{RRM}	V_R=1600V			1	mA

●熱的特性：Theramal Characteristics

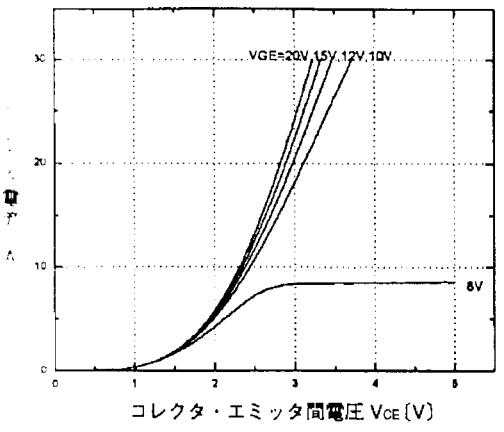
Items	Symbols	Conditions	Characteristics min.	typ.	max.	Units
熱抵抗（1chip）	Rth (j-c)	Inverter IGBT			1.04	℃/W
		Inverter FRD			2.78	
		Brake IGBT			1.04	
		Converter Diode			3.4	
接触熱抵抗（ケース フィン間）※	Rth (c-f)	With Thermal Compound		0.05		

※サーマルコンパウンドを使用して放熱フィン上にモジュールを取り付けた時の接触熱抵抗値
※This is the value which is defined mounting on the additional cooling fin with thermal compound.

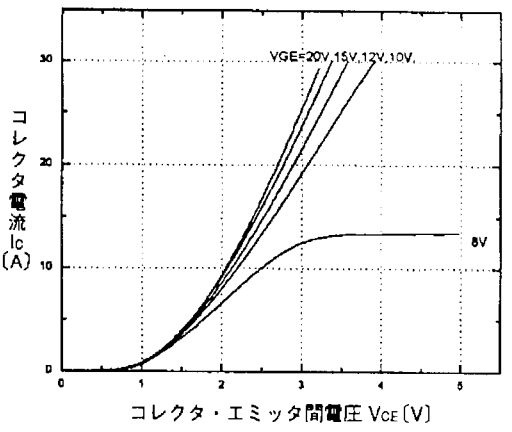
■等価回路：Equivalent Circuit Schematic



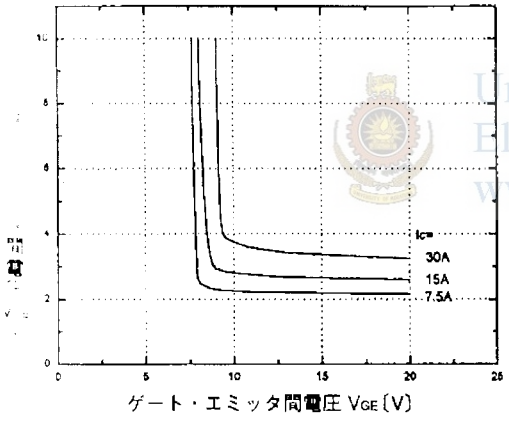
■特性曲線：Characteristics



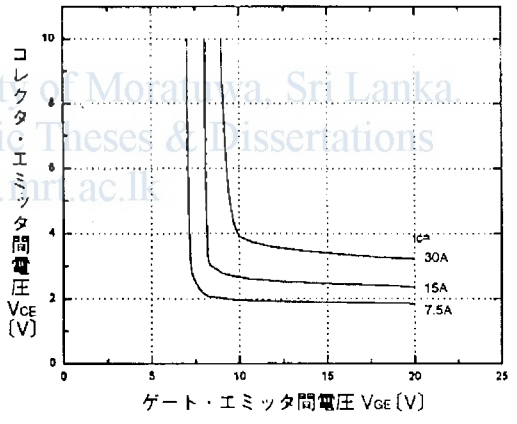
コレクタ電流－コレクタ・エミッタ間電圧特性(T_j＝25°C)〈INV部〉
Collector current vs. Collector-Emitter voltage〈INV〉



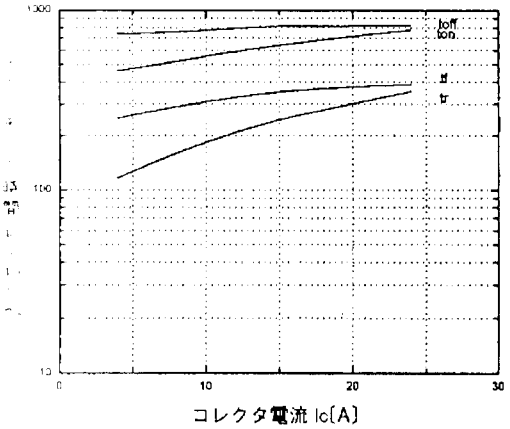
コレクタ電流－コレクタ・エミッタ間電圧特性(T_j＝125°C)〈INV部〉
Collector current vs. Collector-Emitter voltage〈INV〉



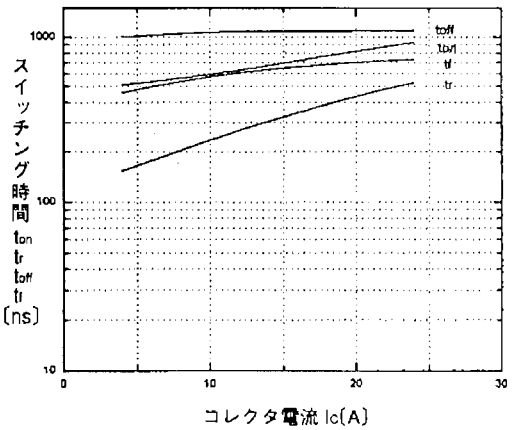
コレクタ・エミッタ間電圧－ゲート・エミッタ間電圧特性(T_j＝25°C)〈INV部〉
Collector-Emitter voltage vs. Gate-Emitter voltage〈INV〉



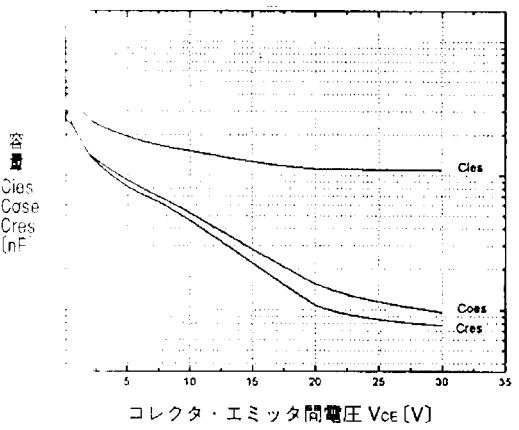
コレクタ・エミッタ間電圧－ゲート・エミッタ間電圧特性(T_j＝125°C)〈INV部〉
Collector-Emitter voltage vs. Gate-Emitter voltage〈INV〉



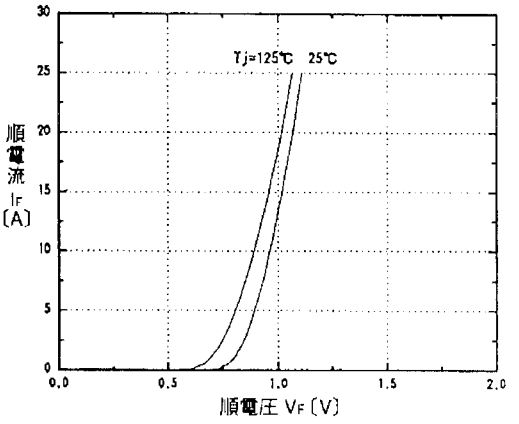
スイッチング時間－コレクタ電流特性(T_j＝25°C)〈INV部〉
Switching time vs. Collector current〈INV〉



スイッチング時間－コレクタ電流特性(T_j＝125°C)〈INV部〉
Switching time vs. Collector current〈INV〉

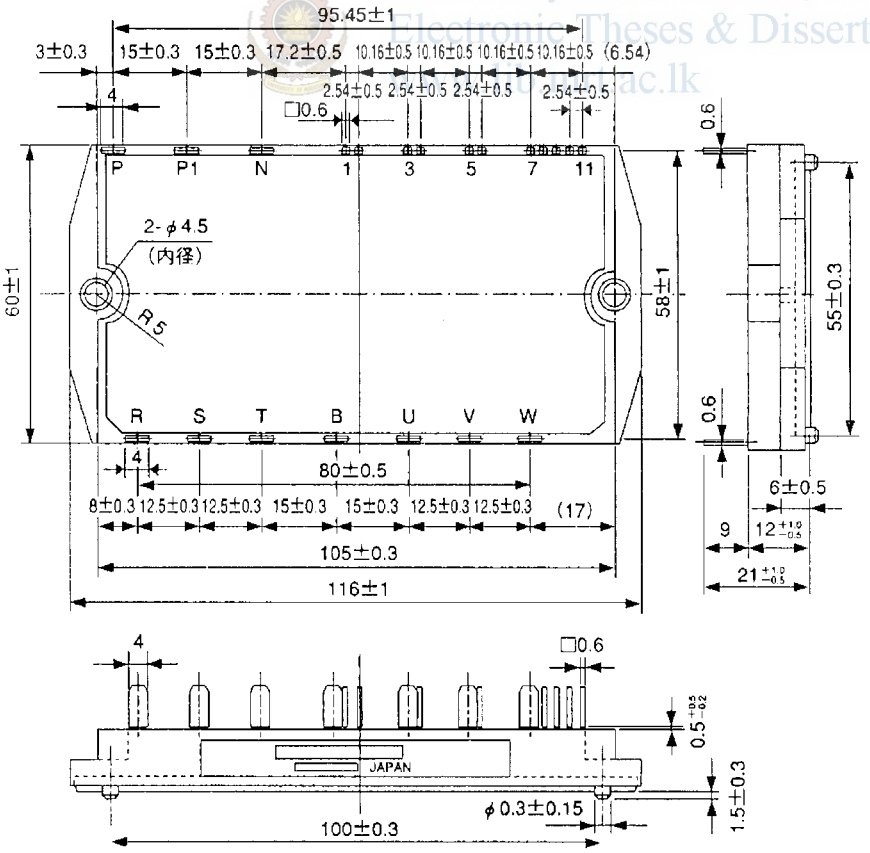


容量－コレクタ・エミッタ間電圧特性(T_j=25°C)〈ブレーキ部〉
Capacitance vs. Collector-Emitter voltage〈BRAKE〉



コンバータ部ダイオード順電圧特性
Converter Diode
Forward current vs. Forward voltage

■外形寸法：Outline Drawings



International
IOR Rectifier

Data Sheet No. PD60162 Rev. V

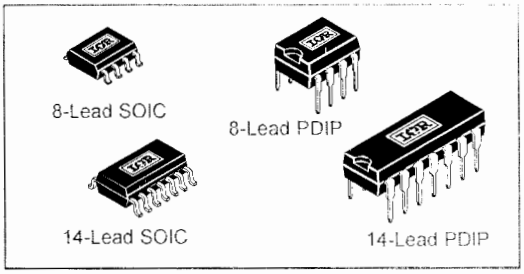
IR2106(4)(S)

HIGH AND LOW SIDE DRIVER

Features

- Floating channel designed for bootstrap operation
  Fully operational to +600V
  Tolerant to negative transient voltage
  dV/dt immune
- Gate drive supply range from 10 to 20V (IR2106(4))
- Undervoltage lockout for both channels
- 3.3V, 5V and 15V input logic compatible
- Matched propagation delay for both channels
- Logic and power ground +/- 5V offset.
- Lower di/dt gate driver for better noise immunity
- Outputs in phase with inputs (IR2106)

Packages



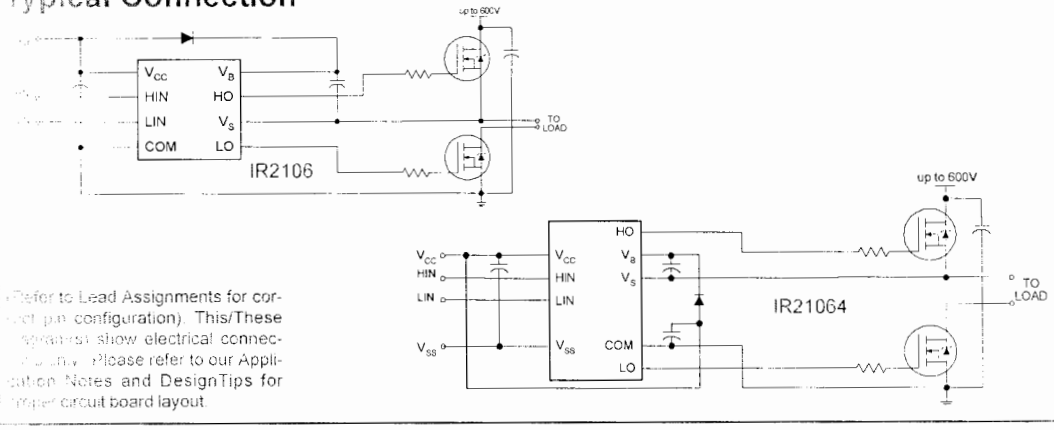
Description

The IR2106(4)(S) are high voltage, high speed power MOSFET and IGBT drivers with independent high and low side referenced output channels. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. The logic input is compatible with standard CMOS or LSTTL output, down to 3.3V logic. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. The floating channel can be used to drive an N-channel power MOSFET or IGBT in the high side configuration which operates up to 600 volts.

2106/2301//2108//2109/2302/2304Feature Comparison

Part	Input logic	Cross-conduction prevention logic	Dead-Time	Ground Pins	Ton/Toff
2106/2301	HIN/LIN	no	none	COM	220/200
21064				VSS/COM	
2108	HIN/$\overline{\text{LIN}}$	yes	Internal 540ns	COM	220/200
21084			Programmable 0.54~5µs	VSS/COM	
2109/2302	$\overline{\text{IN}}$/SD	yes	Internal 540ns	COM	750/200
21094			Programmable 0.54~5µs	VSS/COM	
2304	HIN/LIN	yes	Internal 100ns	COM	160/140

Typical Connection



(Refer to Lead Assignments for correct pin configuration). This/These diagram(s) show electrical connections only. Please refer to our Application Notes and DesignTips for proper circuit board layout.

Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

Symbol	Definition		Min.	Max.	Units
V_B	High side floating absolute voltage		-0.3	625	V
V_S	High side floating supply offset voltage		V_B - 25	V_B + 0.3	
V_{HO}	High side floating output voltage		V_S - 0.3	V_B + 0.3	
V_{CC}	Low side and logic fixed supply voltage		-0.3	25	
V_{LO}	Low side output voltage		-0.3	V_{CC} + 0.3	
V_{IN}	Logic input voltage		V_{SS} - 0.3	V_{CC} + 0.3	
V_{SS}	Logic ground (IR21064 only)		V_{CC} - 25	V_{CC} + 0.3	
dV_S/dt	Allowable offset supply voltage transient		—	50	V/ns
P_D	Package power dissipation @ $T_A \leq +25°C$	(8 lead PDIP)	—	1.0	W
		(8 lead SOIC)	—	0.625	
		(14 lead PDIP)	—	1.6	
		(14 lead SOIC)	—	1.0	
$RthJA$	Thermal resistance, junction to ambient	(8 lead PDIP)	—	125	°C/W
		(8 lead SOIC)	—	200	
		(14 lead PDIP)	—	75	
		(14 lead SOIC)	—	120	
T_J	Junction temperature		—	150	°C
T_S	Storage temperature		-50	150	
T_L	Lead temperature (soldering, 10 seconds)		—	300	

Recommended Operating Conditions

The Input/Output logic timing diagram is shown in figure 1. For proper operation the device should be used within the recommended conditions. The V_S and V_{SS} offset rating are tested with all supplies biased at 15V differential.

Symbol	Definition	Min.	Max.	Units
V_B	High side floating supply absolute voltage IR2106(4)	V_S + 10	V_S + 20	V
V_S	High side floating supply offset voltage	Note 1	600	
V_{HO}	High side floating output voltage	V_S	V_B	
V_{CC}	Low side and logic fixed supply voltage IR2106(4)	10	20	
V_{LO}	Low side output voltage	0	V_{CC}	
V_{IN}	Logic input voltage	V_{SS}	V_{CC}	
V_{SS}	Logic ground (IR21064 only)	-5	5	
T_A	Ambient temperature	-40	125	°C

Note 1: Logic operational for V_S of -5 to +600V. Logic state held for V_S of -5V to $-V_{BS}$. (Please refer to the Design Tip DT97-3 for more details).

Dynamic Electrical Characteristics

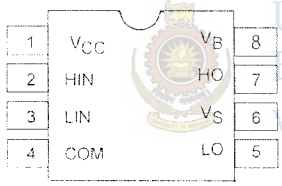
V_{BIAS} (V_{CC}, V_{BS}) = 15V, V_{SS} = COM, C_L = 1000 pF, T_A = 25°C.

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
t_{on}	Turn-on propagation delay	—	220	300	nsec	V_S = 0V
t_{off}	Turn-off propagation delay	—	200	280		V_S = 0V or 600V
MT	Delay matching, HS & LS turn-on/off	—	0	30		
t_r	Turn-on rise time	—	150	220		V_S = 0V
t_f	Turn-off fall time	—	50	80		V_S = 0V

Lead Definitions

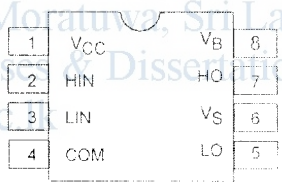
Symbol	Description
HIN	Logic input for high side gate driver output (HO), in phase
LIN	Logic input for low side gate driver output (LO), in phase
VSS	Logic Ground (IR21064 only)
V_B	High side floating supply
HO	High side gate drive output
V_S	High side floating supply return
V_{CC}	Low side and logic fixed supply
LO	Low side gate drive output
COM	Low side return

Lead Assignments



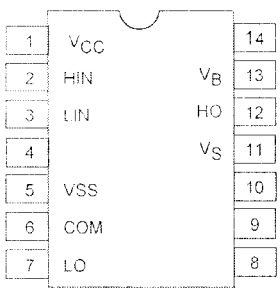
8 Lead PDIP

IR2106



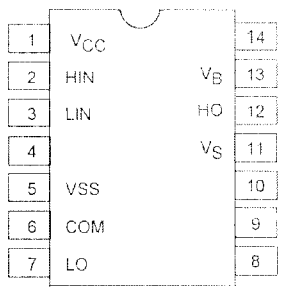
8 Lead SOIC

IR2106S



14 Lead PDIP

IR21064



14 Lead SOIC

IR21064S

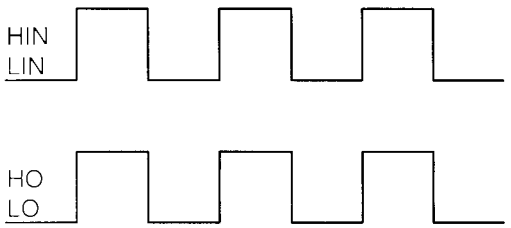


Figure 1. Input/Output Timing Diagram

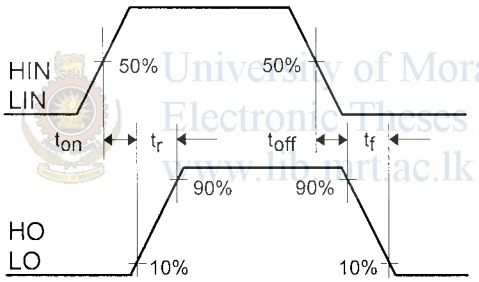


Figure 2. Switching Time Waveform Definitions

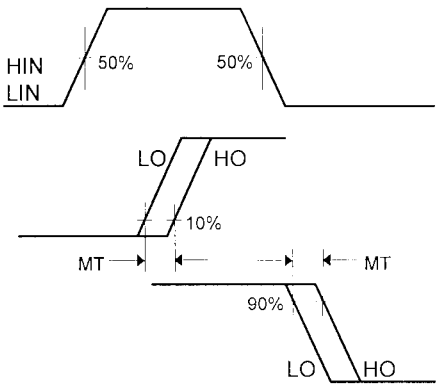
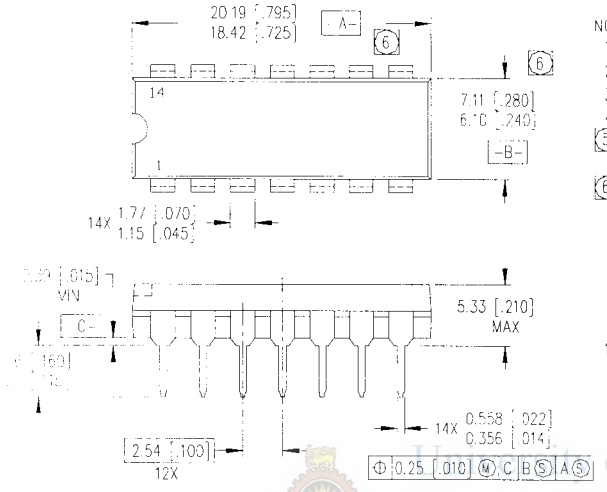
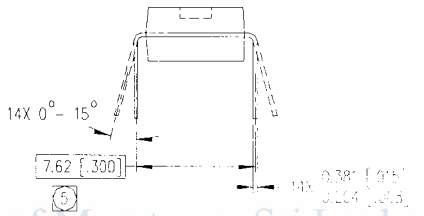


Figure 3. Delay Matching Waveform Definitions

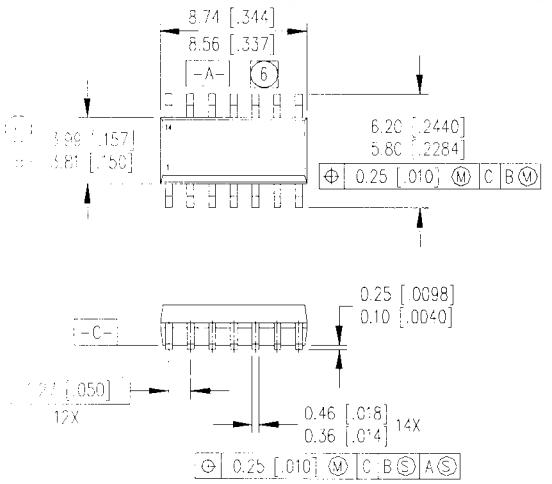


NOTES.
1. DIMENSIONING & TOLERANCING PER ANS Y14.5M-1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-001AC.
5. MEASURED WITH THE LEADS CONSTRAINED TO BE PERPENDICULAR TO DATUM PLANE C.
6. DIMENSION DOES NOT INCLUDE MOLD PROTUSIONS. MOLD PROTUSIONS SHALL NOT EXCEED 0.25 [.010].

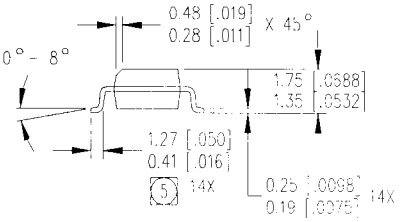


14 Lead PDIP

01-6010
01-3002 03 (MS-001AC)



NOTES:
1. DIMENSIONING & TOLERANCING PER ANS Y14.5M 1982.
2. CONTROLLING DIMENSION: MILLIMETER
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-012AB.
5. DIMENSION IS THE LENGTH OF LEAD FOR SOLDERING TO A SUBSTRATE.
6. DIMENSION DOES NOT INCLUDE MOLD PROTUSIONS. MOLD PROTUSIONS SHALL NOT EXCEED 0.15 [.006].



14 Lead SOIC (narrow body)

01-6019
01-3063 00 (MS-012AB)

PIC16F7X7
Data Sheet

28/40/44-Pin, 8-Bit CMOS Flash Microcontrollers with 10-Bit A/D and nanoWatt Technology

MICROCHIP

PIC16F7X7

28/40/44-Pin, 8-Bit CMOS Flash Microcontrollers with 10-Bit A/D and nanoWatt Technology

Low-Power Features:

- Power-Managed modes:
  - Primary Run (XT, RC oscillator, 76 µA, 1 MHz, 2V)
  - RC_RUN (7 µA, 31.25 kHz, 2V)
  - SEC_RUN (9 µA, 32 kHz, 2V)
  - Sleep (0.1 µA, 2V)
- Timer1 Oscillator (1.8 µA, 32 kHz, 2V)
- Watchdog Timer (0.7 µA, 2V)
- Two-Speed Oscillator Start-up

Oscillators:

- Three Crystal modes:
  - LP, XT, HS (up to 20 MHz)
- Two External RC modes
- One External Clock mode:
  - ECIO (up to 20 MHz)
- Internal Oscillator Block:
  - 8 user-selectable frequencies (31 kHz, 125 kHz, 250 kHz, 500 kHz, 1 MHz, 2 MHz, 4 MHz, 8 MHz)

Analog Features:

- 10-bit, up to 14-channel Analog-to-Digital Converter:
  - Programmable Acquisition Time
  - Conversion available during Sleep mode
- Dual Analog Comparators
- Programmable Low-Current Brown-out Reset (BOR) Circuitry and Programmable Low-Voltage Detect (LVD)

Peripheral Features:

- High Sink/Source Current: 25 mA
- Two 8-bit Timers with Prescaler
- Timer1/RTC module:
  - 16-bit timer/counter with prescaler
  - Can be incremented during Sleep via external 32 kHz watch crystal
- Master Synchronous Serial Port (MSSP) with 3-wire SPI™ and I²C™ (Master and Slave) modes
- Addressable Universal Synchronous Asynchronous Receiver Transmitter (AUSART)
- Three Capture, Compare, PWM modules:
  - Capture is 16-bit, max. resolution is 12.5 ns
  - Compare is 16-bit, max. resolution is 200 ns
  - PWM max. resolution is 10 bits
- Parallel Slave Port (PSP) – 40/44-pin devices only

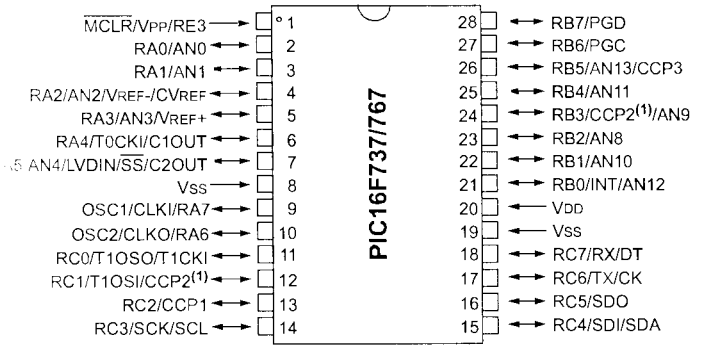
Special Microcontroller Features:

- Fail-Safe Clock Monitor for protecting critical applications against crystal failure
- Two-Speed Start-up mode for immediate code execution
- Power-on Reset (POR), Power-up Timer (PWRT) and Oscillator Start-up Timer (OST)
- Programmable Code Protection
- Processor Read Access to Program Memory
- Power-Saving Sleep mode
- In-Circuit Serial Programming™ (ICSP™) via two pins
- MPLAB® In-Circuit Debug (ICD) via two pins
- $\overline{MCLR}$ pin function replaceable with input only pin

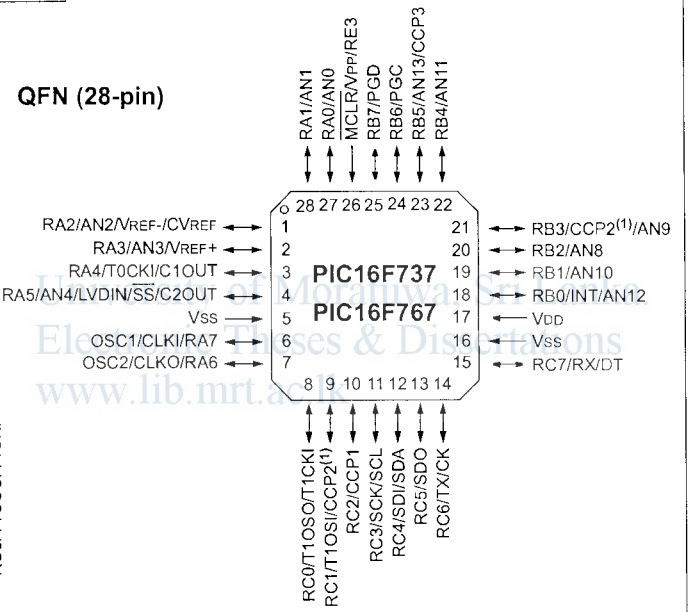
Device	Program Memory (# Single-Word Instructions)	Data SRAM (Bytes)	I/O	Interrupts	10-bit A/D (ch)	Comparators	CCP (PWM)	MSSP		AUSART	Timers 8/16-bit
								SPI™	I²C™ (Master)		
PIC16F737	4096	368	25	16	11	2	3	Yes	Yes	Yes	2/1
PIC16F747	4096	368	36	17	14	2	3	Yes	Yes	Yes	2/1
PIC16F767	8192	368	25	16	11	2	3	Yes	Yes	Yes	2/1
PIC16F777	8192	368	36	17	14	2	3	Yes	Yes	Yes	2/1

Pin Diagrams

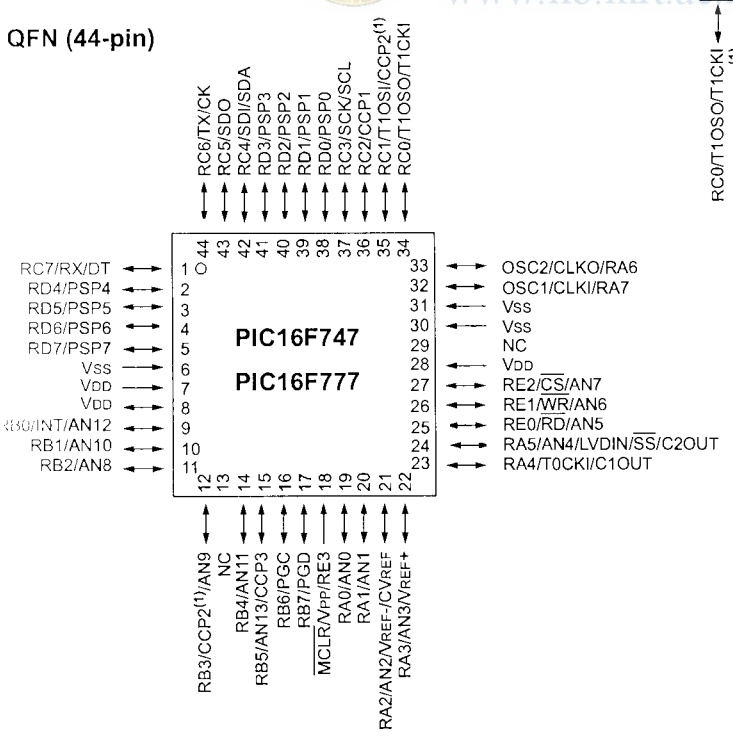
PDIP, SOIC, SSOP (28-pin)



QFN (28-pin)



QFN (44-pin)



Note 1: Pin location of CCP2 is determined by the CCPMX bit in Configuration Word Register 1.

Table of Contents

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To determine if an errata sheet exists for a particular device, please check with one of the following:

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1.0 DEVICE OVERVIEW

This document contains device specific information about the following devices:

- PIC16F737
- PIC16F747
- PIC16F767
- PIC16F777

PIC16F737/767 devices are available only in 28-pin packages, while PIC16F747/777 devices are available in 40-pin and 44-pin packages. All devices in the PIC16F7X7 family share common architecture with the following differences:

- The PIC16F737 and PIC16F767 have one-half of the total on-chip memory of the PIC16F747 and PIC16F777.
- The 28-pin devices have 3 I/O ports, while the 40/44-pin devices have 5.
- The 28-pin devices have 16 interrupts, while the 40/44-pin devices have 17.
- The 28-pin devices have 11 A/D input channels, while the 40/44-pin devices have 14.
- The Parallel Slave Port is implemented only on the 40/44-pin devices.
- Low-Power modes: RC_RUN allows the core and peripherals to be clocked from the INTRC, while SEC_RUN allows the core and peripherals to be clocked from the low-power Timer1. Refer to **Section 4.7 "Power-Managed Modes"** for further details.
- Internal RC oscillator with eight selectable frequencies, including 31.25 kHz, 125 kHz, 250 kHz, 500 kHz, 1 MHz, 2 MHz, 4 MHz and 8 MHz. The INTRC can be configured as a primary or secondary clock source. Refer to **Section 4.5 "Internal Oscillator Block"** for further details.
- The Timer1 module current consumption has been greatly reduced from 20 μA (previous PIC16 devices) to 1.8 μA typical (32 kHz at 2V), which is ideal for real-time clock applications. Refer to **Section 7.0 "Timer1 Module"** for further details.
- Extended Watchdog Timer (WDT) that can have a programmable period from 1 ms to 268s. The WDT has its own 16-bit prescaler. Refer to **Section 15.17 "Watchdog Timer (WDT)"** for further details.
- Two-Speed Start-up: When the oscillator is configured for LP, XT or HS, this feature will clock the device from the INTRC while the oscillator is warming up. This, in turn, will enable almost immediate code execution. Refer to **Section 15.17.3 "Two-Speed Clock Start-up Mode"** for further details.
- Fail-Safe Clock Monitor: This feature will allow the device to continue operation if the primary or secondary clock source fails by switching over to the INTRC.

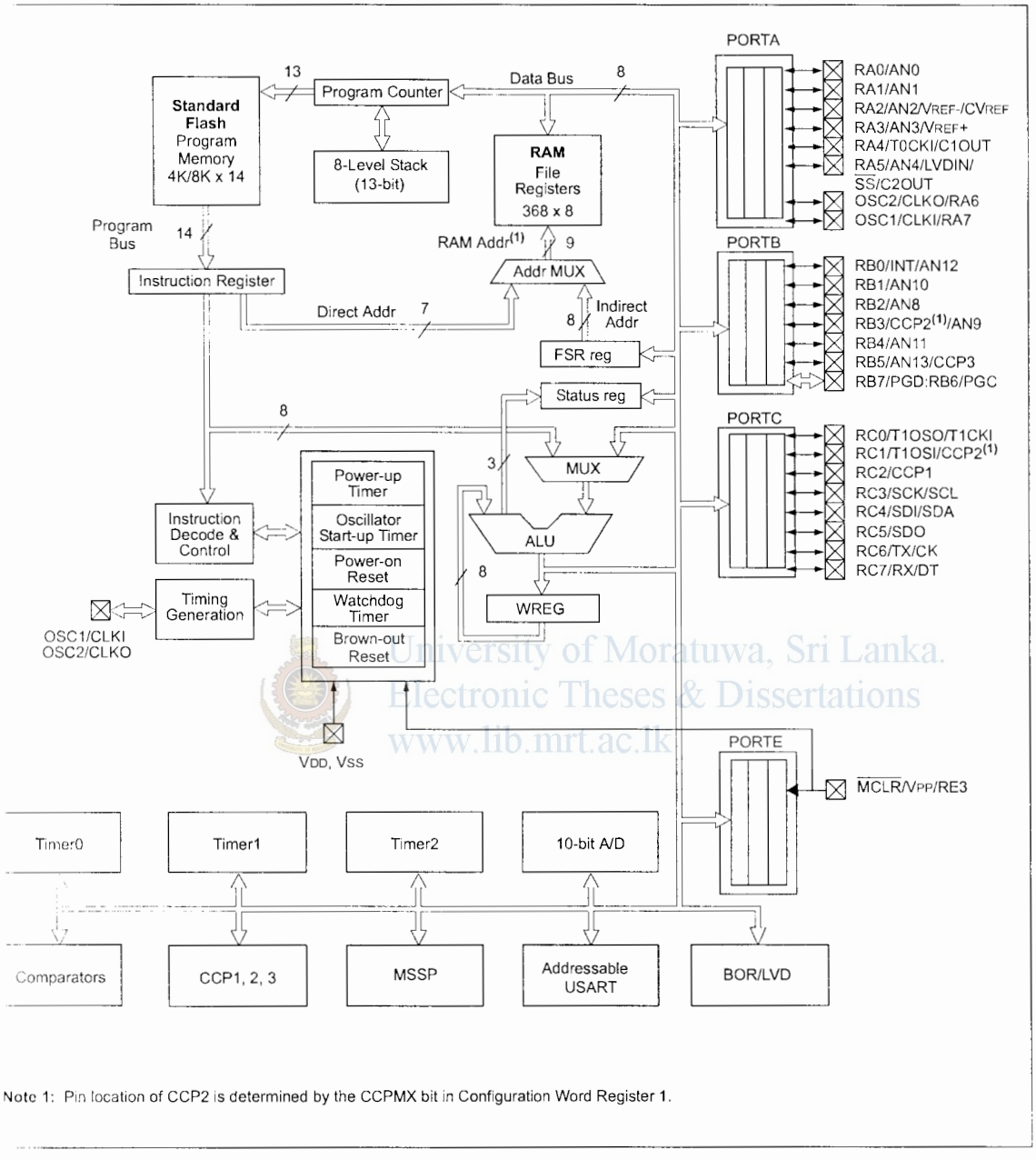
The available features are summarized in Table 1-1. Block diagrams of the PIC16F737/767 and PIC16F747/777 devices are provided in Figure 1-1 and Figure 1-2, respectively. The pinouts for these device families are listed in Table 1-2 and Table 1-3.

Additional information may be found in the *"PICmicro® Mid-Range MCU Family Reference Manual"* (DS33023) which may be obtained from your local Microchip Sales Representative or downloaded from the Microchip web site. The Reference Manual should be considered a complementary document to this data sheet and is highly recommended reading for a better understanding of the device architecture and operation of the peripheral modules.

TABLE 1-1: PIC16F7X7 DEVICE FEATURES

Key Features	PIC16F737	PIC16F747	PIC16F767	PIC16F777
Operating Frequency	DC – 20 MHz	DC – 20 MHz	DC – 20 MHz	DC – 20 MHz
Resets (and Delays)	POR, BOR (PWRT, OST)	POR, BOR (PWRT, OST)	POR, BOR (PWRT, OST)	POR, BOR (PWRT, OST)
Flash Program Memory (14-bit words)	4K	4K	8K	8K
Data Memory (bytes)	368	368	368	368
Interrupts	16	17	16	17
I/O Ports	Ports A, B, C	Ports A, B, C, D, E	Ports A, B, C	Ports A, B, C, D, E
Timers	3	3	3	3
Capture/Compare/PWM Modules	3	3	3	3
Master Serial Communications	MSSP, AUSART	MSSP, AUSART	MSSP, AUSART	MSSP, AUSART
Parallel Communications	—	PSP	—	PSP
10-bit Analog-to-Digital Module	11 Input Channels	14 Input Channels	11 Input Channels	14 Input Channels
Instruction Set	35 Instructions	35 Instructions	35 Instructions	35 Instructions
Packaging	28-pin PDIP 28-pin SOIC 28-pin SSOP 28-pin QFN	40-pin PDIP 44-pin QFN 44-pin TQFP	28-pin PDIP 28-pin SOIC 28-pin SSOP 28-pin QFN	40-pin PDIP 44-pin QFN 44-pin TQFP

FIGURE 1-1: **PIC16F737 AND PIC16F767 BLOCK DIAGRAM**



Note 1: Pin location of CCP2 is determined by the CCPMX bit in Configuration Word Register 1.

TABLE 1-2: PIC16F737 AND PIC16F767 PINOUT DESCRIPTION

Pin Name	PDIP SOIC SSOP Pin #	QFN Pin #	I/O/P Type	Buffer Type	Description
OSC1/CLKI/RA7	9	6		ST/CMOS(3)	Oscillator crystal or external clock input.
OSC1			I		Oscillator crystal input or external clock source input. ST buffer when configured in RC mode; otherwise CMOS.
CLKI			I		External clock source input. Always associated with pin function OSC1 (see OSC1/CLKI, OSC2/CLKO pins).
RA7			I/O	ST	Digital I/O.
OSC2/CLKO/RA6	10	7		—	Oscillator crystal or clock output.
OSC2			O		Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode.
CLKO			O		In RC mode, OSC2 pin outputs CLKO which has 1/4 the frequency of OSC1 and denotes the instruction cycle rate.
RA6			I/O	ST	Digital I/O.
MCLR/VPP/RE3	1	26		ST	Master Clear (input) or programming voltage (output).
MCLR			I		Master Clear (Reset) input. This pin is an active-low Reset to the device.
VPP			P		Programming voltage input.
RE3			I	ST	Digital input only pin.
					PORTA is a bidirectional I/O port.
RA0/AN0	2	27		TTL	
RA0			I/O		Digital I/O.
AN0			I		Analog input 0.
RA1/AN1	3	28		TTL	
RA1			I/O		Digital I/O.
AN1			I		Analog input 1.
RA2/AN2/VREF-/CVREF	4	1		TTL	
RA2			I/O		Digital I/O.
AN2			I		Analog input 2.
VREF-			I		A/D reference voltage input (low).
CVREF			O		Comparator voltage reference output.
RA3/AN3/VREF+	5	2		TTL	
RA3			I/O		Digital I/O.
AN3			I		Analog input 3.
VREF+			I		A/D reference voltage input (high).
RA4/T0CKI/C1OUT	6	3		ST	
RA4			I/O		Digital I/O – Open-drain when configured as output.
T0CKI			I		Timer0 external clock input.
C1OUT			O		Comparator 1 output bit.
RA5/AN4/LVDIN/SS/C2OUT	7	4		TTL	
RA5			I/O		Digital I/O.
AN4			I		Analog input 4.
LVDIN			I/O		Low-Voltage Detect input.
SS			I		SPI™ slave select input.
C2OUT			O		Comparator 2 output bit.

Legend: I = input O = output I/O = input/output P = power
— = Not used TTL = TTL input ST = Schmitt Trigger input

Note 1: This buffer is a Schmitt Trigger input when configured as the external interrupt.
2: This buffer is a Schmitt Trigger input when used in Serial Programming mode.
3: This buffer is a Schmitt Trigger input when configured in RC Oscillator mode and a CMOS input otherwise.
4: Pin location of CCP2 is determined by the CCPMX bit in Configuration Word Register 1.

TABLE 1-2: **PIC16F737 AND PIC16F767 PINOUT DESCRIPTION (CONTINUED)**

Pin Name	PDIP SOIC SSOP Pin #	QFN Pin #	I/O/P Type	Buffer Type	Description
					PORTB is a bidirectional I/O port. PORTB can be software programmed for internal weak pull-up on all inputs.
RB0/INT/AN12	21	18		TTL/ST(1)	
RB0			I/O		Digital I/O.
INT			I		External interrupt.
AN12			I		Analog input channel 12.
RB1/AN10	22	19		TTL	
RB1			I/O		Digital I/O.
AN10			I		Analog input channel 10.
RB2/AN8	23	20		TTL	
RB2			I/O		Digital I/O.
AN8			I		Analog input channel 8.
RB3/CCP2/AN9	24	21		TTL	
RB3			I/O		Digital I/O.
CCP2(4)			I/O		CCP2 capture input, compare output, PWM output.
AN9			I		Analog input channel 9.
RB4/AN11	25	22		TTL	
RB4			I/O		Digital I/O.
AN11			I		Analog input channel 11.
RB5/AN13/CCP3	26	23		TTL	
RB5			I/O		Digital I/O.
AN13			I		Analog input channel 13.
CCP3			I/O		CCP3 capture input, compare output, PWM output.
RB6/PGC	27	24		TTL/ST(2)	
RB6			I/O		Digital I/O.
PGC			I/O		In-Circuit Debugger and ICSP™ programming clock.
RB7/PGD	28	25		TTL/ST(2)	
RB7			I/O		Digital I/O.
PGD			I/O		In-Circuit Debugger and ICSP programming data.

Legend: I = input O = output I/O = input/output P = power
— = Not used TTL = TTL input ST = Schmitt Trigger input

Note 1: This buffer is a Schmitt Trigger input when configured as the external interrupt.
2: This buffer is a Schmitt Trigger input when used in Serial Programming mode.
3: This buffer is a Schmitt Trigger input when configured in RC Oscillator mode and a CMOS input otherwise.
4: Pin location of CCP2 is determined by the CCPMX bit in Configuration Word Register 1.

TABLE 1-2: PIC16F737 AND PIC16F767 PINOUT DESCRIPTION (CONTINUED)

Pin Name	PDIP SOIC SSOP Pin #	QFN Pin #	I/O/P Type	Buffer Type	Description
					PORTC is a bidirectional I/O port.
T1OSO/T1CKI	11	8		ST	
RC0			I/O		Digital I/O.
T1OSO			O		Timer1 oscillator output.
T1CKI			I		Timer1 external clock input.
T1OSI/CCP2	12	9		ST	
RC1			I/O		Digital I/O.
T1OSI			I		Timer1 oscillator input.
CCP2(4)			I/O		Capture2 input, Compare2 output, PWM2 output.
CCP1	13	10		ST	
RC2			I/O		Digital I/O.
CCP1			I/O		Capture1 input, Compare1 output, PWM1 output.
SCK/SCL	14	11		ST	
RC3			I/O		Digital I/O.
SCK			I/O		Synchronous serial clock input/output for SPI™ mode.
SCL			I/O		Synchronous serial clock input/output for I^2C™ mode.
SDI/SDA	15	12		ST	
RC4			I/O		Digital I/O.
SDI			I		SPI data in.
SDA			I/O		I^2C data I/O.
/SDO	16	13		ST	
RC5			I/O		Digital I/O.
SDO			O		SPI data out.
/TX/CK	17	14		ST	
RC6			I/O		Digital I/O.
TX			O		AUSART asynchronous transmit.
CK			I/O		AUSART synchronous clock.
/RX/DT	18	15		ST	
RC7			I/O		Digital I/O.
RX			I		AUSART asynchronous receive.
DT			I/O		AUSART synchronous data.
	8, 19	5, 16	P	—	Ground reference for logic and I/O pins.
	20	17	P	—	Positive supply for logic and I/O pins.

Legend: I = input O = output I/O = input/output P = power
— = Not used TTL = TTL input ST = Schmitt Trigger input

Note 1: This buffer is a Schmitt Trigger input when configured as the external interrupt.
2: This buffer is a Schmitt Trigger input when used in Serial Programming mode.
3: This buffer is a Schmitt Trigger input when configured in RC Oscillator mode and a CMOS input otherwise.
4: Pin location of CCP2 is determined by the CCPMX bit in Configuration Word Register 1.

2.0 MEMORY ORGANIZATION

There are two memory blocks in each of these PICmicro® MCUs. The program memory and data memory have separate buses so that concurrent access can occur and is detailed in this section. The program memory can be read internally by user code (see **Section 3.0 "Reading Program Memory"**).

Additional information on device memory may be found in the *"PICmicro® Mid-Range MCU Family Reference Manual"* (DS33023).

2.1 Program Memory Organization

The PIC16F7X7 devices have a 13-bit program counter capable of addressing an 8K word x 14-bit program memory space. The PIC16F767/777 devices have 4K words of Flash program memory and the PIC16F737/747 devices have 4K words. The program memory maps for PIC16F7X7 devices are shown in Figure 2-1. Accessing a location above the physically implemented address will cause a wraparound.

The Reset vector is at 0000h and the interrupt vector is at 0004h.

2.2 Data Memory Organization

The data memory is partitioned into multiple banks which contain the General Purpose Registers and the Special Function Registers. Bits RP1 (Status<6>) and RP0 (Status<5>) are the bank select bits:

RP1:RP0	Bank
00	0
01	1
10	2
11	3

Each bank extends up to 7Fh (128 bytes). The lower locations of each bank are reserved for the Special Function Registers. Above the Special Function Registers are General Purpose Registers, implemented as static RAM. All implemented banks contain Special Function Registers. Some frequently used Special Function Registers from one bank may be mirrored in another bank for code reduction and quicker access.

2.2.1 GENERAL PURPOSE REGISTER FILE

The register file (shown in Figure 2-2 and Figure 2-3) can be accessed either directly, or indirectly, through the File Select Register (FSR).

FIGURE 2-1: PROGRAM MEMORY MAPS AND STACKS FOR PIC16F7X7 DEVICES

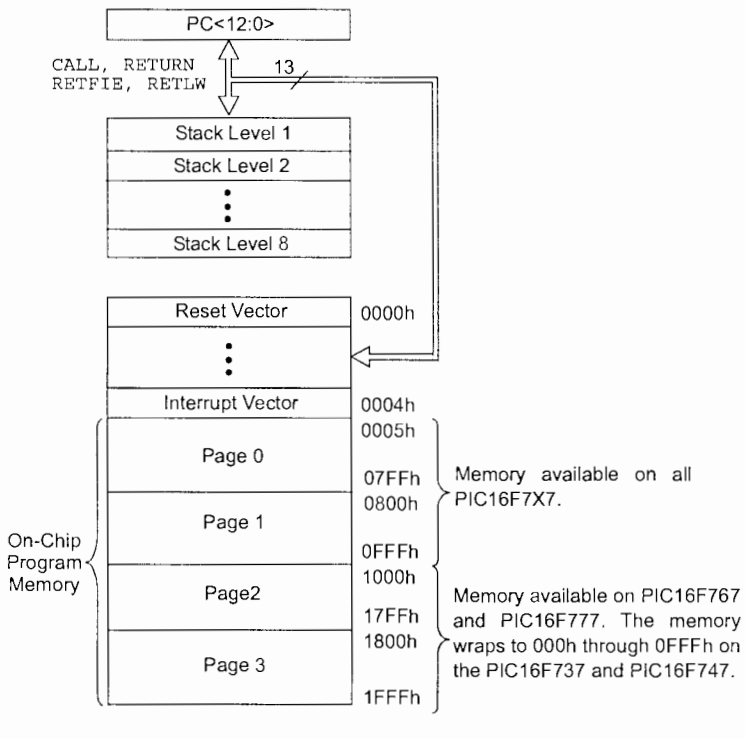
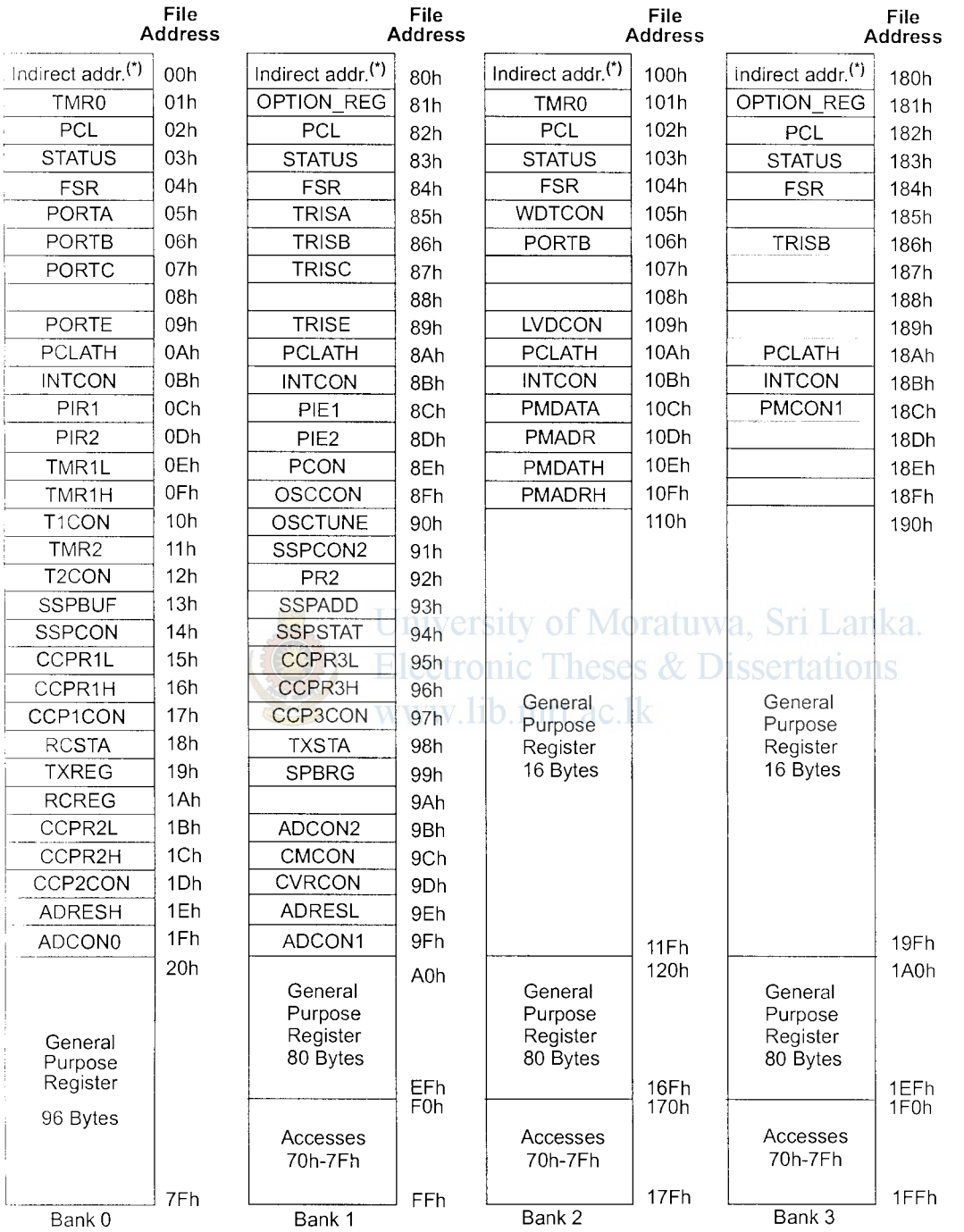


FIGURE 2-2: **DATA MEMORY MAP FOR PIC16F737 AND THE PIC16F767**



☐ Unimplemented data memory locations read as '0'.
* Not a physical register.

2.2.2 SPECIAL FUNCTION REGISTERS

The Special Function Registers are registers used by the CPU and peripheral modules for controlling the desired operation of the device. These registers are implemented as static RAM. A list of these registers is given in Table 2-1.

The Special Function Registers can be classified into two sets: core (CPU) and peripheral. Those registers associated with the core functions are described in detail in this section. Those related to the operation of the peripheral features are described in detail in the peripheral feature section.

TABLE 2-1: SPECIAL FUNCTION REGISTER SUMMARY

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Details on page
Bank 0											
00h(4)	INDF	Addressing this location uses contents of FSR to address data memory (not a physical register)								0000 0000	30, 180
01h	TMR0	Timer0 Module Register								xxxx xxxx	76, 180
02h(4)	PCL	Program Counter (PC) Least Significant Byte								0000 0000	29, 180
03h(4)	STATUS	IRP	RP1	RP0	$\overline{TO}$	$\overline{PD}$	Z	DC	C	0001 1xxx	21, 180
04h(4)	FSR	Indirect Data Memory Address Pointer								xxxx xxxx	30, 180
05h	PORTA	PORTA Data Latch when written: PORTA pins when read								xx0x 0000	55, 180
06h	PORTB	PORTB Data Latch when written: PORTB pins when read								xx00 0000	64, 180
07h	PORTC	PORTC Data Latch when written: PORTC pins when read								xxxx xxxx	66, 180
08h(5)	PORTD	PORTD Data Latch when written: PORTD pins when read								xxxx xxxx	67, 180
09h(5)	PORTE	—	—	—	—	RE3	RE2	RE1	RE0	---- x000	68, 180
0Ah(1,4)	PCLATH	—	—	—	Write Buffer for the upper 5 bits of the Program Counter					---0 0000	29, 180
0Bh(4)	INTCON	GIE	PEIE	TMR0IE	INT0IE	RBIE	TMR0IF	INT0IF	RBIF	0000 000x	23, 180
0Ch	PIR1	PSPIF(3)	ADIF	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	0000 0000	25, 180
0Dh	PIR2	OSFIF	CMIF	LVDIF	—	BCLIF	—	CCP3IF	CCP2IF	000- 0-00	27, 180
0Eh	TMR1L	Holding Register for the Least Significant Byte of the 16-bit TMR1 Register								xxxx xxxx	83, 180
0Fh	TMR1H	Holding Register for the Most Significant Byte of the 16-bit TMR1 Register								xxxx xxxx	83, 180
10h	T1CON	—	T1RUN	T1CKPS1	T1CKPS0	T1OSCEN	$\overline{T1SYNC}$	TMR1CS	TMR1ON	-000 0000	83, 180
11h	TMR2	Timer2 Module Register								0000 0000	86, 180
12h	T2CON	—	TOUTPS3	TOUTPS2	TOUTPS1	TOUTPS0	TMR2ON	T2CKPS1	T2CKPS0	-000 0000	86, 180
13h	SSPBUF	Synchronous Serial Port Receive Buffer/Transmit Register								xxxx xxxx	101, 180
14h	SSPCON	WCOL	SSPOV	SSPEN	CKP	SSPM3	SSPM2	SSPM1	SSPM0	0000 0000	101, 180
15h	CCPR1L	Capture/Compare/PWM Register 1 (LSB)								xxxx xxxx	90, 180
16h	CCPR1H	Capture/Compare/PWM Register 1 (MSB)								xxxx xxxx	90, 180
17h	CCP1CON	—	—	CCP1X	CCP1Y	CCP1M3	CCP1M2	CCP1M1	CCP1M0	--00 0000	88, 180
18h	RCSTA	SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D	0000 000x	134, 180
19h	TXREG	AUSART Transmit Data Register								0000 0000	139, 180
1Ah	RCREG	AUSART Receive Data Register								0000 0000	141, 180
1Bh	CCPR2L	Capture/Compare/PWM Register 2 (LSB)								xxxx xxxx	92, 180
1Ch	CCPR2H	Capture/Compare/PWM Register 2 (MSB)								xxxx xxxx	92, 180
1Dh	CCP2CON	—	—	CCP2X	CCP2Y	CCP2M3	CCP2M2	CCP2M1	CCP2M0	--00 0000	88, 180
1Eh	ADRESH	A/D Result Register High Byte								xxxx xxxx	160, 180
1Fh	ADCON0	ADCS1	ADCS0	CHS2	CHS1	CHS0	GO/$\overline{DONE}$	CHS3	ADON	0000 0000	152, 180

Legend: x = unknown, u = unchanged, q = value depends on condition, — = unimplemented, read as '0', r = reserved. Shaded locations are unimplemented, read as '0'.

Note 1: The upper byte of the program counter is not directly accessible. PCLATH is a holding register for the PC<12:8> bits, whose contents are transferred to the upper byte of the program counter during branches (CALL or GOTO).

2: Other (non Power-up) Resets include external Reset through $\overline{MCLR}$ and Watchdog Timer Reset.

3: Bits PSPIE and PSPIF are reserved on the 28-pin devices; always maintain these bits clear.

4: These registers can be addressed from any bank.

5: PORTD, PORTE, TRISD and TRISE are not physically implemented on the 28-pin devices (except for RE3), read as '0'.

6: This bit always reads as a '1'.

7: OSCCON<OSTS> bit resets to '0' with dual-speed start-up and LP, HS or HS-PLL selected as the oscillator.

8: RE3 is an input only. The state of the TRISE3 bit has no effect and will always read '1'.

TABLE 2-1: SPECIAL FUNCTION REGISTER SUMMARY (CONTINUED)

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Details on page
Bank 1											
80h(4)	INDF	Addressing this location uses contents of FSR to address data memory (not a physical register)								0000 0000	30, 180
81h	OPTION_REG	$\overline{RBPU}$	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0	1111 1111	22, 180
82h(4)	PCL	Program Counter's (PC) Least Significant Byte								0000 0000	29, 180
83h(4)	STATUS	IRP	RP1	RP0	$\overline{TO}$	$\overline{PD}$	Z	DC	C	0001 1xxx	21, 180
84h(4)	FSR	Indirect Data Memory Address Pointer								xxxx xxxx	30, 180
85h	TRISA	PORTA Data Direction Register								1111 1111	55, 181
86h	TRISB	PORTB Data Direction Register								1111 1111	64, 181
87h	TRISC	PORTC Data Direction Register								1111 1111	66, 181
88h(5)	TRISD	PORTD Data Direction Register								1111 1111	67, 181
89h(5)	TRISE	IBF(5)	OBF(5)	IBOV(5)	PSPMODE(5)	—(8)	PORTE Data Direction bits			0000 1111	69, 181
8Ah(1,4)	PCLATH	—	—	—	Write Buffer for the upper 5 bits of the Program Counter					---0 0000	23, 180
8Bh(4)	INTCON	GIE	PEIE	TMR0IE	INT0IE	RBIE	TMR0IF	INT0IF	RBIF	0000 000x	25, 180
8Ch	PIE1	PSPIE(3)	ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	0000 0000	24, 181
8Dh	PIE2	OSFIE	CMIE	LVDIE	—	BCLIE	—	CCP3IE	CCP2IE	000- 0-00	26, 181
8Eh	PCON	—	—	—	—	—	SBOREN	$\overline{POR}$	$\overline{BOR}$	---- -1qq	28, 181
8Fh	OSCCON	—	IRCF2	IRCF1	IRCF0	OSTS(7)	IOFS	SCS1	SCS0	-000 1000	38, 181
90h	OSCTUNE	—	—	TUN5	TUN4	TUN3	TUN2	TUN1	TUN0	--00 0000	36, 181
91h	SSPCON2	GCEN	ACKSTAT	ACKDT	ACKEN	RCEN	PEN	RSEN	SEN	0000 0000	105
92h	PR2	Timer2 Period Register								1111 1111	86, 181
93h	SSPADD	Synchronous Serial Port (I^2C™ mode) Address Register								0000 0000	101, 181
94h	SSPSTAT	SMP	CKE	D/$\overline{A}$	P	S	R/$\overline{W}$	UA	BF	0000 0000	101, 181
95h	CCPR3L	Capture/Compare/PWM Register 3 (LSB)								xxxx xxxx	92
96h	CCPR3H	Capture/Compare/PWM Register 3 (MSB)								xxxx xxxx	92
97h	CCP3CON	—	—	CCP3X	CCP3Y	CCP3M3	CCP3M2	CCP3M1	CCP3M0	--00 0000	92
98h	TXSTA	CSRC	TX9	TXEN	SYNC	—	BRGH	TRMT	TX9D	0000 -010	145, 181
99h	SPBRG	Baud Rate Generator Register								0000 0000	145, 181
9Ah	—	Unimplemented								—	—
9Bh	ADCON2	—	—	ACQT2	ACQT1	ACQT0	—	—	—	--00 0---	154
9Ch	CMCON	C2OUT	C1OUT	C2INV	C1INV	CIS	CM2	CM1	CM0	0000 0111	55, 161
9Dh	CVRCON	CVREN	CVROE	CVRR	—	CVR3	CVR2	CVR1	CVR0	000- 0000	55, 167
9Eh	ADRESL	A/D Result Register Low Byte								xxxx xxxx	180
9Fh	ADCON1	ADFM	ADCS2	VCFG1	VCFG0	PCFG3	PCFG2	PCFG1	PCFG0	0000 0000	153, 181

Legend: x = unknown, u = unchanged, q = value depends on condition, — = unimplemented, read as '0', r = reserved. Shaded locations are unimplemented, read as '0'.

Note 1: The upper byte of the program counter is not directly accessible. PCLATH is a holding register for the PC<12:8> bits, whose contents are transferred to the upper byte of the program counter during branches (CALL or GOTO).

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3: Bits PSPIE and PSPIF are reserved on the 28-pin devices; always maintain these bits clear.

4: These registers can be addressed from any bank.

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