DESIGN OF CONTROL PHILOSOPHY BETWEEN TRANSFORMER AVR CONTROL AND BSC BANK PFCONTROL

A dissertation submitted to the
Department of Electrical Engineering, University of Moratuwa
in partial fulfilment of the requirements for the
Degree of Master of Science

by
DICKMADU GODAGE SUMITH KUMARA

Supervised by: 1. Dr. J.P. Karunadasa
2. Eng. Mr. K.P. Kusum Shanthi

Department of Electrical Engineering
University of Moratuwa, Sri Lanka

2009

Abstract

Ceylon Electricity Board (CEB) controls major roll in Generation, Transmission and Distribution of the electrical power in the island. It has hydro-power capacity about 950MW and thermal power capacity725 MW. The average VAR consumption a day is 650 MVAR. Average power factor of the operation of the system is about 0.95. Almost 80% of the distribution of electrical power is done by CEB. The transmission network totally owned operated by CEB. The CEB transmission system consists of 220k V and 132kV network. It has 44 Grid Substation which convert 132kV/33kV for the distribution of the power to low voltage consumers. In this Grid Substation there is 109 132kV/33kV power transformer each having capacity of 31.5 MVA.

There are Breaker switch capacitors (BSC) bank installed at some places of these GSS. The total installed capacity of the shunt BSC bank is amount to 320MV AR and yet another 70MV AR planning to connect in the near future. In these GSS there are two systems to control 33kV bus voltage at reference 33kV level. One system varies the transformer tap position by controlling 33kV voltage. We called this as On-Load Tap Control of the transformer. For this to be done there is controller (AVR) which sends the command to OLTC to take appropriate action of increasing or decreasing the tap. On the other hand there is a BSC bank which allowed controlling the reactive power of the GSS.

The main intentions of the use of capacitor banks is to give voltage support at the substation level, reduction of losses in power transformers and transmission lines, and to release the capacity constraints in transformers and lines. CEB uses power factor regulation for switching these capacitor banks for above purposes but no studies have been done to evaluate its suitability with transformer AVR.

Even though these two controllers try to maintain VAR and Voltage (Q&V) of the GSS they are operating independently. Because of that We could not achieved maximum effect of these two system i:e., under optimization of the Voltage and Var.

Some time we have observed that these two controllers are hunting with each other by doing the controlling.

If we could coordinate these two controllers to make proper function we indirectly could save the number of tap operations of the transformer and that will help reducing costly maintenance of the OLTC. My main intention is to coordinate these two controllers to achieve above objects. I further try to develop a new system to take care of the both functions in one unit. I have used PSCAD software program for simulation of the GSS.

For the real time data collection I used two data loggers which are property of the CEB. Finally I have found that for controlling the both controllers we need a additional parameter which High Voltage side voltage measurement which could be easily available at the GSS without any additional cost. Taking this new parameter with existing parameters I have develop a control philosophy which coordinates both the transformer AVR controller and BSC bank controller by optimizing voltage and Var. flow through the system.

DECLARATION

The work submitted in this dissertation is the result of my own investigation, except where otherwise stated.

It has not already been accepted for any degree, and is also not being concurrently submitted for any other degree.

UOM Verified Signature

D.G.S.Kumara

28th November 2009

We/I endorse the declaration by the candidate.

UOM Verified Signature

Dr.J.P. Karunadasa.

15th December 2009

UOM Verified Signature

Eng.Mr.K.P. Kusum Santhi

15th December 2009

Contents

Declaration	i
Abstract	iv
Acknowledgement	v
List of Figures	vi,vii
List of Tables	viii

Chapters

1. Introduction	**1**
1.1 Background	1
1.2 Objectives	1
1.3 Scope of the work	2
1.4 Present problems in AVR and PF control Transmission GSS	3
2. Automatic Voltage Control (AVR) of transformers in GSS	**4**
2.1 Power transformer and On Load Tap Changer (OLTC)	4
2.2 OLT control principle for paralleling transformers in the GSS	4
2.2.1 Operations of the Master – Follower method	5
2.2.2 Operation of the minimum circulation method	5
2.3 Controlling philosophy	7
2.4 Setting of the parameters of the AVR in CEB	7
2.5 Internal hardware structure of the TF's AVR and how it operates	8
3. Methods used for controlling the capacitor bank in GSS	**11**
3.1 Shunt Capacitors	11
3.2 Different types of capacitor banks	12
3.3 Capacitor bank controlling philosophy	13
3.3.1 Temperature control	13
3.3.2 Time control	13
3.3.3 Current control	14
3.3.4 Power factor control	14
3.3.5 VAR Control	15
3.3.6 Voltage control	15
3.4 Description of the existing controller in the Galle GSS	16
4. Case study for Galle Grid Substation	**19**
4.1 Substation technical details	19
4.2 Collection of the system data and measurements	19
4.3 Measuring devices and data loggers	20
4.4 Variation in the power factor in the GSS	21
4.5 Switching patter n of the capacitor banks in the GSS	22
4.6 Uncompensated reactive power	23
4.7 Summery of the system study	26

5. System modeling and simulations **27**
5.1 Software selection for modeling 27
5.2 Components in the substation modeling 28
5.3 Running the simulation 30
5.3.1 Theoretical aspect of the simulation study 30
5.3.2 Transformer var consumption 31

5.4 Data recording and graphs 34

6. Design of new controller for BSC bank controlling **37**
6.1. Introduction of the design 37
6.2. Factors that have been considered for designing the controller 38
6.3. Brief description of the drawings and figures 39
6.4. Detailed description of the design 39
6.5 Sample calculation of the decision variables 44
6.6. Factors that can be included in the design for further improvements 50
6.6.1 VAR controlling of the BSC bank 50
6.6.2. Voltage controlling of the BSC bank 51

7. Concluding Remarks and recommendations **54**
7.1 Analysis and results 54
7.2 Conclusion 55
7.3Recommendations for future studies 55

References **57**

Appendices **58**
Appendix A : 58
(A1). Single line arrangement of the Galle GSS 58
(A2) .AVR and PF control circuit arrangement of the GSS 58
(A3). Single unit (5MVAr) of the BSC bank at Galle GSS 59

Appendix B **60**
(B1). Data record at various tap position of the transformers
(B1.1). OLTC at tap 08 60
(B1.2). OLTC at tap 10-11 60
(B1.3) .OLTC at tap 12 61
(B1.4). OLTC at tap 12-14 61
(B2). Data recording switching various BSC bank combinations
(B2.1). OLTC at tap 08-14 and with one BSC bank on 62
(B2.2). OLTC at tap 08-14 and with two BSC bank on 63
(B2.3). OLTC at tap 08-14 and with three BSC bank on 64
(B2.4) . OLTC at tap 08-14 and with four BSC bank on 65

Acknowledgement

Thanks are due first to my supervisors, Dr. J.P. Karunadasa and Eng. Mr. K.P. Kusum Santhi, for their great insights, perspectives, guidance and sense of humor. My sincere thanks go to the officers in Post Graduate Office, Faculty of Engineering, University of Moratuwa, Sri Lanka, for helping in various ways to clarify the things related to my academic works in time with excellent cooperation and guidance. Sincere gratitude is also extended to the people who serve in the Department of Electrical Engineering office.

I extend sincere gratitude to my employer which is Ceylon Electricity Board (CEB) providing necessary duty leave for attending lectures and giving necessary technical details about the Galle Grid Substation where my study was done.

Lastly, I should thank many individuals, friends and colleagues who have not been mentioned here personally in making this educational process a success. May be I could not have made it without your supports.

D.G.S.Kumara,
Transmission (O&MS) Division
Galle Region

List of Figures

Figures		Page
Figure 2.1	Typical arrangement of OLTC and AVR system in transformers	04
Figure 2.2.1	Schematic diagram of the master –follower system	05
Figure 2.2 2	Equivalent scheme for two parallel transformers in accordance with minimizing circulating current method	06
Figure 2.3	Typical AVR Voltage Scale for Automatic OLTC Control	07
Figure 2.4.(a)	The bandwidth and the error threshold time setting set in the AVR	08
Figure 2.4.(b)	How does the time setting curve selected for various conditions in AVR	08
Figure 2.5.1	Hardware arrangement and operational block of the AVR system	09
Figure 2.5 2	Front view of the modern MR Tapcon 260 AVR control relay and MK 30 relay	09
Figure 2.5 3	Schematic connection diagram and the components of the AVR control system (two transformers are in parallel	10
Figure 3.2	Typical pad mounted Capacitor bank	12
Figure 3.3	Stacked rack capacitor bank	12
Figure 3.4	Typical pole mounted capacitor bank	13
Figure 3.3.4	Power factor controlling philosophy of the BSC bank	14
Figure 3.3.5	One of the methods of controlling capacitor var input to the system	15
Figure 3.4.1	Basic unit of the BSC controller (MasterPiece 020)	16
Figure 3.4.2	Type of the transducers used for the signaling	16
Figure 3.4.3	BSC bank control program structure embedded into the MasterPiece 020	17
Figure 3.4.4	Modern overall system how the BSC banks controls using SCADA system and the server	18
Figure 4.1 (a)	Ben analyzer connected for 33kV measurements	20
Figure 4.1 (b)	Analyzer connected for 132kV measurements	20
Figure 4.2	How the sensing equipments are connected	21
Figure 4.3 (a)	Pattern of the power factor measured at 33kv & 132kV levels over total measurement period	21
Figure 4.3 (b)	Pattern of the power factors measured at 33kv & 132kV levels on 21st July 2009	22
Figure: 4.6 (a)	Pattern of tap position with no capacitor banks 16th & 20th July 2009	25
Figure: 4.6 (b)	Pattern of tap position with no capacitor banks 21st & 22nd July 2009	25
Figure 5.1	132kV system and Transformer module with the circuit breakers	28
Figure 5.2	Modeling of the OLTC of the transformer	29
Figure 5.3	Load & load current measuring module	29
Figure 5.4	Capacitor bank & Inrush/Detuning reactor module	29
Figure 5.5	complete models for Galle Grid Substation	32
Figure 5.6	HV bus voltage variations under different cap bank configurations – Simulated data for 26st .28nd & 31th July 2009	34
Figure 5.7	Tap position variation to give constant LV voltage– Simulation results	35

Figure 5.8 Tap position variations to give constant LV voltage – Actual measurements 35
Figure 5.9 (a) Voltage and VAR flow of the system where at fixed tap and 36
Figure 5.9 (b) Voltage and VAR flow of the system where at varying tap with BSC bank switching ON 36
Figure 6.4 1 Circuit diagram and the controller arrangement of the system. 40
Figure 6.4.2 Mathematical model employed in the controller for decision 41
Figure 6.4.3 Shows the single phase arrangement of the schematic diagram 42
Figure 6.5 1 Flow chart illustrating the process of calculation in the controller 45
Figure 6.5.2 Primary system voltage variation with BSC bank ON (15MVAR) 46
Figure 6.5.3 Secondary system voltage variation with BSC bank ON (5MVAR) 46
Figure 6.5.4 System MVAR flow through the transformers 46
Figure 6.5.5 Sudden voltage dip existed in the primeray side for 175 S period 47
Figure 6.5.6 Secondary side voltage variation with BSC bank switch ON 47
Figure 6.5.7 System VAR flow at that instance with switching the BSC bank 48
Figure 6.5.8 Primary side voltage variation with steady increase in load 48
Figure 6.5.9 Secondary side voltage variation with steady increase in load 49
Figure 6.5.10 System MVAR flow through the GSS 49
Figure 6.6.1 Typical VAR control concept 50
Figure 6.6.2.1 Proposal for dead bands for AVR and capacitor controller 52
Figure 6.6.2.2 Comparison of switched banks under voltage control schemes & var control with 52
Figure 6.6.2.3 Block diagram and input and output signal arrangement of the controller 53

List of Tables

Table	Page
Table 4.6 Out of the simulation and actual reading	51
Table 5.1.VAR and Voltage variation at fixed tap with varying load	33
Table 5.2 Multi mode run of the system with various tap switching capacitor banks	33
Table 6.6.1 No of switching operations under proposed VAR control scheme	51