



DESIGN OF CONTROL PHILOSOPHY BETWEEN TRANSFORMER AVR CONTROL AND BSC BANK PFCONTROL

A dissertation submitted to the
Department of Electrical Engineering, University of Moratuwa
in partial fulfilment of the requirements for the
Degree of Master of Science

by
DICKMADU GODAGE SUMITH KUMARA

Supervised by: 1. Dr. J.P. Karunadasa
2. Eng. Mr. K.P. Kusum Shanthi

Department of Electrical Engineering
University of Moratuwa, Sri Lanka

2009

94854



Abstract

Ceylon Electricity Board (CEB) controls major roll in Generation, Transmission and Distribution of the electrical power in the island. It has hydro-power capacity about 950MW and thermal power capacity 725 MW. The average VAR consumption a day is 650 MVAR. Average power factor of the operation of the system is about 0.95. Almost 80% of the distribution of electrical power is done by CEB. The transmission network totally owned operated by CEB. The CEB transmission system consists of 220k V and 132kV network. It has 44 Grid Substation which convert 132kV/33kV for the distribution of the power to low voltage consumers. In this Grid Substation there is 109 132kV/33kV power transformer each having capacity of 31.5 MVA.

There are Breaker switch capacitors (BSC) bank installed at some places of these GSS. The total installed capacity of the shunt BSC bank is amount to 320MV AR and yet another 70MV AR planning to connect in the near future. In these GSS there are two systems to control 33kV bus voltage at reference 33kV level. One system varies the transformer tap position by controlling 33kV voltage. We called this as On-Load Tap Control of the transformer. For this to be done there is controller (AVR) which sends the command to OLTC to take appropriate action of increasing or decreasing the tap. On the other hand there is a BSC bank which allowed controlling the reactive power of the GSS.

The main intentions of the use of capacitor banks is to give voltage support at the substation level, reduction of losses in power transformers and transmission lines, and to release the capacity constraints in transformers and lines. CEB uses power factor regulation for switching these capacitor banks for above purposes but no studies have been done to evaluate its suitability with transformer AVR.

Even though these two controllers try to maintain VAR and Voltage (Q&V) of the GSS they are operating independently. Because of that We could not achieved maximum effect of these two system i.e., under optimization of the Voltage and Var.



Some time we have observed that these two controllers are hunting with each other by doing the controlling.

If we could coordinate these two controllers to make proper function we indirectly could save the number of tap operations of the transformer and that will help reducing costly maintenance of the OLTC. My main intention is to coordinate these two controllers to achieve above objects. I further try to develop a new system to take care of the both functions in one unit. I have used PSCAD software program for simulation of the GSS.

For the real time data collection I used two data loggers which are property of the CEB. Finally I have found that for controlling the both controllers we need a additional parameter which High Voltage side voltage measurement which could be easily available at the GSS without any additional cost. Taking this new parameter with existing parameters I have develop a control philosophy which coordinates both the transformer AVR controller and BSC bank controller by optimizing voltage and Var. flow through the system.

DECLARATION

The work submitted in this dissertation is the result of my own investigation, except where otherwise stated.

It has not already been accepted for any degree, and is also not being concurrently submitted for any other degree.

UOM Verified Signature

D.G.S.Kumara University of Moratuwa, Sri Lanka.
Electronic Theses & Dissertations
28th November 2009 www.lib.mrt.ac.lk

We/I endorse the declaration by the candidate.

UOM Verified Signature

Dr.J.P. Karunadasa.

15th December 2009

UOM Verified Signature

Eng.Mr.K.P. Kusum Santhi

15th December 2009



Contents

Declaration	i
Abstract	iv
Acknowledgement	v
List of Figures	vi,vii
List of Tables	viii

Chapters

1. Introduction	1
1.1 Background	1
1.2 Objectives	1
1.3 Scope of the work	2
1.4 Present problems in AVR and PF control Transmission GSS	3
2. Automatic Voltage Control (AVR) of transformers in GSS	4
2.1 Power transformer and On Load Tap Changer (OLTC)	4
2.2 OLTC control principle for paralleling transformers in the GSS	4
2.2.1 Operations of the Master – Follower method	5
2.2.2 Operation of the minimum circulation method	5
2.3 Controlling philosophy of Moratuwa, Sri Lanka.	7
2.4 Setting of the parameters of the AVR in CEB	7
2.5 Internal hardware structure of the TF's AVR and how it operates	8
3. Methods used for controlling the capacitor bank in GSS	11
3.1 Shunt Capacitors	11
3.2 Different types of capacitor banks	12
3.3 Capacitor bank controlling philosophy	13
3.3.1 Temperature control	13
3.3.2 Time control	13
3.3.3 Current control	14
3.3.4 Power factor control	14
3.3.5 VAR Control	15
3.3.6 Voltage control	15
3.4 Description of the existing controller in the Galle GSS	16
4. Case study for Galle Grid Substation	19
4.1 Substation technical details	19
4.2 Collection of the system data and measurements	19
4.3 Measuring devices and data loggers	20
4.4 Variation in the power factor in the GSS	21
4.5 Switching pattern of the capacitor banks in the GSS	22
4.6 Uncompensated reactive power	23
4.7 Summary of the system study	26

5. System modeling and simulations	27
5.1 Software selection for modeling	27
5.2 Components in the substation modeling	28
5.3 Running the simulation	30
5.3.1 Theoretical aspect of the simulation study	30
5.3.2 Transformer var consumption	31
5.4 Data recording and graphs	34
6. Design of new controller for BSC bank controlling	37
6.1. Introduction of the design	37
6.2. Factors that have been considered for designing the controller	38
6.3. Brief description of the drawings and figures	39
6.4. Detailed description of the design	39
6.5 Sample calculation of the decision variables	44
6.6. Factors that can be included in the design for further improvements	50
6.6.1 VAR controlling of the BSC bank	50
6.6.2. Voltage controlling of the BSC bank	51
7. Concluding Remarks and recommendations	54
7.1 Analysis and results	54
7.2 Conclusion	55
7.3 Recommendations for future studies	55
References	57
Appendices	58
Appendix A :	58
(A1). Single line arrangement of the Galle GSS	58
(A2) .AVR and PF control circuit arrangement of the GSS	58
(A3). Single unit (5MVAR) of the BSC bank at Galle GSS	59
Appendix B	60
(B1). Data record at various tap position of the transformers	
(B1.1). OLTC at tap 08	60
(B1.2). OLTC at tap 10-11	60
(B1.3) .OLTC at tap 12	61
(B1.4). OLTC at tap 12-14	61
(B2). Data recording switching various BSC bank combinations	
(B2.1). OLTC at tap 08-14 and with one BSC bank on	62
(B2.2). OLTC at tap 08-14 and with two BSC bank on	63
(B2.3). OLTC at tap 08-14 and with three BSC bank on	64
(B2.4) . OLTC at tap 08-14 and with four BSC bank on	65



Acknowledgement

Thanks are due first to my supervisors, Dr. J.P. Karunadasa and Eng. Mr. K.P. Kusum Santhi, for their great insights, perspectives, guidance and sense of humor. My sincere thanks go to the officers in Post Graduate Office, Faculty of Engineering, University of Moratuwa, Sri Lanka, for helping in various ways to clarify the things related to my academic works in time with excellent cooperation and guidance. Sincere gratitude is also extended to the people who serve in the Department of Electrical Engineering office.

I extend sincere gratitude to my employer which is Ceylon Electricity Board (CEB) providing necessary duty leave for attending lectures and giving necessary technical details about the Galle Grid Substation where my study was done.

Lastly, I should thank many individuals, friends and colleagues who have not been mentioned here personally in making this educational process a success. May be I could not have made it without your supports.

D.G.S.Kumara,
Transmission (O&MS) Division
Galle Region



University of Moratuwa, Sri Lanka.
Electronic Theses & Dissertations
www.lib.mrt.ac.lk



List of Figures

Figures	Page
Figure 2.1 Typical arrangement of OLTC and AVR system in transformers	04
Figure 2.2.1 Schematic diagram of the master –follower system	05
Figure 2.2.2 Equivalent scheme for two parallel transformers in accordance with minimizing circulating current method	06
Figure 2.3 Typical AVR Voltage Scale for Automatic OLTC Control	07
Figure 2.4.(a) The bandwidth and the error threshold time setting set in the AVR	08
Figure 2.4.(b) How does the time setting curve selected for various conditions in AVR	08
Figure 2.5.1 Hardware arrangement and operational block of the AVR system	09
Figure 2.5.2 Front view of the modern MR Tapcon 260 AVR control relay and MK 30 relay	09
Figure 2.5.3 Schematic connection diagram and the components of the AVR control system (two transformers are in parallel)	10
Figure 3.2 Typical pad mounted Capacitor bank	12
Figure 3.3 Stacked rack capacitor bank	12
Figure 3.4 Typical pole mounted capacitor bank	13
Figure 3.3.4 Power factor controlling philosophy of the BSC bank	14
Figure 3.3.5 One of the methods of controlling capacitor var input to the system	15
Figure 3.4.1 Basic unit of the BSC controller (MasterPiece 020)	16
Figure 3.4.2 Type of the transducers used for the signaling	16
Figure 3.4.3 BSC bank control program structure embedded into the MasterPiece 020	17
Figure 3.4.4 Modern overall system how the BSC banks controls using SCADA system and the server	18
Figure 4.1 (a) Ben analyzer connected for 33kV measurements	20
Figure 4.1 (b) Analyzer connected for 132kV measurements	20
Figure 4.2 How the sensing equipments are connected	21
Figure 4.3 (a) Pattern of the power factor measured at 33kv & 132kV levels over total measurement period	21
Figure 4.3 (b) Pattern of the power factors measured at 33kv & 132kV levels on 21 st July 2009	22
Figure: 4.6 (a) Pattern of tap position with no capacitor banks 16 th & 20 th July 2009	25
Figure: 4.6 (b) Pattern of tap position with no capacitor banks 21 st & 22 nd July 2009	25
Figure 5.1 132kV system and Transformer module with the circuit breakers	28
Figure 5.2 Modeling of the OLTC of the transformer	29
Figure 5.3 Load & load current measuring module	29
Figure 5.4 Capacitor bank & Inrush/Detuning reactor module	29
Figure 5.5 complete models for Galle Grid Substation	32
Figure 5.6 HV bus voltage variations under different cap bank configurations – Simulated data for 26 st ,28 nd & 31th July 2009	34
Figure 5.7 Tap position variation to give constant LV voltage– Simulation results	35

Figure 5.8 Tap position variations to give constant LV voltage – Actual measurements	35
Figure 5.9 (a) Voltage and VAR flow of the system where at fixed tap and	36
Figure 5.9 (b) Voltage and VAR flow of the system where at varying tap with BSC bank switching ON	36
Figure 6.4.1 Circuit diagram and the controller arrangement of the system.	40
Figure 6.4.2 Mathematical model employed in the controller for decision	41
Figure 6.4.3 Shows the single phase arrangement of the schematic diagram	42
Figure 6.5.1 Flow chart illustrating the process of calculation in the controller	45
Figure 6.5.2 Primary system voltage variation with BSC bank ON (15MVAR)	46
Figure 6.5.3 Secondary system voltage variation with BSC bank ON (5MVAR)	46
Figure 6.5.4 System MVAR flow through the transformers	46
Figure 6.5.5 Sudden voltage dip existed in the primeraay side for 175 S period	47
Figure 6.5.6 Secondary side voltage variation with BSC bank switch ON	47
Figure 6.5.7 System VAR flow at that instance with switching the BSC bank	48
Figure 6.5.8 Primary side voltage variation with steady increase in load	48
Figure 6.5.9 Secondary side voltage variation with steady increase in load	49
Figure 6.5.10 System MVAR flow through the GSS	49
Figure 6.6.1 Typical VAR control concept	50
Figure 6.6.2.1 Proposal for dead bands for AVR and capacitor controller	52
Figure 6.6.2.2 Comparison of switched banks under voltage control schemes & var control with	52
Figure 6.6.2.3 Block diagram and input and output signal arrangement of the controller	53



List of Tables

Table	Page
Table 4.6 Out of the simulation and actual reading	51
Table 5.1. VAR and Voltage variation at fixed tap with varying load	33
Table 5.2 Multi mode run of the system with various tap switching capacitor banks	33
Table 6.6.1 No of switching operations under proposed VAR control scheme	51



University of Moratuwa, Sri Lanka.
Electronic Theses & Dissertations
www.lib.mrt.ac.lk



1.1 Background

This study is related to coordinating shunt reactance switching (BSC Bank or Reactor) in power transmission and/or supply systems, and in one embodiment, for coordinating shunt compensation switching with on load tap change transformers.

A system and method for coordinating shunt reactance switching in a power system with transformer having primary and secondary voltage for supplying low voltage power to a load. Voltage (V), Current (I), Power (W) and Reactive power (Q) are measured at both side of the transformer flowing to the load. A Programmable Logic Controller (PLC) or Intelligent Electronic Device (IED) receives as one set of input measurements of primary voltage and reactive power flowing to the load and as another set of inputs, predetermine ranges establishing high and low limits for the voltage and reactive power. Base on these inputs, PLC connects or disconnects at least one shunt reactance to maintain the load voltage substantially constant.

Voltage fluctuation and drop on High Voltage AC system can be reduced by installing static reactive power generators (Some time known as VAR generators) on the grid substation or on the transmission/distribution lines [5]. Voltage regulation is based on the fact that essentially inductive transmission lines, transformers, voltage increases if capacitive current is injected in to the system by for example, connection of a shunt capacitor across the line/load. Alternatively voltage can be decrease by connecting and inductor across the line/load (or by removing a previously connected capacitor). Static VAR generators may be switched across the line using electromagnetic relay devices controlled by a predetermined timer or using a thyristor.

A problem facing many utilities is controlling shunt compensation on voltage buses especially where voltage is already regulated by an On Load Tap Change (OLTC) transformer. In an OLTC transformer, the low side line voltage delivered to the load is monitored and regulated by a conventional, fine tuning OLTC controller. Such a controller measures actual low side voltage, compares it with desired value, and then adjusts the position where the OLTC makes contact with high side OLTC transformer coil, e.g., via a control signal to a motorized tap changer. Typical OLTC transformers may have 16 to 32 tap positions, with each position being representative of some fractional portion of the rated voltage. Thus, for example, a one position tap change on a 32 tap OLTC transformer would cause a relatively small bus voltage change as compared with the rated or desired output voltage.

In operation, an OLTC transformer compares the secondary side voltage with both a minimum and a maximum voltage threshold. If either threshold is exceeded, a timer is started [10]. If the timer exceeds a predetermined delay period, the OLTC controller moves the tap to increase or decrease the secondary voltage as necessary.

OLTC transformers function well to effect small changes in voltage. However large voltage fluctuations required switching of shunt reactance to ensure that sufficient reactive power is provided to the system, end-users and customers such that secondary voltage can be held essentially constant. Since the OLTC controller is already monitoring and

regulating the secondary distribution voltage, a shunt reactance control unit cannot also directly control that secondary distribution voltage. As a result, most utilities typically follow a fairly rigid load cycle to estimate roughly when a reactance element, such as a capacitor bank, should be switched in shunt across the load to offset a decrease in the secondary distribution voltage from an increased load.

After capacitor bank switching, The OLTC controller gradually adjusts the tap to return the low side voltage to the desired value. This rigid scheduling is far from optimal because it fails to accurately respond to actual system need (as opposed to scheduled estimates) and to detect abnormal system condition. On the other hand the power factor controlling of the shunt BSC bank too have similar effect because it did not take in to account of the low side bus voltage variation. Some time when these two controllers are responding there may be instances that some hunting of the two control system is experienced and this too not good for the system and the component itself.

1.2 Objectives

The present method seeks to overcome these problems by flexibly coordinating the OLTC fine tune controller and shunt reactance switching (BSC or Reactor). More specifically this method provides voltage and reactive power regulation using a programmable controller (PLC) or intelligent electronic device (IED) for controlling shunt capacitor switching in order to attain following exemplary objectives.

- Coordinate of the two controllers for making optimal use of the BSC bank VAR and transformer OLTC operations
- Maintain the distribution and transmission voltages at required set value;
- Track the station loading;
- Complements the action of the OLTC transformer;
- Provide sufficient dead-band and time delays to avoid hunting;
- Detect and compensate abnormal system conditions;

1.3 Scope of work

This study seeks the following problems faced by the GSS. It is also noted that frequent tap operations of the transformer deteriorate the diverter switch of the OLTC which is much expensive unit to be replaced. On the other hand the VAR – Voltage Optimisation did not take in to account when operating these two controllers because they are responded by independently.

- Studying the existing Transformer AVR and BSC bank control system used in CEB Tx. Network;

- Check whether parameterizations have been properly done;
- Studying the available above controllers in the present market;
- Simulate the Q-V variation/requirement in grid by using PSCAD;
- Simulate the present Q-V hunting problem at 33kV bus bar with using actual loads;
- Check whether this could be overcome by changing all possible parameters in AVR and capacitor controller;
- Prove that communication is needed between AVR and controller to overcome the problem;
- Seek possibilities of designing a control module between two units;
- If it is not workable, then design a integrated control module to cater both *functions in a single module*;

1.4 Present problems in AVR and PF control in Transmission Grids Substations

Most of the utility systems that delivers power to customer, prime statutory obligation is to keep the voltage as much as possible at constant at delivery point of the substation. Voltage control mainly done by transformer AVR control which changes the turn ratio of the transformer primary winding. Some time there are GSS which installed a breaker switch capacitor to control VAR flow of the substation [2]. When these two systems responses to the different parameters they are finally adjust the voltage and VAR in the substation. Following operational constraints have to be taken in to account when studying the system as a unit [3].

- AVR system connected to transformers is controlled by system voltage;
- PF controller connected to capacitors is operated as per Q requirements;
- No coordination between AVR and PF controllers though they control system Q and V;
- Experience the hunting phenomena in both AVR and PF controllers;

2. Automatic Voltage Control (AVR) of transformer in Substations

2.1. Power Transformers and the On Load Tap Changer (OLTC)

Presently CEB Grid Substation has been installed with two to three, numbers 31.5MVA transformers which are equipped with On Load Tap Changer (OLTC). Typical OLTC transformers may have 16 to 32 tap positions, with each position being representative of some fractional portion of rated voltage. Thus, for example, a one position tap change on a 32 tap OLTC transformer would cause a relatively small 33kV bus voltage change as compared with the rated or desired output voltage. Typical step size of the tap voltage is 1.5% to 1.25% of the rated voltage. The OLTC is placed on the high voltage side winding of the transformer due to economic and easy insulation coordination. Figure 2.1 shows how the entire system operates with its components.

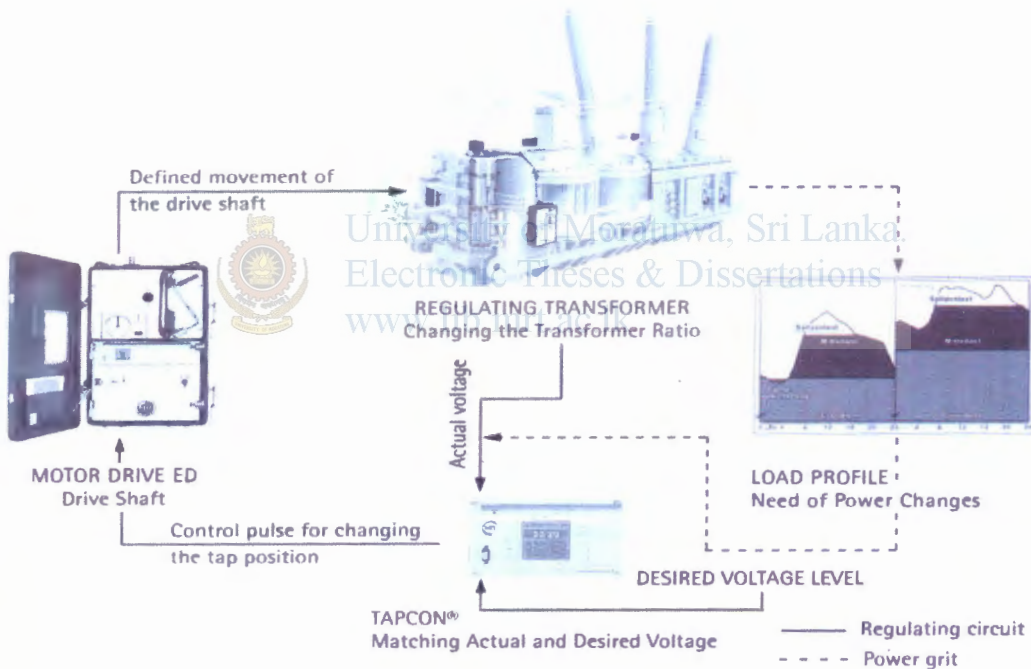


Figure 2.1 Typical arrangement of OLTC and AVR system in transformers

2.2. OLTC control principles for paralleling transformers in the GSS

Automatic On-Load Tap-Changer Control of parallel transformers can be made according to three different methods:

1. Reverse Reactance method
2. Master - Follower method
3. Minimum Circulating Current method [1],[10]

Unlike the first method, the last two methods require exchange of signals and measured values between the transformers, or between the transformers and a central control unit. However, the drawback with the first method is that the voltage control will be affected by changes in the load power factor. The Master-Follower method is generally limited to applications with similar transformers, whilst the circulating current method, which is typically available in new numerical AVRs, also handles, in an elegant way, the more generic case with unequal transformers in parallel operation.

2.2.1. Operations of the Master – Follower Method:

In this method the two transformers which are in equal impedance connected in parallel. The secondary side voltage and current are taken through Voltage Transformer (VT) and Current Transformer (CT) into the Automatic Voltage Control (AVR) devices. There is also logic for the two transformers where both transformers are in parallel, only one AVR is acted and it is called Master and the other simply follows the master [10].

For these operations, the logic was taken from each secondary side circuit breaker auxiliary contact. There is another function called independent which operate under secondary side (33kV) bus-coupler is opened position. In that case two controllers are independently operated with each other. Figure 2.2.1 shows schismatic diagram of the Mater follower system in the GSS.

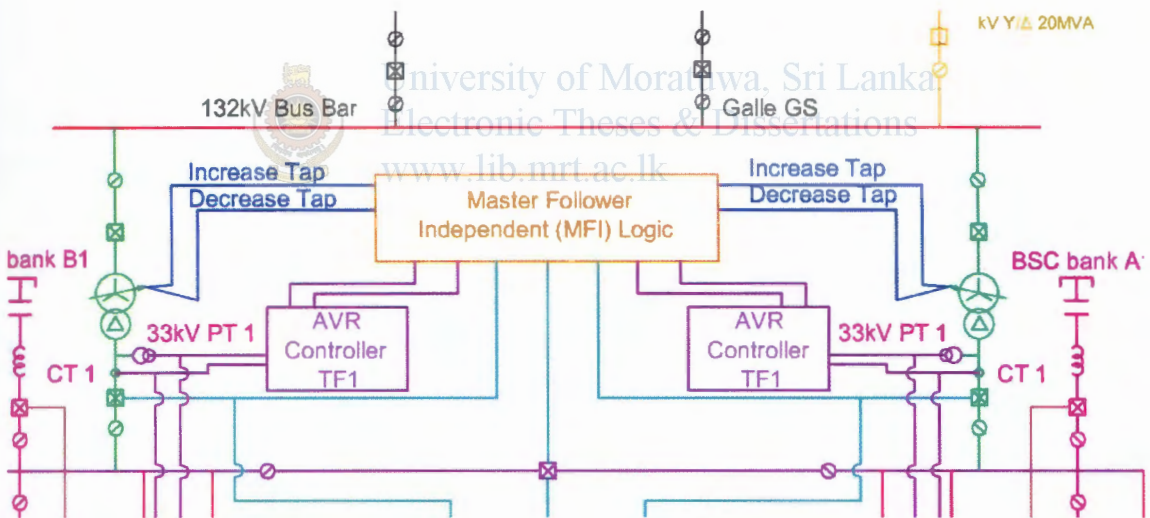


Figure 2.2.1 Schematic diagram of the master –follower system

2.2.2. Operations of the Minimum Current Circulation Method:

Two main objectives of voltage control of parallel transformers with the circulating current method are:

1. Regulate the LV side busbar voltage to the preset target value
2. Minimize the circulating current, in order to achieve optimal sharing of the reactive load between parallel operating transformers

The first objective is the same as for the voltage control of a single transformer while the second objective tries to bring the circulating current, which appears due to unequal LV

side no load voltages in each transformer, into an acceptable value. Figure 2.2.2 shows an example with two transformers connected in parallel. If transformer T1 has higher no load voltage (i.e. U_{T1}) it will drive a circulating current which adds to the load current in T1 and subtracts from the load current in T2. It can be shown that the magnitude of the circulating current in this case can be approximately calculated with the following formula [1]:

$$|I_{cc_T1}| = |I_{cc_T2}| = \left| \frac{U_{T1} - U_{T2}}{Z_{T1} + Z_{T2}} \right|$$

Because transformer impedances are dominantly inductive it is possible to use only the transformer reactance in the above formula. At the same time this means that transformer T1 circulating current lags the busbar voltage almost 90° , whilst transformer T2 circulating current leads the busbar voltage by almost 90° . This also means that the circulating current is mainly reactive in nature, and it only represents reactive power that circulates between two transformers connected in parallel.

Therefore by minimizing the circulating current flow through the transformers, the total reactive power flow through the parallel-connected transformer group is optimised as well. At the same time, at this optimum state the apparent power flow is distributed among the transformers in the group in direct proportion to their rated power.

Therefore an AVR [1], regardless of whether it is used for single or parallel transformer control, always reacts and changes OLTC position in accordance with LV side load variations. However, the AVR will as well react on abnormal voltage variations on the high voltage (HV) side of the power transformer. Sometimes such AVR behaviour is not desirable because it just further increases the total load on the HV system (i.e. transmission system). Especially, such behaviour shall be prevented during critical operation states of the transmission system such as a slow power system voltage collapse [5].

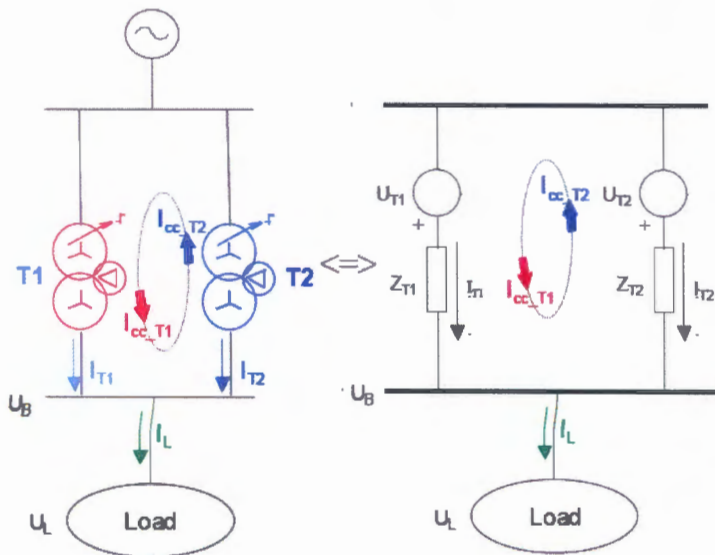


Figure 2.2.2 Equivalent scheme for two parallel transformers in accordance with minimizing circulating current method

2.3. Controlling philosophy

A typical AVR measures the busbar voltage (U_B) at the power transformer LV side, and if no other additional features are enabled (i.e. line drop compensation) this voltage is used for voltage regulation. The voltage control algorithm then compares U_B with the set target voltage (U_{set}) and decides which action should be taken. Because this control method is based on a step-by-step principle, a dead-band ΔU (i.e. degree of insensitivity) is introduced in order to avoid unnecessary switching around the target voltage. The dead-band is typically symmetrical around U_{set} as shown in Figure 2.3. Dead-band should be set to a value close to the power transformers OLTC voltage step. Typical setting is 75% of the OLTC step [2].

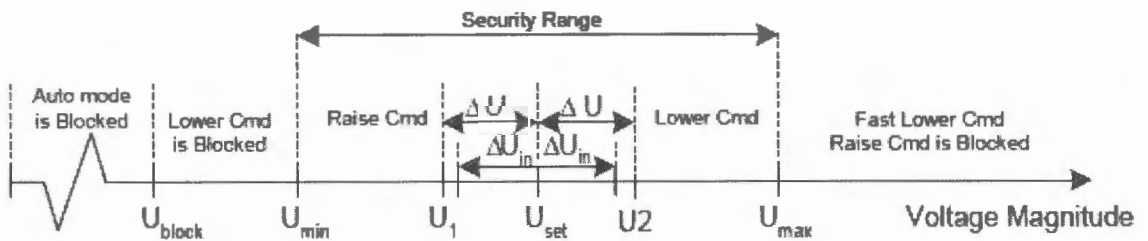


Figure 2.3 Typical AVR Voltage Scale for Automatic OLTC Control

During normal operating conditions the busbar voltage U_B , stays within the dead-band. In that case no actions will be taken by the AVR. However, if U_B becomes smaller than U_1 or greater than U_2 (see Figure 2.3), an appropriate lower or raise timer will start. The timer will run as long as the measured voltage stays outside the inner dead-band. If this condition persists for longer than a preset time, the appropriate LOWER or RAISE command will be issued. If necessary, the procedure will be repeated until the busbar voltage is again within the inner dead-band [1].

The main purpose of the time delay is to prevent unnecessary OLTC operations due to temporary voltage fluctuations. The time delay may also be used for OLTC co-ordination in radial distribution networks in order to decrease the number of unnecessary OLTC operations. This can be achieved by setting a longer time delay for AVRs located closer to the end consumer and shorter time delays for AVRs located at higher voltage levels

2.4. Setting of parameters of the AVR in the CEB network:

A. Band width (BW) $-\Delta U = U_{st} * 1.6$ ($U_{st} = 1.25\%$ of U_{rated} or 1.5%)

B. Time (Rate of change of voltage), 10 second curve

Following Figure 2.4.(a) and Figure 2.4.(b) shows how does the two parameters functions in the AVR controller. It very important to set these two parameters according to the power system operation condition otherwise it will ruins to hunting and transient conditions of the system [2].



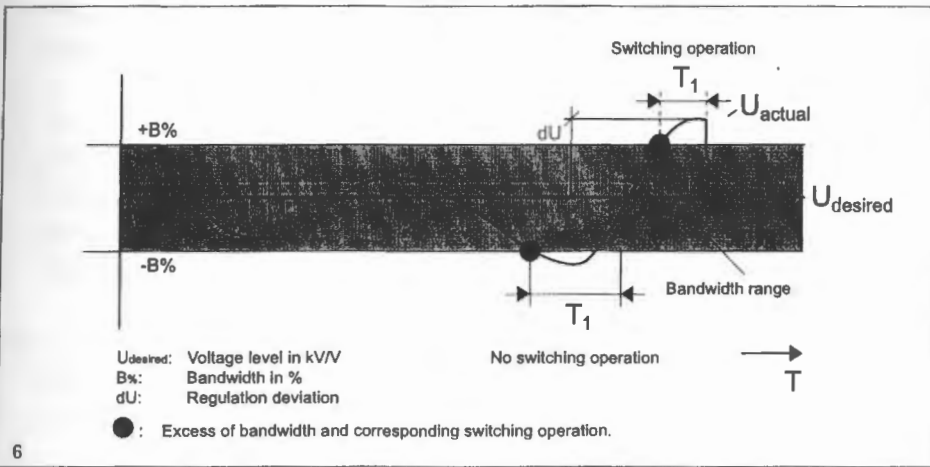


Figure 2.4.(a) The bandwidth and the error threshold time setting set in the AVR

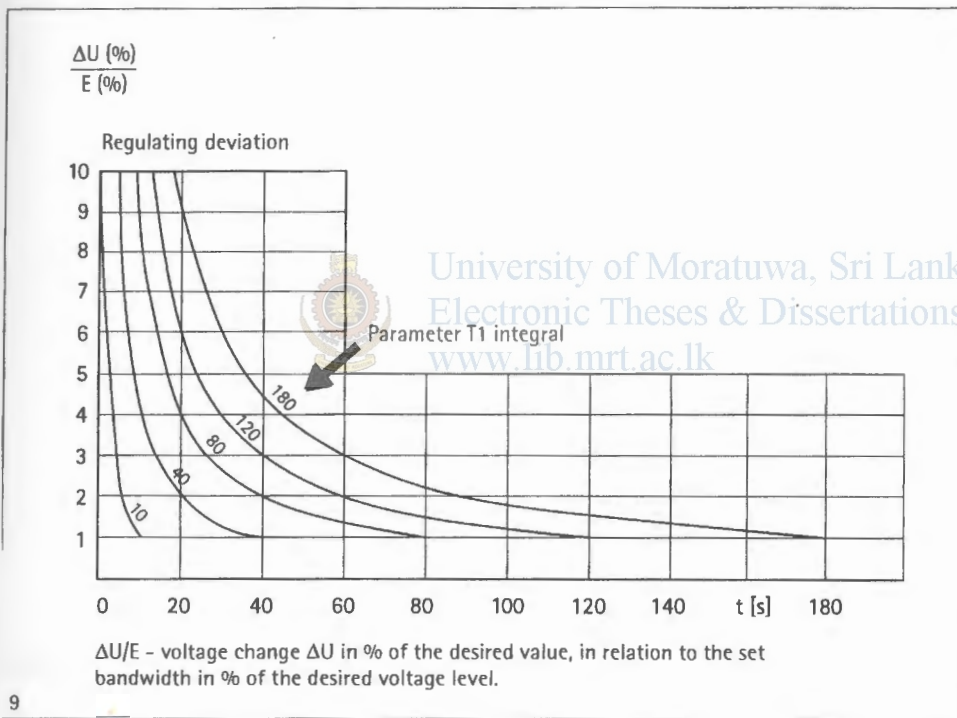


Figure 2.4.(b) How does the time setting curve selected for various conditions in AVR

2.5. Internal hardware structure of the Transformer AVR and how it operates:

Figure 2.5.1 shows arrangement of the system components of the conventional AVR. The description of these components will be primarily in terms of functions, with suitable hardware and software being used to achieve required functions. The AVR unit is constructed so as to have:

- (1) A deviation integrating function 1000 for integrating the deviation V_3 between system-voltage V_1 which is input to the apparatus and a reference voltage V_2 for a constant time period, this function being shown in the figure ;

- (2) A system-voltage status evaluating function 2000 for identifying features capable of improving the voltage characteristics and reducing the frequency of tap change of a tap changing transformer;
- (3) An integration constant corrected value inferring function 3000 for inferring an integration constant corrected value by input of the result derived by the system-voltage status evaluating function 2000 using fuzzy inference on the basis of an integration constant correcting rule, which rule expresses the relationship between the status evaluation result and the integration constant corrected value;
- (4) A judging function 4000 for judging whether or not switching of the tap is necessary; this is on the basis of consideration of the corrected value obtained by the inferring function 3000;
- (5) An on-load tap changing transformer 5000 to be controlled.

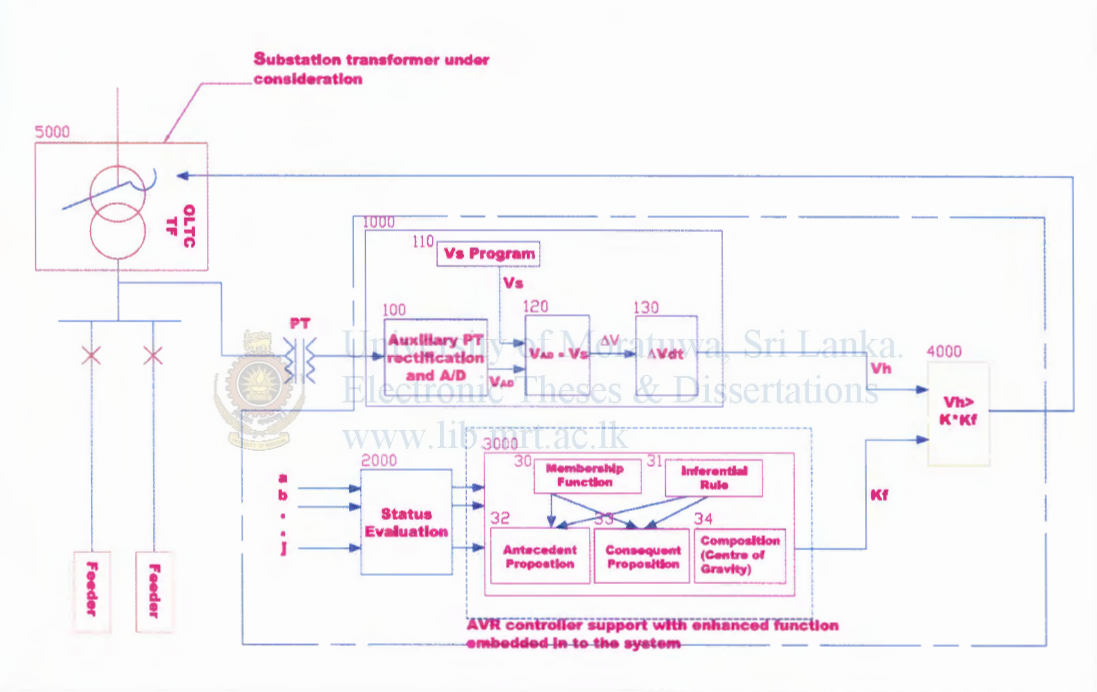


Figure 2.5.1 Hardware arrangement and operational block of the AVR system

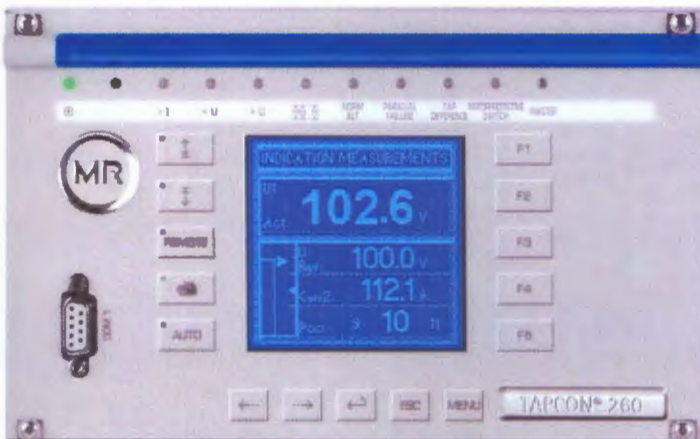


Figure 2.5.2 Front view of the modern MR Tapcon 260 AVR control relay and MK 30 relay

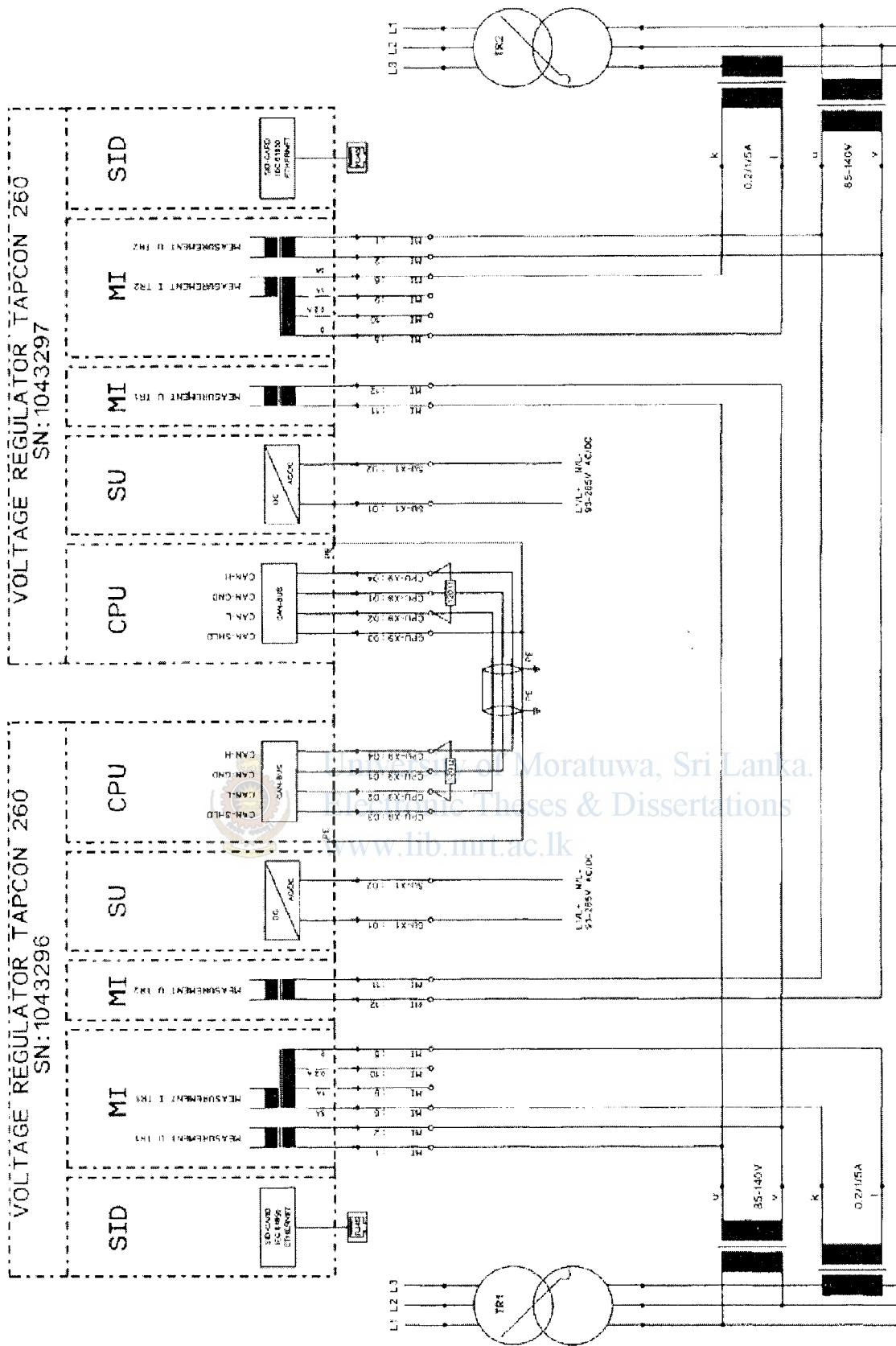


Figure 2.5 3 Schematic connection diagram and the components of the AVR control system (two transformers are in parallel)

3. Methods used for controlling the capacitor banks in Substations

3.1 Shunt Capacitors

Use of capacitor banks in utility substations as a source of reactive power is not new to electricity transmission and distribution. They are comparatively inexpensive, easy and quick to install, and can be deployed at any location. Therefore, this is one of the most economical way of generating the reactive power requirement and maintaining the voltage stability in power systems in comparison to the other similar devices such as static VAR compensators, STATCOM devices etc.

Capacitor Banks consist of individual capacitor units where such a unit is a combination of shunt or series set of capacitor elements. Depending on the bank size, those units are again connected in series or parallel to give the required size. In medium and high voltage levels, sizing of the capacitors in parallel combinations in banks generally has to consider the discharge energy through a shorted parallel capacitor in the same group [8], [4].

These capacitors banks are fixed or switched type according to a local requirement. The switched type capacitor banks give a poor regulation due to step wise connections. Typical applications of capacitor banks at different locations are shown in Figure 3.2



University of Moratuwa, Sri Lanka.
Electronic Theses & Dissertations
www.lib.mrt.ac.lk

3.2 Different types of Capacitor banks

Different types of capacitor banks are available in the present market. Metal enclosed type, pad mounted type, stack-rack banks and pole tip mounted types are the most common type in utility applications [8]. Metal enclosed type banks specifically made for indoor installations. Pad mounted capacitor banks are also enclosed in a metal enclosure and commonly used for areas where accessible to public.

Normally, metal enclosed and pad mounted units come with factory assembled and tested hence the installation is very easy. Those banks significantly reduce unnecessary human interference such as trespassing and tampering. They do not need a fence around it. However their initial cost is high compared to other types and only available up to a certain voltage level.





Figure 3.2 Typical pad mounted Capacitor bank

Stack rack capacitor banks are commonly used in the utility sub stations. The initial cost of these is comparatively low and all components are visible. The components are easily replaceable and also easily expandable



Figure 3.3 Stacked rack capacitor bank

The pole tip mounted banks are commonly used in distribution networks for improving the voltage profile in distribution lines. Those are available as smaller banks and eliminate the need for space. The maintenance and component replacement is little difficult.

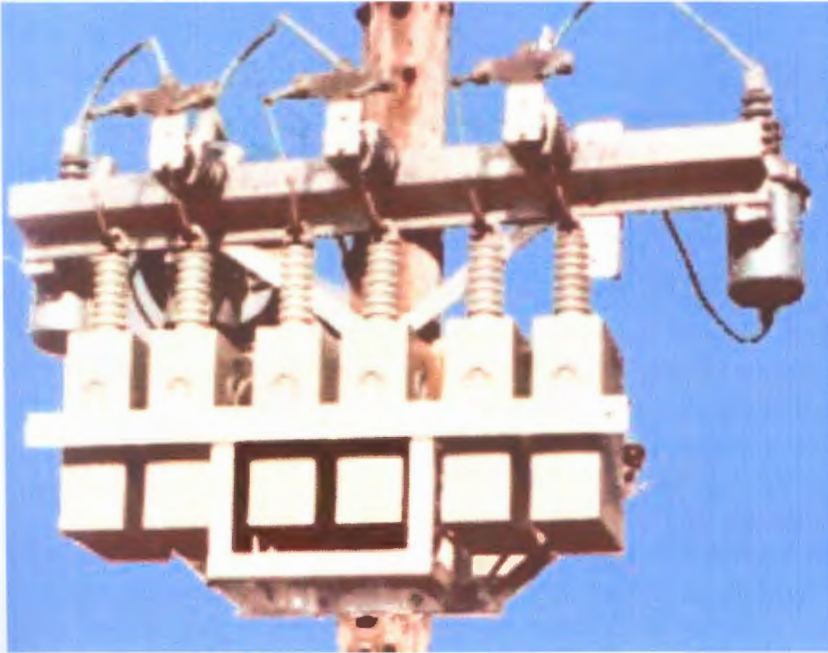


Figure 3.4 Typical pole mounted capacitor bank

3.3 Controlling philosophy

The switching of the breaker switched capacitor banks in utility substations depends on the local requirements of each utility. Basic need for such a control is to regulate the bus voltage, reduce the losses in lines and transformers and to avoid system constraints [9]. Depending on those, the controlling parameter may be different, and may be one of such as voltage, Var, time, temperature or power factor. Some of these parameters are directly represent the system parameters but some, for example power factor can be used as an indirect measurement for var, losses etc.,

3.3.1. Temperature control

This is not a true indicator of the system status and an indirect measure only. The control effectiveness depends on how well the load characteristics are known. Not useful in cases where those characteristics change often. Temperature control does not require any current sensors.

3.3.2. Time control

Somewhat better parameter for controlling and has to be based on load characteristics. Ever changing characteristics of the system load profiles does not allow the optimal controlling when time based control is used. Time control does not require any current sensors. Both time and temperature controlling need only simple and inexpensive controllers.

3.3.3. Current control

Current control is not an efficient control because it responds to total line current, and assumptions must be made about the load power factor. Current controls require current sensors.

3.3.4. Power factor control

The power factor is an indirect measure of the VAR load or the line or transformer losses of the system and always depends on the real power at the time of measurement. For same power factor, the actual amount of VAR load depends or changes according to the real power [9]. These measurements require both current and voltage sensors. Generally, power factor regulation or control is advisable for bulk consumer loads, to avoid low load power factors which are penalized by the utility companies. Power factor improvement by capacitor banks in the substation does not reduce the distribution line losses and neither eliminates distribution line constraints [12]. It will release the transformer capacities, reduces transmission line losses and improve the voltage profile. However power factor is an indirect measure for all these. Therefore, power factor controlled capacitor banks may not be fully utilized in most of the time unless the setting parameters are carefully assessed.

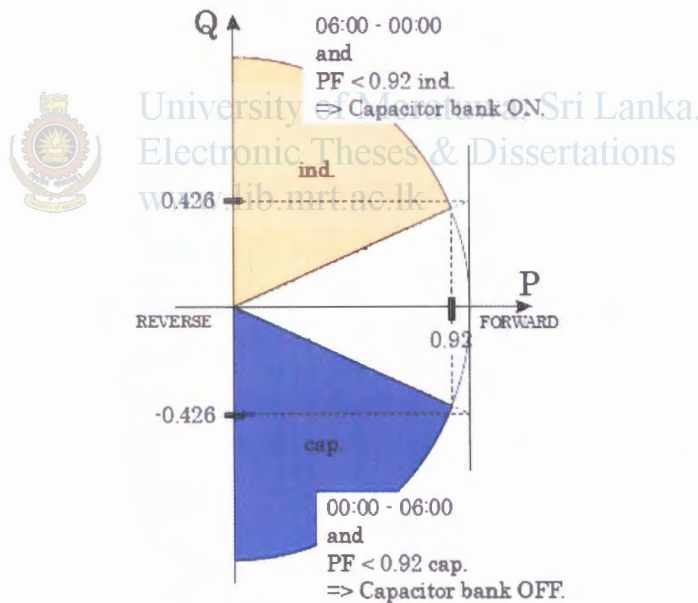


Figure 3.3.4 Power factor controlling philosophy of the BSC bank

We have noticed occasions where the capacitor banks kept unconnected due to power factor being within limits while the loads consume reactive power than minimum switchable steps. Specially, during low voltage profiles, since the power factor does not consider bus voltage, the capacitors may be kept unconnected if power factor is within the limits. This means that as a result of the switched capacitors they will reduce transmission line losses and improves the bus voltage, but power factor is not a measure of the need for the above. So, for a utility substation, power factor correction is not the best control criteria for switching. The above will be explained using system data in a later chapter.

3.3.5. VAR control

VAR control is the natural means to control capacitors because the latter adds a fixed amount of leading VAR to the system regardless of other conditions, and loss reduction depends only on reactive current. Since reactive current at any point along a feeder is affected by downstream capacitor banks, this kind of control is susceptible to interaction with downstream banks [6]. In a system like CEB, there are no switchable capacitor banks along the distribution feeder so that this problem will not arise. However, in multiple capacitor feeders, the furthest downstream banks should go on-line first and off-line last. VAR controls require current sensors and typically costly.

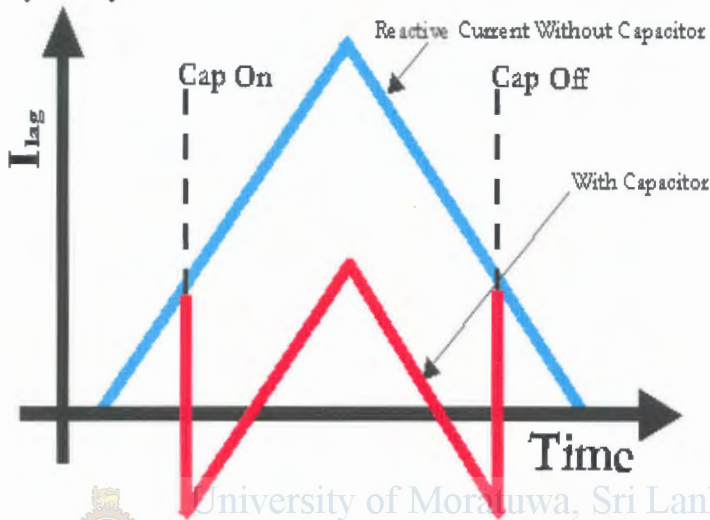


Figure 3.3.5 One of the methods of controlling capacitor VAR input to the system

3.3.6. Voltage control

Voltage control is used to regulate voltage profiles on the bus on which the capacitors are connected to [13]. However, while doing this it may not consider the reduction of system losses since lagging or leading low power factors always increase the currents through its components. Voltage control requires no current sensors.

Considering above parameters for switching the capacitor banks, we can define two concepts of control philosophies. First is single variable switching that considers only one measuring parameter. Second concept is multi variable and Boolean switching. In the latter case multiple parameters are measured and the decision for switching is done depending on the optimal situation considering both parameters. The fact we have to consider is the cost of the controllers.

3.4 Description of the existing controller in the Galle GS.

The Breaker Switch Capacitor Banks (BSC) is product of ASEA Sweden which is well known power product manufacturer but it is no more in the market as ASEA. The control system consists of two units called programming unit and the control unit (Basic unit). The programmes entered in to the Read/Write Memory (RAM) of the basic unit by means of the pushbuttons on the programming unit [6].

The basic unit which is called as Asea MasterPiece20 works digital input and output signals. The input signals are comes from different type of sensors like power factor transducer, current and voltage transducers. The control program consists of series of instruction each of which documents a step in the program memory. Figure 3.4.1 shows the basic unit of the BSC controller and Figure 3.4.2 shows the types of transducers used for measurement and the Figure 3.4.3 shows one of the internal program modules of the controller.



Figure 3.4.1 Basic unit of the BSC controller (MasterPiece 020)



Figure 3.4.2 Type of the transducers used for the signalling

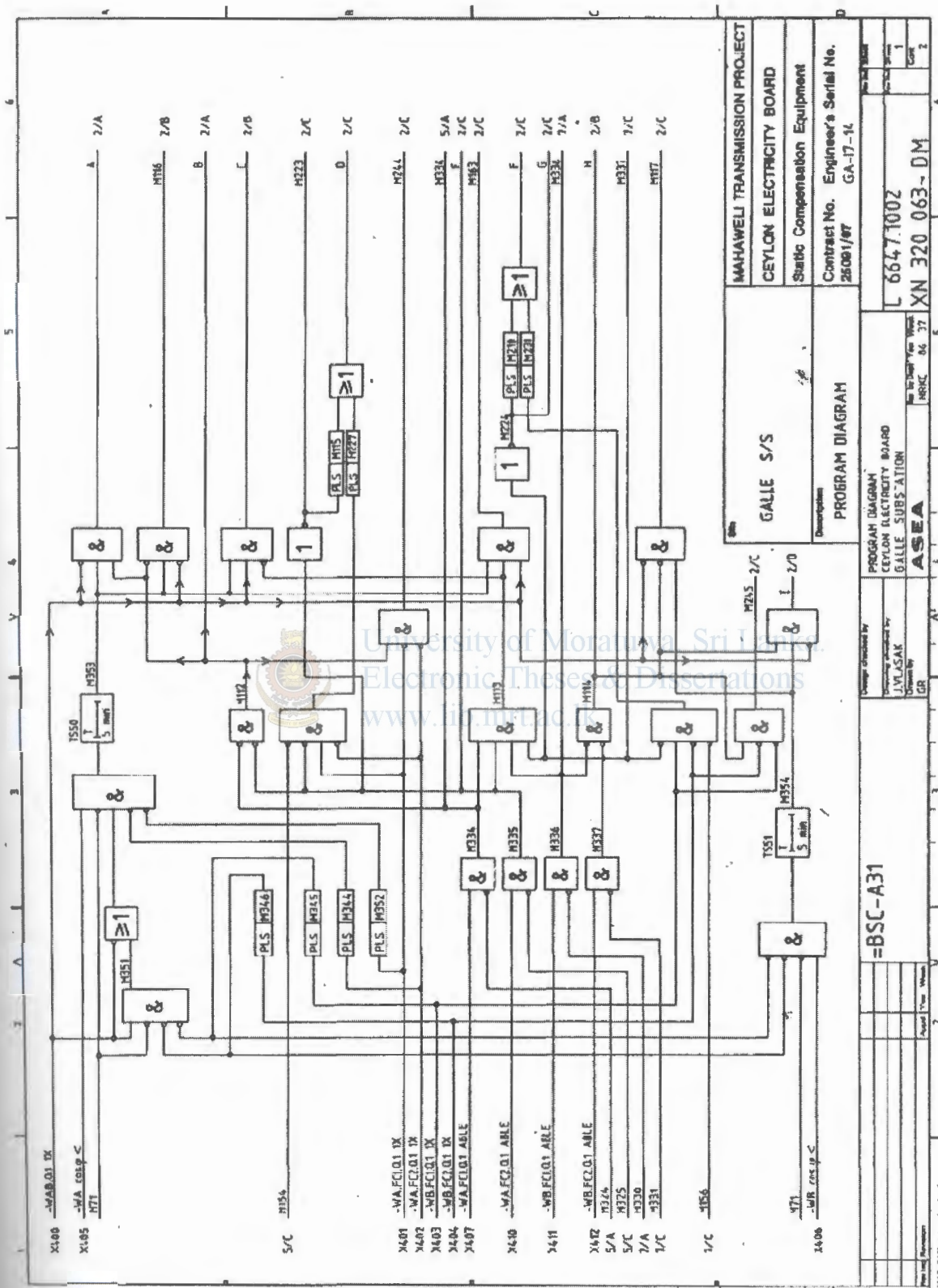


Figure 3.4.3 BSC bank control program structure embedded into the MasterPiece 020

MAHAWELI TRANSMISSION PROJECT CEYLON ELECTRICITY BOARD Static Compensation Equipment Contract No. Engineer's Serial No. 25081/87 GA-17-14	
GALLE S/S Description PROGRAM DIAGRAM	
Design Checked By J.V. ASAK University GB	Approved By M.B.C. 06. 37 Case 1 Case 2
PROGRAM DIAGRAM CEYLON ELECTRICITY BOARD GALLE SUB-STATION ASEA	
L 6647100Z XN 320 063 - DM	

Typical Operation Timeline

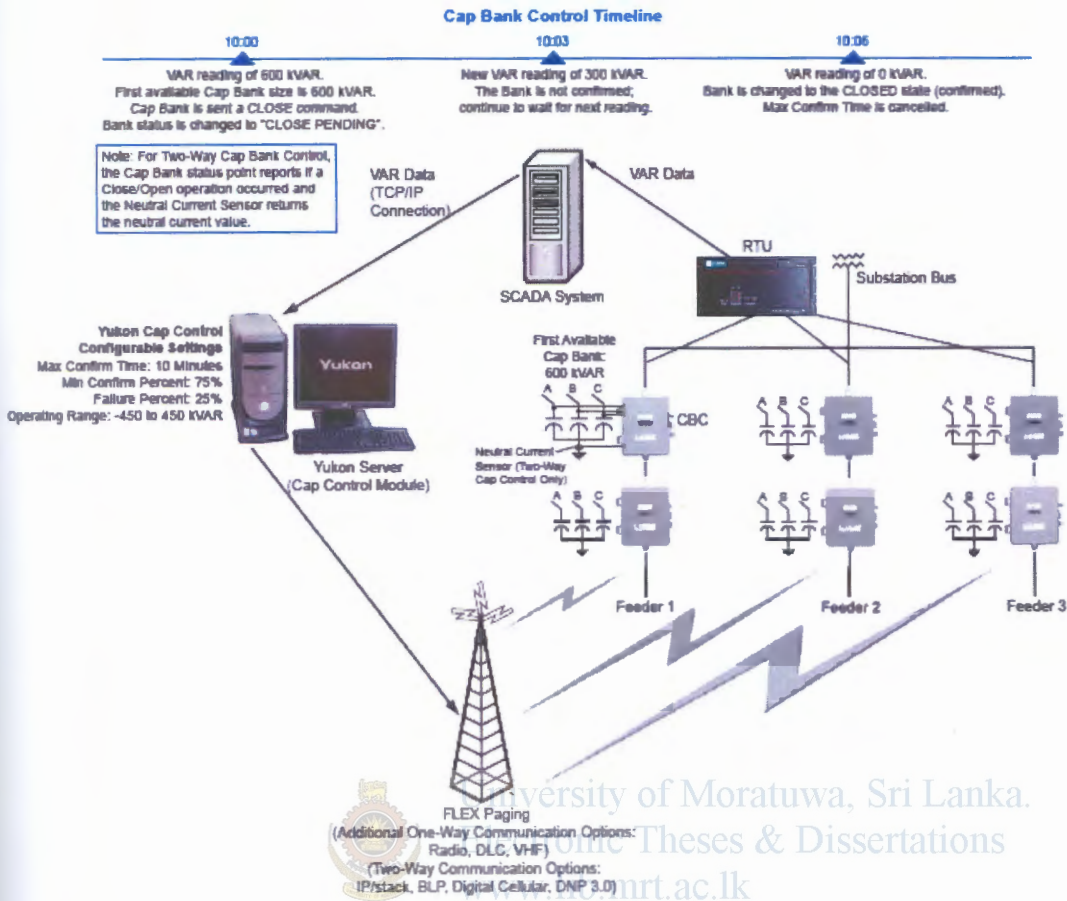


Figure 3.4.4 Modern overall system how the BSC banks controls using SCADA system and the server

4. Case study for Galle Grid Substation

A comprehensive study on the real system behaviour is an important necessity. Factors like convenience in fixing equipment, flexibilities in supervision etc, made the selection further easy. The load curves both real and reactive were compared with the system behaviour and found satisfactorily matching and representing the system as a whole.

The Galle GS is the one of the oldest substation in Sri Lanka. It consists of a two 132kV transmission line which comes from the Balangoda GS and two 132kV/ 33kV power transformer. Apart from that GS was introduced Static VAR Compensator (SVC) and four numbers of 5MVAR capacitor banks. Due to the radial nature of the system the voltage and VAR variation in the GS is substantial compared to other GSS in the country. However, studying the total system is practically impossible in a live system.

There are lots of operational difficulties for precise data collection and measurements in an operating system. However, a case study is a sufficient and satisfactory solution for a research like this. Such a sample study has to be selected to represent the total system as a whole. On the other hand, the duration during which the data collection and measurements is done, shall cover a substantial duration to represent the actual system variations. The general practice of such a study is to have one week duration.



University of Moratuwa, Sri Lanka.
Electronic Theses & Dissertations
www.lib.mrt.ac.lk

4.1 Substation details

Sub station capacity	- 2 x 30 MVA transformers
Incoming Transmission line	- Connected to Balangoda GS / Double circuit connection
No of feeders	- 8
No of capacitor banks	- 4 x 5 Mvar
Maximum average night peak	- 59MW +33Mvar
Minimum average load	- 27MW +16Mvar



4.2 Collection of the system data and measurements.

Following on line measurements were recorded for 7 days cycle at 132kV and 33kV voltage levels. Two on line data loggers were used for recording data, one at 33kV voltage level and.

- 33kV side measurements - MW and Mvar
- 33kV bus voltage
 - Power factor at 33kV incomer –Transformer 2
 - Tap position of on load tap changer – transformer 2

- 132 kV side measurements - MW & Mvar
- Power Factor at 132kV bus bar
 - 132kV bus voltage

Using these measured data computer simulation model was designed using PSCAD which is the simulation software used for the network simulations. Following the results of these simulations, the same measurements were done with all four capacitor banks forcibly connected to the system.

4.3 Measuring devices and data loggers

The following standard data logging equipment with their sensing equipment were used in measuring and recording the data.

- LEM Qwave Primium - power quality Analyzer
- Ellite 4 – Pholyphase power meter

Figures 4.1 and 4.2 show the equipment and their sensing devices used for the data logging and recording.

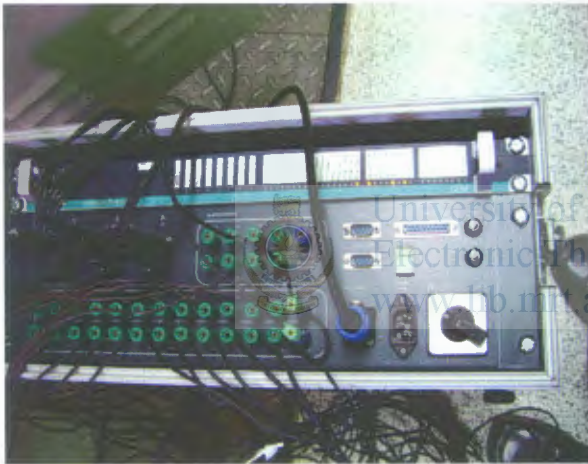


Figure 4.1 (a) Ben analyzer connected for 33kV measurements



Figure 4.1 (b) Analyzer connected for 132kV measurements

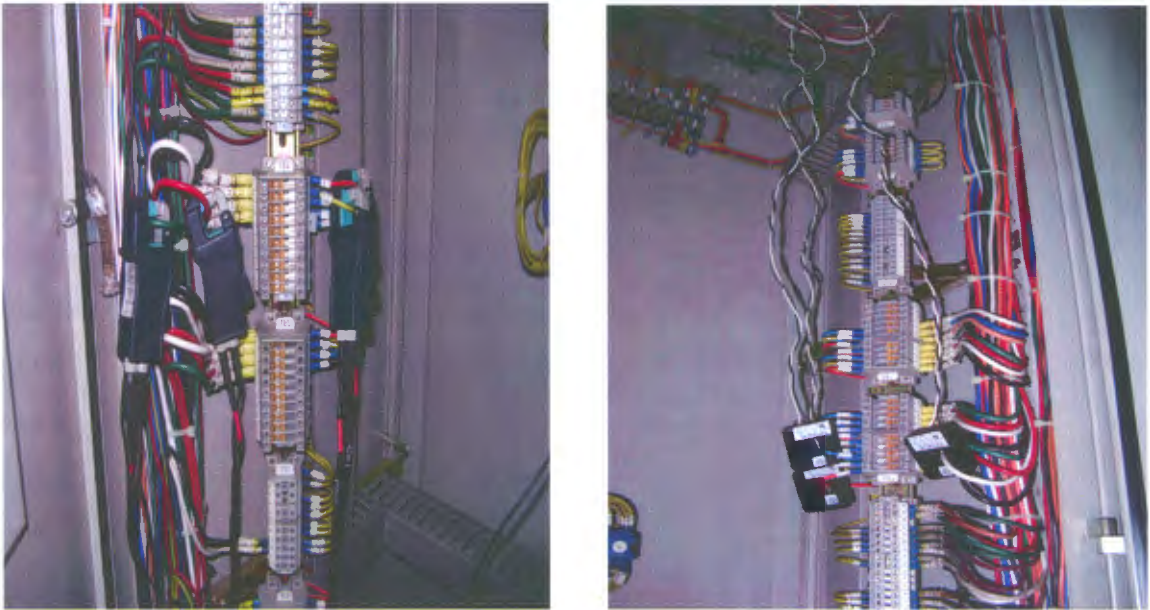


Figure 4.2 How the sensing equipments are connected

4.4 Variation of the power factor in the system

Figures 4.3(a) shows a regular daily pattern with two peaks. One peak can be observed around 5.00hrs in the morning, during the morning load peak. The second peak is during the night peak time at around 19.00 hrs. Figure 4.3(b) indicates one day time window of the variation of the PF.

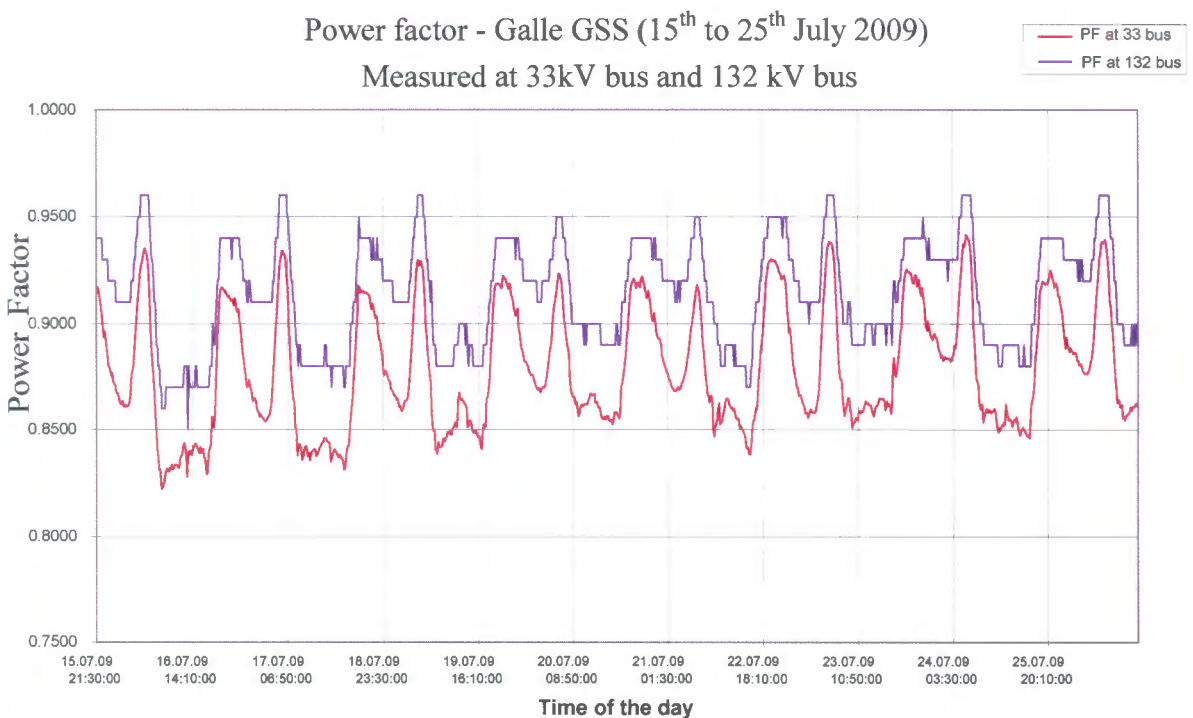


Figure 4.3 (a) Pattern of the power factor measured at 33kv & 132kV levels over total measurement period

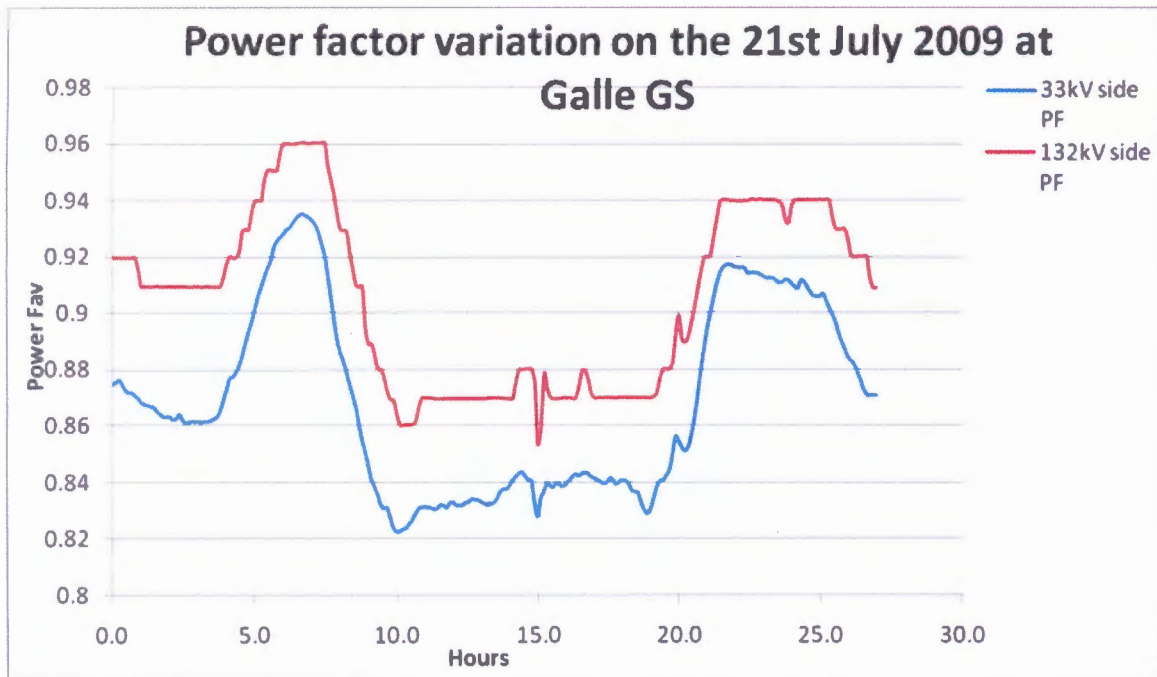


Figure 4.3 (b) Pattern of the power factors measured at 33kv & 132kV levels on 21st July 2009

4.5 Switching pattern of capacitor banks in the Substation

The behaviour of the capacitor banks in the substation with the present switching criteria was observed. The capacitor controller installed at Galle grid substation behaves as follows [7].

Controller - Masterpiece 20 ASEA controller
 Type - ASEA-095-222-A000 S

Switching ON criteria;
 If measured power factor ($\text{Cos}\phi_1$) < 0.95

Switching OFF criteria;
 If $\text{Cos}\phi_2 > \text{Cos}\phi_1 * (1 + \text{Hysteresis}/100)$

Where $\text{Cos}\phi_2$ = Power factor calculated from
 the actual $\text{cos } \phi$ value and set $\text{cos } \phi$ value
 Hysteresis = A setting value defined by user (set value
 10%)
 $\text{Cos}\phi_1$ = Set power factor (0.95)
 If the PF is below this value BSC bank will
 switch on according to the program set by
 Masterpiece 20

By observing the switching patterns, the following factors are noticed.

difference (i.e controller in independent mode of operation when the 33 bus coupler OFF)

- In the independent mode, two capacitor banks (one for each transformer) are in ON state through out the day. In the master slave mode, most of the time four capacitors are in ON position.
- In master slave mode, since four banks are ON in the mid night time, i.e. approximately after the night peak time and up to around 6.00 hrs morning, the sub station operates at a high leading power factor.
- In the real situation, during the period with lightly loaded lines especially in mid night, the line capacitances dominate and Ferranti effects causes high voltages at load ends. Addition of capacitors during such a period at substation makes the situation worst. Due to this, the control centre sometimes instructs to switch off the capacitor banks manually. Under such circumstances, due to operational difficulties, the operators switch off the controllers and hence all the banks are switched off. When operating a transmission network, this kind of leading reactive power compensation is also necessary. Although this is an un-economical situation as far as the sub station is considered, it is unavoidable. The situations like this once again prove that the power factor regulation is not the best switching criteria for CEB sub stations.
- Daily switching pattern shows that even at times where all four banks can be switched on, there are occasions where the controller switches only three banks especially during daytime. This may be due to the flat profile of the power factor during such periods. Both real and reactive power increases in the same proportion keeping the power factor unchanged. The controller does not consider reactive power increase if there is no decrease in power factor below limits.
- When the banks are switched off at nights manually to avoid voltage rises and again put into auto mode in the next morning, then the switching pattern disrupts and become even more uneconomical.

4.6 Uncompensated reactive power

The best operational criterion for the substation is to operate its loads close as possible to unity power factor as far as the losses are concerned. The data measured and recorded shows that there are occasions where reactive loads could be further compensated by the capacitor banks while they are not fully utilized, to minimize line and transformer losses. The breaker switched capacitors operates in steps and hence they give poor regulation. Low power factors whether lagging or leading gives same effects as far as losses are concerned. However, under the conditions where transmission network needs reactive power, operate with leading power factor can be considered.

The function of the on load tap changer (OLTC) is to adjust the LV bus voltage to its nominal value. When the load is high, the bus voltage is low due to IZ drop and tap changer raises its tap to high position to adjust the terminal voltage.

The voltage rise obtained by raising one tap position up, is 1.25 % of the voltage at the point of measuring. This is as per the specifications of the OLTC. At 33kV voltage this rise is about 0.4125 kV. The approximated percentage voltage rise given by switching one 5Mvar capacitor bank is given as $(kvar / kva) * X_t$ Where kvar = addition of reactive load, kva = transformer rating and X_t = transformer reactance in % [8]. When two transformers are in parallel, this value becomes 0.65% and the voltage rise is 0.2063kV at 33kV.

As these figures suggests, the effect of rise in one tap step is same as adding two 5Mvar capacitor banks when two transformers are paralleled or one 5Mvar banks when one transformer is connected. Tap changer adjusts the voltage by adjusting the transformer ratio but capacitor banks by reducing the reactive power through the transformers and transmission lines. Further it reduces the currents and hence the losses and release the equipment capacities. Therefore, the reactions of capacitor controller and AVR has to be optimally utilized [3].

Multiple Run Output File No cap banks							
Run #	Tap Position	HV Voltage	LV Voltage	Ph Ang_LV	LV_MW	LV_MVar	TF_HV_Current
1	.9250000000	74.78120511	33.50227824	-23.51500332	47.12524546	20.50556929	.1714195128
2	.9400000000	74.79557315	32.98062952	-23.51500149	45.68920959	19.87200561	.1560712497----- (B)
3	.9550000000	74.80926471	32.47476970	-23.51500464	44.27907683	19.26711830	.1609690167
4	.9700000000	74.82232163	31.98400256	-23.51500323	42.95096263	18.68921707	.1560980129 ----- (A)
5	.9850000000	74.83478258	31.50767152	-23.51499635	41.68126197	18.13673328	.1514445311
Multiple Run Output File 3 cap banks							
Run #	Tap Position	HV Voltage	LV Voltage	Ph Ang_LV	LV_MW	LV_MVar	TF_HV_Current
1	.9250000000	75.17429356	34.45411052	-6.171918169	49.83944434	5.389319552	.1621685425
2	.9400000000	75.17643599	33.91244808	-6.172074955	48.28522601	5.221766022	.1570913437
3	.9550000000	75.17849488	33.38725110	-6.171084037	46.80027560	5.060076609	.1522262048
4	.9700000000	75.18038156	32.87809638	-6.170808773	45.38412407	4.906991965	.1476188801----- (C)
5	.9850000000	75.18219740	32.38406964	-6.171620046	44.03061954	4.760750879	.1431963655

Table 4.6 Out of the simulation and actual reading

The Table 4.6 gives an extract from a output file showing simulation results for LV and HV voltage, MW and Mvar at LV side and transformer HV side peak currents under different tap positions with no capacitor banks and with four capacitor banks. (simulation results for conditions at 20.30 hrs on 23.07.09) If the condition starts from point (A) in table 4.6, It stabilizes at point (B) under tap changer control and ends at point (C) when capacitors are switched on by a voltage control scheme [3].

From (A) to (B), the results shows 3% voltage rise, 6% real power increase, 5 % reactive power increase and 4% current increase. From (A) to (C), there is a voltage increase of 3%, real power increase of 5% but the current and reactive power reduces by 6.6% and 71% respectively. This shows the effectiveness of both control loops when operates independently.

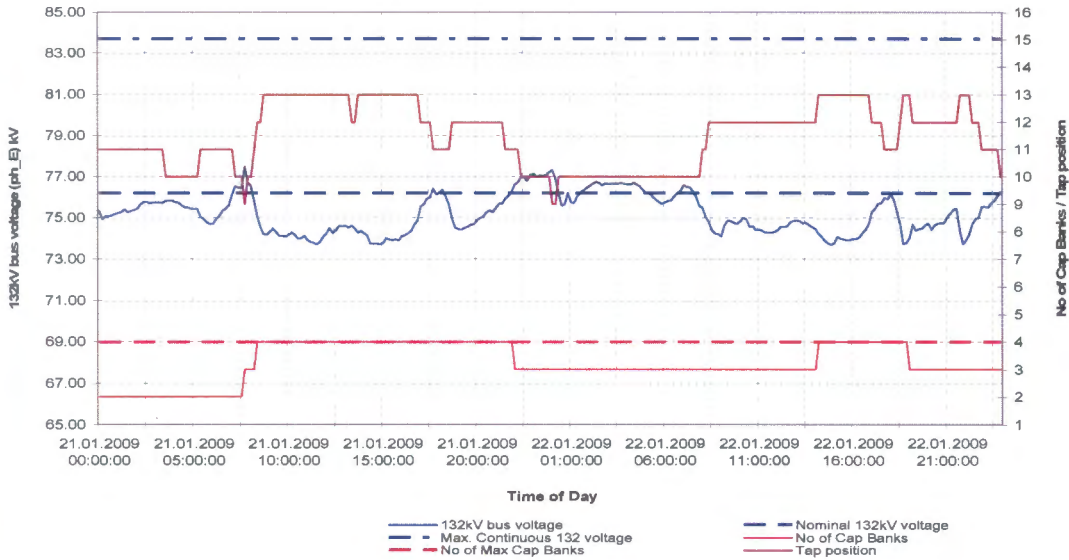


Figure: 4.6 (a) Pattern of tap position with no capacitor banks 21st & 22nd January 2009



University of Moratuwa, Sri Lanka.
Electronic Theses & Dissertations
www.lib.mrt.ac.lk

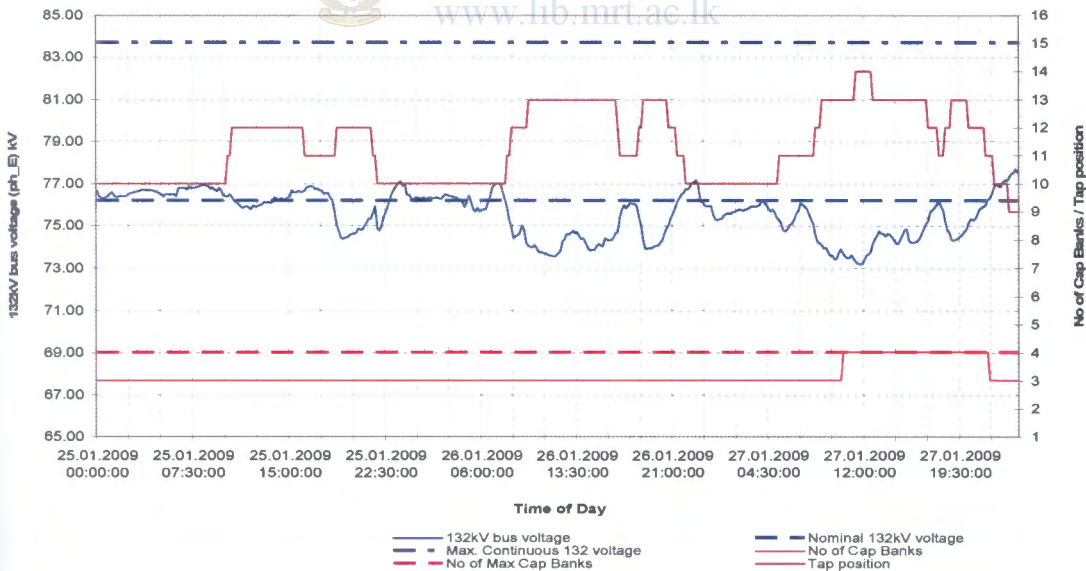


Figure: 4.6 (b) Pattern of tap position with no capacitor banks 25th & 27th January 2009

Figures 4.6 (a), and (b) shows the observations on the behaviour of the tap position in the absence of the capacitors. The number of capacitor banks that could be connected if the controller was in auto mode, is also indicated in the figures. The figures reveal that there is the possibility of operating the sub station at lower tap positions if the capacitor banks connected under the present criteria.

Appendix (B) compares the difference between the patterns of the tap position while having no capacitor banks and the same with the maximum number of capacitor banks. Since the voltage boost up by adding capacitors at 33kV side, the raise of transformer tap can be minimized.

4.7 Summary of the system study

By summarizing the results from the case study, it seems that the present switching criteria especially when the bus section breaker is in ON position dose not neither maximize nor optimize the use of installed capacitor banks in the selected substation.

Therefore, it is worth to consider different switching criteria that utilize the capacitor banks, than the existing utilization. However, under such circumstances, the effects to the system voltage, avoiding extreme over compensation that introduces losses due to leading power factor and other technical constraints have to be considered.



University of Moratuwa, Sri Lanka.
Electronic Theses & Dissertations
www.lib.mrt.ac.lk

5. System modelling and simulation

Studying the possibilities of optimising two controllers operations for solving the previously encountered problems have to be done in several steps. As discussed in the previous chapters, the first is to collect and record the system data and analyze them. Then by considering those results, simulation of the system under various operating scenarios and different capacitor bank combinations can be done. Therefore a suitably developed computer simulation model is very much essential. Using such a simulation various effects on the system due to switched capacitor banks and transformer AVR control can be studied. Followings are the areas that have to be studied as mentioned above.

- Voltage variation due addition of capacitor banks at the bus bar in which they are connected (Maximum voltage rise)
- Transformer OLTC and AVR to handle those voltage variations by changing tap position, when necessary.
- Changing the VAR flow through transformer when a tap operation occurs.
- Change in the VAR consumption of the transformer when tap operation occurs.
- A relationship between 132kV VAR flow and tap operation in the GSS
- Cost analysis considering the reduction of losses due to power factor improvement, release of system component capacities etc. and many others.

5.1 Software selection for modelling

There must be very good computer aided software needed for the system modelling of the substation this must be capable of modelling the substation for analyzing various system conditions by simulation. The software should have capabilities of both transient and steady state was needed for this purpose. Power System Computer Aided Design abbreviated as PSCAD [7] schematically construct a circuit, run a simulation, analyze the results and manage the data in a completely integrated graphical environment. PSCAD which is a tool used by many power system engineers, was used for modelling and simulations. PSCAD has a graphical user interface working along with an electromagnetic transient analysis program called EMTDC and a widely used software by power system engineers for power system studies [9].

All the power system software need some sort of license which means it has to be purchased from the software developer. It will cost much for obtaining licence but this PSSCAD provide free student version and the trial version for familiarisation. By using these two options the basic trials were done for simplest blocks with the free student version and later the complete model was developed with the trial version.



5.2 Components in Substation model

Main substation components such as power transformers, grounding zigzag transformers, circuit breakers, substation load, capacitor banks, tap changers, etc., are included in the model. Master library provide most of the basic components and if need some user defined component or sample model can be developed or designed.

Power transformers are taken as two winding transformers with the tap changer on HV side of the transformers. The actual transformer was approximated to the simplest form and p.u impedance was considered as an inductance only. The no load circuit was approximated with typical values.

The red squares represent the either side circuit breakers. The voltage and current measurement devices are also connected to the system. This represents a very good approximated components arrangement for the power transformer modelling. The developed module for the transformer is as given in figure 5.1

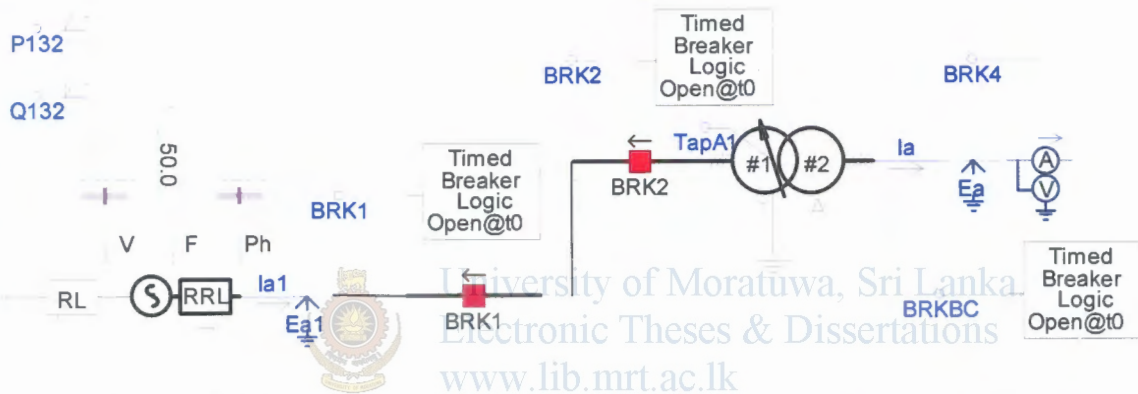


Figure 5.1 132kV system and Transformer module with the circuit breakers.

The modelling of the tap changer is represented as a HV to LV ratio changer to suit the real tap changer ratios. Nominal ratio of the transformer is 8 and this has to be taken as 1 in the PSCAD model. The tap changer at Galle is consisting of 20 taps with each 1.25% voltage difference. The tap changer is arranged as to control manually or change step wise in the multiple run mode, as below.

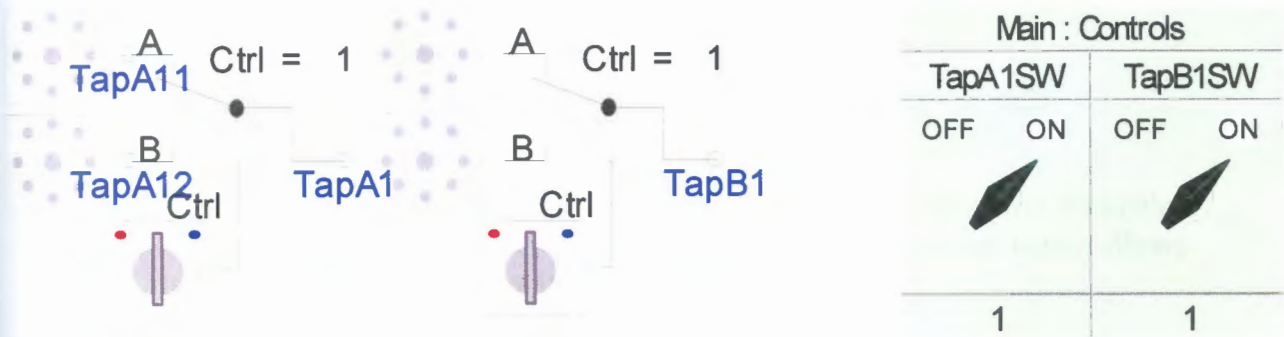


Figure 5.2: Modelling of the OLTC of the transformer

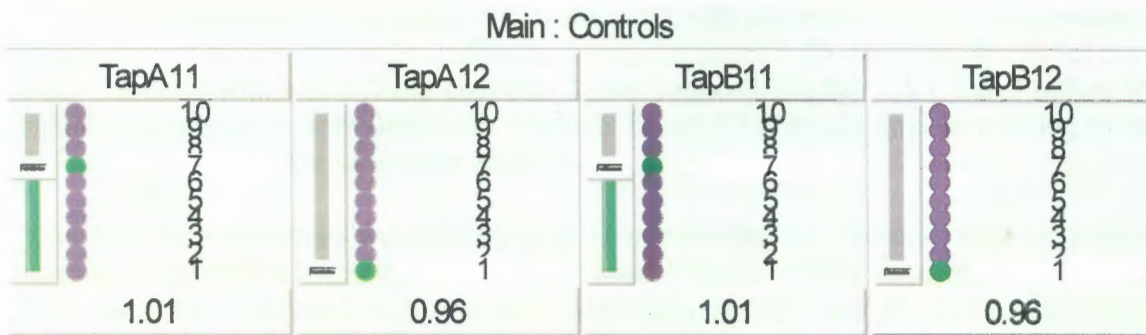


Figure 5.2: Modelling of the OLTC of the transformer.

Reducing the network beyond the 132kV bus basically depends on approximations. In any approximated representation, if frequency response analysis at the bus bar level is not expected then a simple Thevinin's modelling is sufficient.

A fixed load at a time is represented in the model and as a lumped load. This is specified with real and reactive power but the input values are real values so that input parameters from outputs of others modules could not be used in this module. Therefore, during multiple run functions, the second module with R and L values was used. R and L values are calculated as per the MW and Mvar values at different time slots.

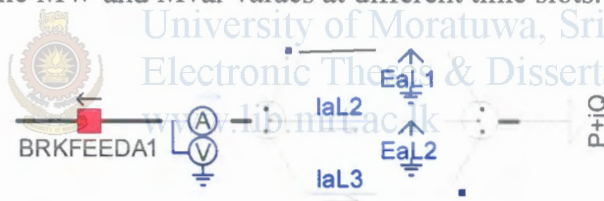


Figure 5.3 Load & load current measuring module

Breaker Switch capacitor Bank (BSC) with inrush and detune reactors are modelled with equivalent C and L values as in shown the diagram. Real capacitor bank configuration is ungrounded double WYE configuration, it is shown as its with the floating ground for the analysis.



Figure 5.4 Capacitor bank & Inrush/Detuning reactor module

The complete model is developed using above components for the Galle Grid Substation. The measurements of the V, Q, P, PF are done using meters available at master library. Galle Grid Substation in CEB system is shown in the Figure 5.4

5.3 Running the simulations

The simulation is run for measured data, real and reactive loads, tap positions, and voltage at source end and recorded data was compared with the actual measured data. This was done with and without capacitor banks connected to the 33kV bus. Further, the actual measurements were done with 5 minute interval but it was time consuming to run the simulations with the same time intervals.

Therefore the simulations were run only for 15 minute interval. The data were recorded at various stages for studying the system behaviour, Voltage, Power, Vars and power factor were recorded. The maximum and minimum loads at GSS was divided equally in 15 steps and time slots were allocated accordingly to execute the actual system with e model

5.3.1 Theoretical aspect of the simulation study

According to the theoretical calculations, the voltage rise at LV side of a transformer can be approximated as follows.

$$\text{Percentage voltage rise} = (\text{MVAR} / S_k)$$

Where kvar = addition of reactive load

S_k (MVA) = Short Circuit Capacity at the point of VAR injection

With present configuration, the maximum effective reactive power injection when either transformers in parallel, or transformers are independent, is 10Mvar (since each transformer is connected with two banks). Therefore, as per the above approximation, for this substation addition of full reactive load of 20 MVAR give a rise of about 1.47kV at 33kV bus voltage.

As indicated in **section 4.7**, the change of one tap position change the voltage by 0.0125 pu and this is about 0.4125kV at 33kV. The effect of rise in voltage over the nominal value due to addition of maximum capacitor banks can be handled with two tap positions.

5.3.2. Transformer var consumption

No load VAR drawn by the transformer ($Q_{\text{no-load}}$) = V^2/X_{shunt}

Noload current drawn by the transformer = 0.04Irated (from the test reports)

$$\begin{aligned} \text{Therefore } Q_{\text{no-load}} \text{ drawn by the transformer} &= 0.04 * \text{MVA}_{\text{tf}} \\ &= 0.04 * 30 \\ Q_{\text{no-load tf}} &= 1.2 \text{ MVAR} \end{aligned}$$

$$\begin{aligned} \text{Maiximum var drawn by the transformer at rated current (} Q_{\text{load tf}} \text{)} &= X_{\text{pu}} * \text{MVA}_{\text{tf}} \\ &= 0.1 * \text{MVA}_{\text{tf}} \\ &= 0.1 * 30 \\ Q_{\text{load tf}} &= 3 \text{ MVAR} \end{aligned}$$

$$\begin{aligned} \text{Total MVAR taken by the transformer itself} &= Q_{\text{no-load tf}} + Q_{\text{load tf}} \\ &= 1.2 + 3 \\ &= 4.2 \text{ MVAR} \end{aligned}$$

This value well suited with the simulation the simulation shows 4.46 MVAR consumption of VAR at rated current at rated voltage at tap position 08

5.3.3 VAR flow to the 33kV system when a tap operation occurs.

It will be noted from the simulation that when the OLTC change the turns ratio of the transformer which will draw more reactive power than delivering to the load. Therefore it is not worthwhile to allow drawing the Var through the transformer if it is available of BSC bank at 33kV bus to switch it on giving priority to the BSC bank controller. It reveals from the simulation model that two third of the Var is consumed by the transformer when it's tap position in maximum point.

From that we can deduce that when try to draw the Var from the system it will increase the number of the tap operation and on the other hand it will consumed the more Var further deteriorating the system voltage profile.

The sample calculation done on Var flow when tap operation occurs above shows that the simulation result is well within the calculation. The actual voltage drop and Var flow done by measurement too indicate the result are well suited with each others.

5



University of Moratuwa, Sri Lanka.
Electronic Theses & Dissertations
www.lib.mrt.ac.lk

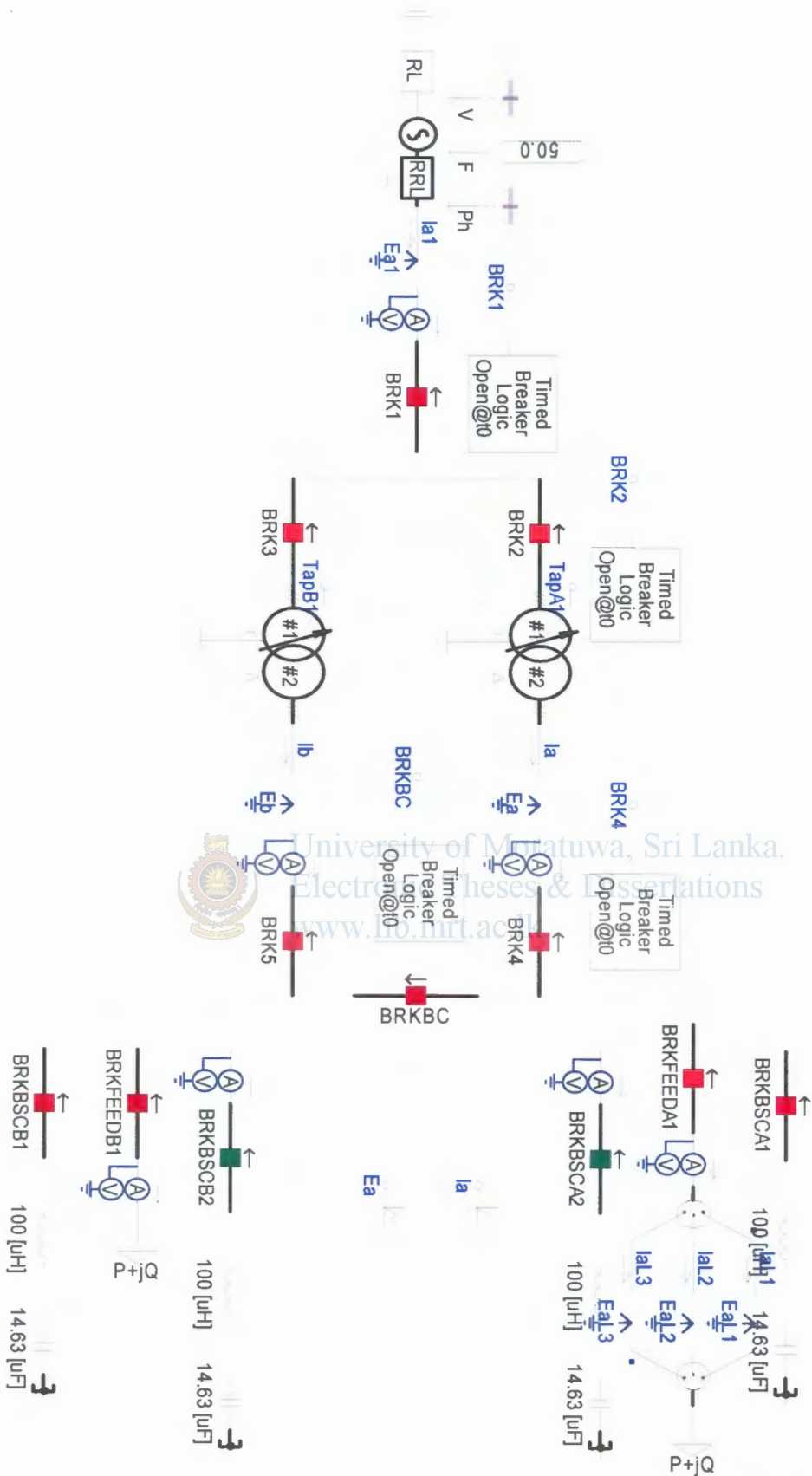


Figure: 5.5 Complete model for Galle Grid Substation



ed tap at rated V BSC are OFF (TA11 Tap 08)

Load	Qload	Q33kv	P33kv	V33kv	Q132kv	P132kv	Vmax	Vmin	PF angle
00000	2.666667	14.65727	25.3598	31.6009	19.3146	25.6573	33.33	32.67	37.0047
55556	2.855556	15.5879	27.145	31.5082	20.468	27.4421	33.33	32.67	36.3762
11111	3.044444	16.50565	28.9047	31.4158	21.6215	29.2016	33.33	32.67	35.806
66667	3.233333	17.4106	30.6392	31.3233	22.7746	30.936	33.33	32.67	35.28425
22222	3.422222	18.30293	32.3489	31.2306	23.9275	32.6459	33.33	32.67	34.8156
77778	3.611111	19.18271	34.0346	31.1377	25.0799	34.3315	33.33	32.67	
33333	3.800000	20.0502	35.6963	31.045	26.2318	35.9941	33.33	32.67	33.96505
88889	3.988889	20.9095	37.3346	30.9524	27.3832	37.633	33.33	32.67	33.5936
44444	4.177778	21.6118	38.95	30.8594	28.5338	39.2491	33.33	32.67	33.25
70000	4.366667	22.5796	40.5425	30.7667	29.6837	40.8424	33.33	32.67	32.9321
55556	4.555556	23.3987	42.1124	30.674	30.8328	42.4134	33.33	32.67	32.63785
41111	4.744444	24.206	43.6605	30.5811	31.9808	43.9623	33.33	32.67	32.3643
76667	4.933333	25.0015	45.1866	30.4882	33.1279	45.4895	33.33	32.67	32.1104
12222	5.122222	25.7856	46.6911	30.3955	34.2738	46.995	33.33	32.67	31.87425
							33.33	32.67	
47778	5.311111	26.5568	48.1741	30.303	35.4185	48.4793	33.33	32.67	31.65445
							33.33	32.67	
83333	5.500000	27.319	49.6361	30.2102	36.5619	49.9424	33.33	32.67	31.44935

Table 5.1. VAR and Voltage variation at fixed tap with varying load



University of Moratuwa, Sri Lanka
Electronic Theses & Dissertations
www.lib.mrt.ac.lk

Multiple Run Output File		All Caps			17.2 MW	9.6Mvar	
Run #	Tap Position	HV Voltage	LV Voltage	Ph Ang_LV	LV_MW	LV_MVar	TF_HV_Current
1	1.00000000	83.07677576	36.75584001	31.20543495	21.37469995	-12.92286353	1051738480
2	1.01500000	83.06745081	36.30956725	31.20486137	20.74670260	-12.54229066	1020880757
3	1.03000000	83.05852515	35.77920687	31.20529453	20.14495215	-12.17835456	9915548672E-01
4	1.04500000	83.04997852	35.26412698	31.20548649	19.56857477	-11.83015222	9635954657E-01
5	1.06000000	83.04179021	34.76367327	31.20524509	19.01855912	-11.49667914	9365258054E-01
6	1.07500000	83.03394569	34.27726921	31.20527452	18.49070244	-11.17708379	9107116275E-01
7	1.09000000	83.02642465	33.80428815	31.20504308	17.98304192	-10.87145676	8860031208E-01
8	1.10500000	83.01920234	33.34420109	31.20536777	17.49747653	-10.57650063	8622601926E-01
Multiple Run Output File		All Caps			17.2 MW	9.6Mvar	
Run #	Tap Position	HV Voltage	LV Voltage	Ph Ang_LV	LV_MW	LV_MVar	TF_HV_Current
1	1.00000000	82.55300216	35.39586479	-29.22323451	19.81771014	11.11511467	1024325584
2	1.01500000	82.55901578	34.96615854	-29.22323752	19.24149323	10.79224345	9946125022E-01
3	1.03000000	82.56476859	34.46138792	-29.22324054	18.68997372	10.48319655	9661804273E-01
4	1.04500000	82.57027546	33.97092109	-29.22324356	18.16176419	10.18719813	9389568724E-01
5	1.06000000	82.57555021	33.49416116	-29.22324657	17.65557300	9.903525888	9128743988E-01
6	1.07500000	82.58060570	33.03054389	-29.22324957	17.17019652	9.631506662	8878702009E-01
7	1.09000000	82.58545392	32.57953542	-29.22325255	16.70451202	9.370512516	8638857295E-01
8	1.10500000	82.59010604	32.14063033	-29.22325551	16.25747125	9.119957137	8408663513E-01

Table 5.2 Multi mode run of the system with various tap switching capacitor banks.

The table 5.2 very clearly indicates that the high voltage side bus voltage at the present real conditions does not overstep the maximum continuous voltage of 83.715kV. The figure also shows that for maximum allowable HV bus voltage and for minimum load, the maximum LV bus voltage rise for same tap position is (36.7558-35.3959) kV equalling to 1.36kV.

The Figures 5.6 show the simulation results of how the voltage at the HV bus behaves with the number of capacitor banks, for 22nd of July 2009

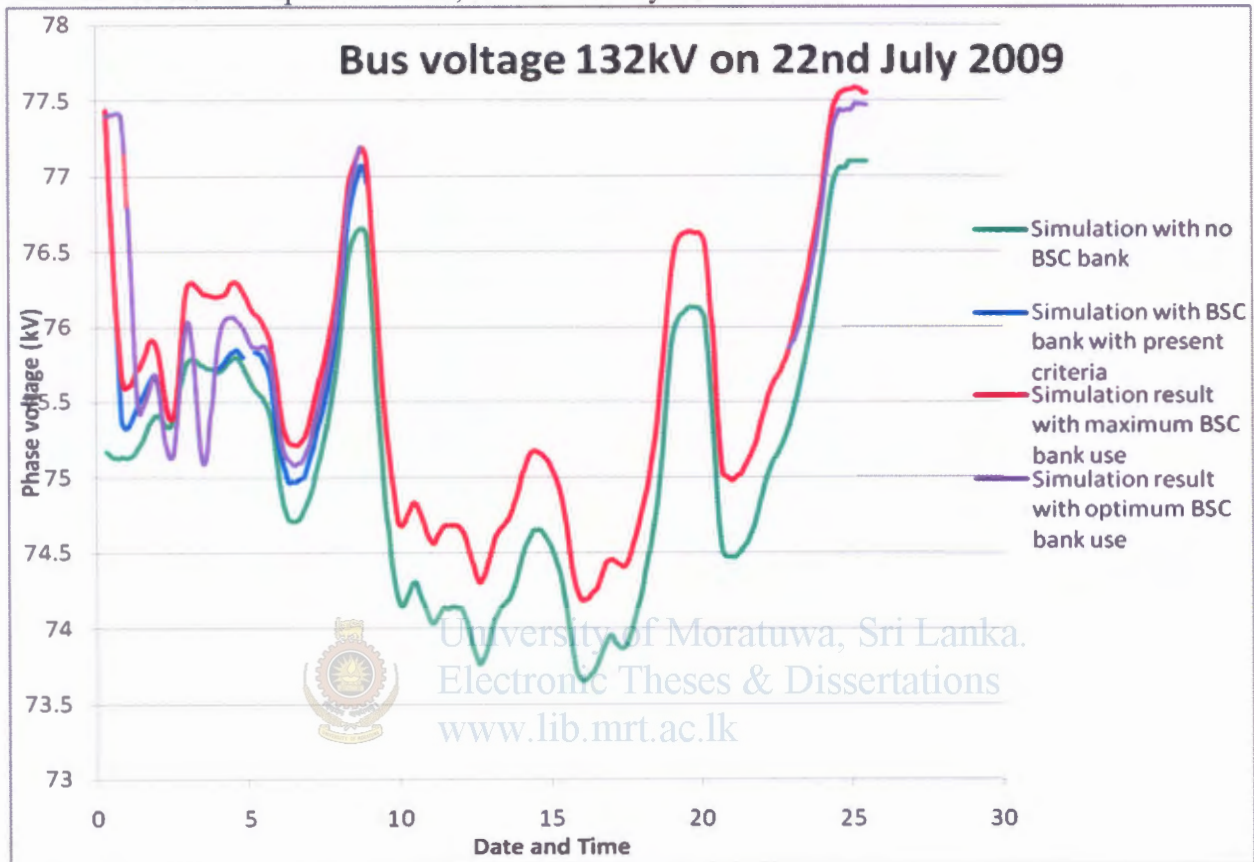


Figure 5.6 HV bus voltage variations under different cap bank configurations – Simulated data for 22nd July 2009

5.4 Data recoding and graphs

As mentioned in the previous paragraph, while providing the necessary reactive power support to the system at grid substation, if the switching of the capacitor banks is not based on voltage, i.e- voltage controlled switching, and then rise of voltages beyond the nominal values has to be maintained by the AVR and tap changer. For this purpose, the voltage at 33kV bus has to be within the controllable limit of the tap positions. Otherwise, the capacitor banks will be tripped by the over voltage relay.

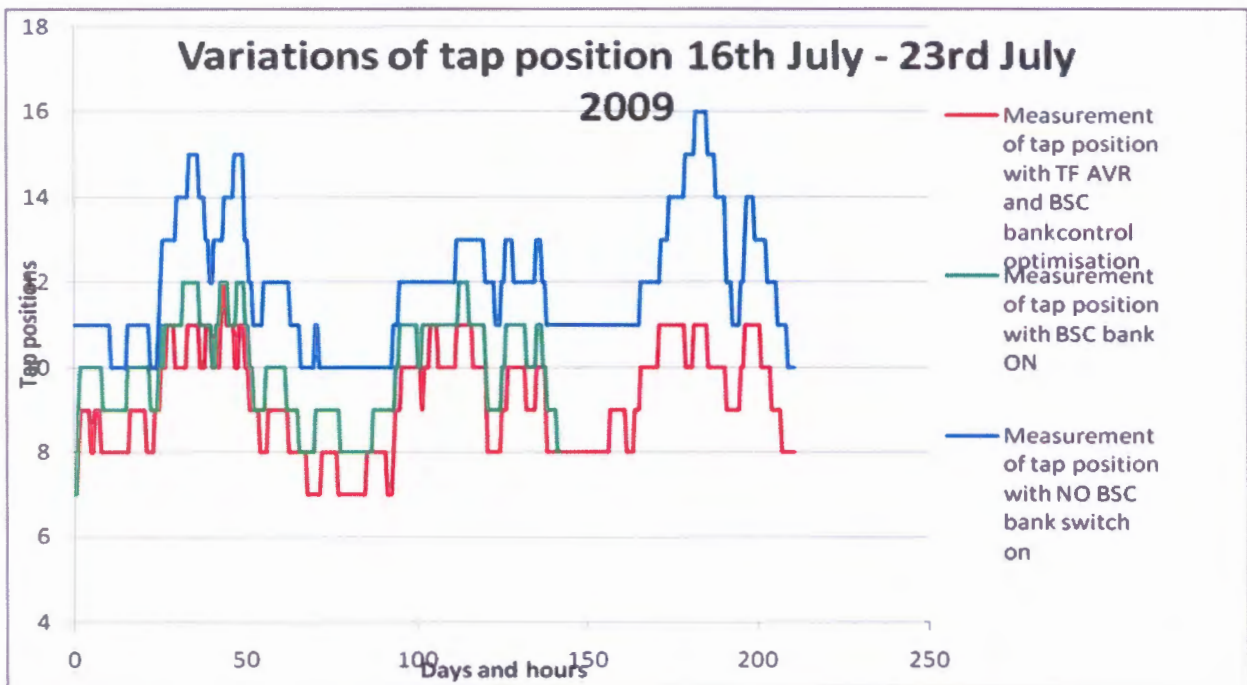


Figure 5.7 Tap position variation to give constant LV voltage– Simulation results

The figure 5.7 shows the simulation results of variation of the tap position under maximum var support. It indicates that the tap position remains around the nominal tap and voltage variation has been handled by the taps. A real time measurement also was done to track the varying tap position throughout couple of days with all capacitors connected and the data is shown in Figure 5.8.

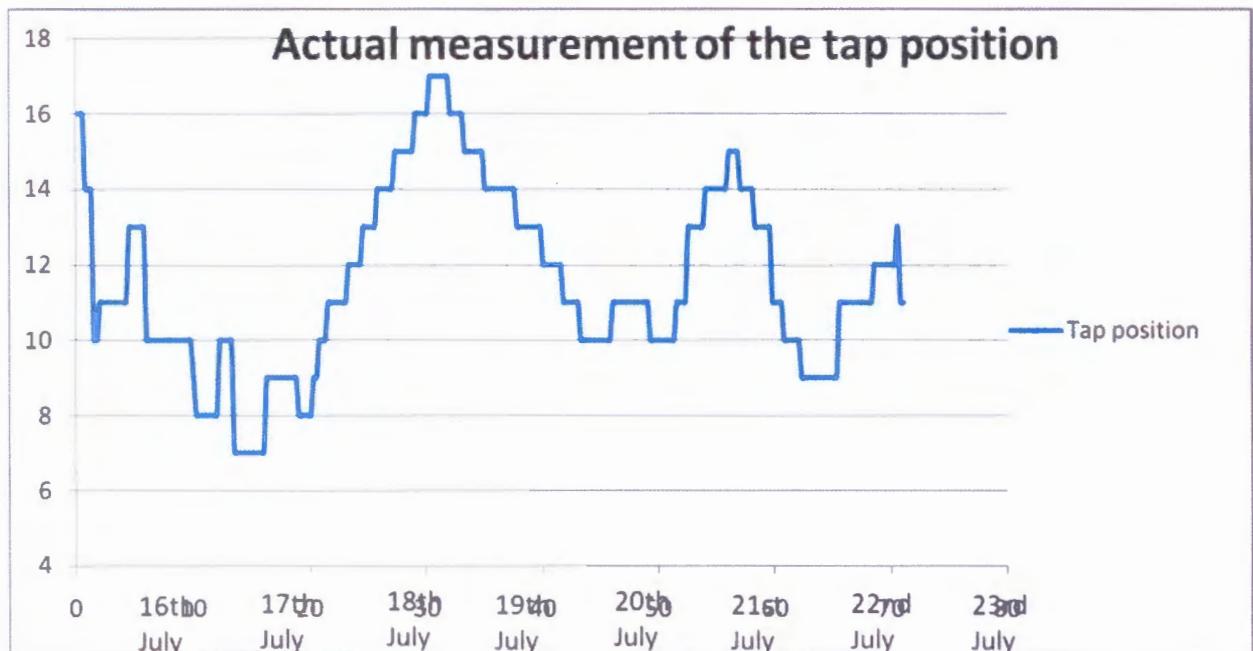


Figure 5.8 Tap position variations to give constant LV voltage – Actual measurements

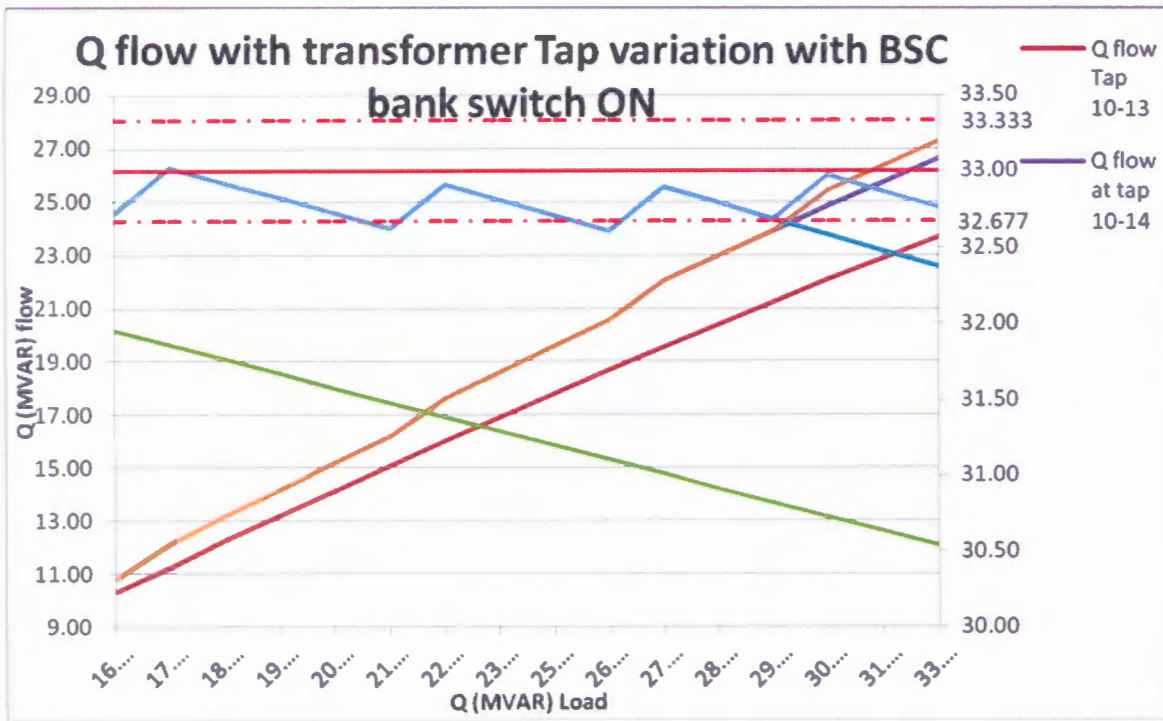


Figure 5.9 (a) Voltage and VAR flow of the system where.

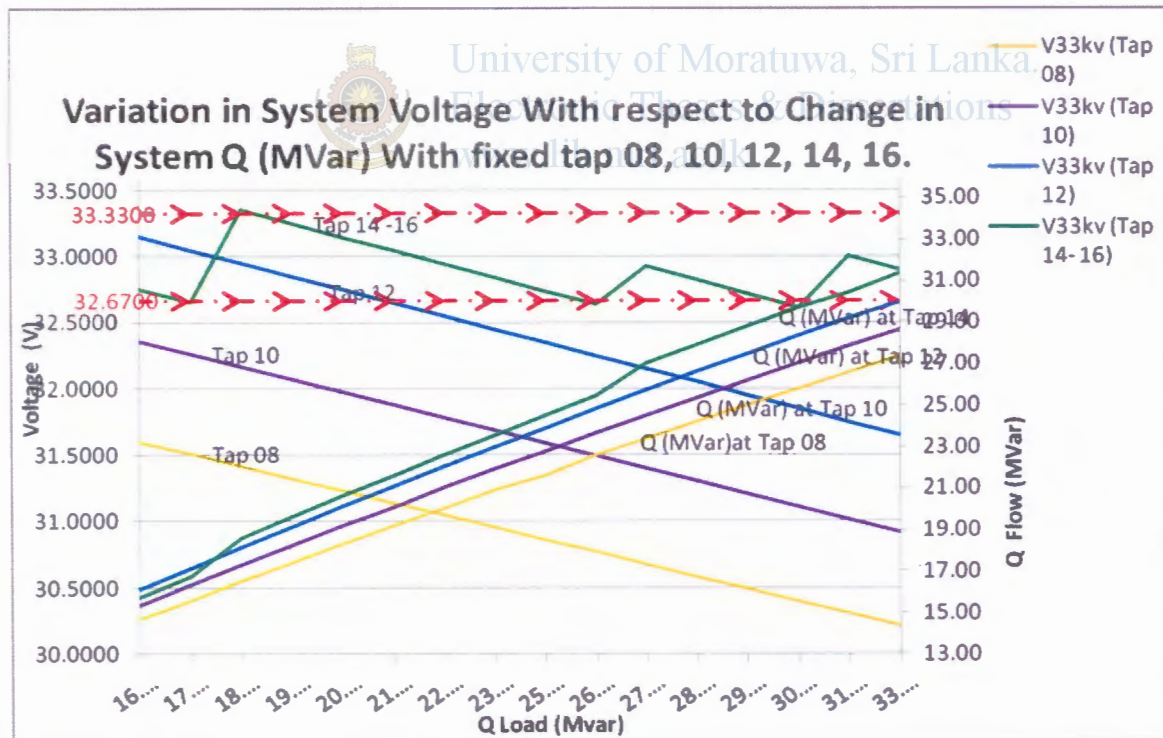


Figure 5.9 (b) Voltage and VAR flow of the system at varying tap with BSC bank switching ON

6. Design of new controller for BSC bank controlling

A system and method for coordinating shunt reactance switching in a system with a transformer having a primary voltage and a secondary voltage for supplying low voltage power to a load. Voltage and power meters are provided for measuring the primary voltage and the reactive power flowing to the load. A programmable logic controller receives as one set of inputs measurements of primary voltage and reactive power flowing to the load, and as another set of inputs, predetermined ranges establishing high and low limits for the primary voltage and the reactive power. Based on these inputs, the programmable logic controller connects or disconnects at least one shunt reactance to maintain the load voltage substantially constant.

6.1 Introduction of the design

Voltage fluctuations and variation on high voltage AC transmission system can be reduced by installing static reactive power generators (sometimes known as VAR generators) in the transmission Grid Substations (GSS). Voltage regulation is based on the fact that in an essentially inductive transmission line, transformer, voltage increases if capacitive current is injected into the line by, for example, connection of a shunt capacitor across the particular bus [5]. Alternatively, voltage can be decreased by connecting an inductor across the bus (or removing a previously connected capacitor). Static VAR generators may be switched across the bus using electromagnetic relay devices controlled by a predetermined timer or using a thyristor (or other semiconductor).

A problem facing many utilities is controlling shunt compensation on voltage buses especially where voltage is already regulated by on load tap change (OLTC) transformers. In an OLTC transformer, the low side line voltage delivered to the load is monitored and regulated by a conventional, fine tuning OLTC controller. Such a controller measures actual low side voltage, compares it with the desired value, and then adjusts the position where the load tap makes contact with the high side OLTC transformer coil, e.g., via a control signal to a motorized tap changer [10]. Typical OLTC transformers may have 16 or 32 tap positions, with each position being representative of some fractional portion of rated voltage. Thus, for example, a one position tap change on a 32 tap OLTC transformer would cause a relatively small bus voltage change as compared with the rated or desired output voltage.

OLTC transformers function well to effect small changes in voltage. However, large voltage fluctuations require switching of shunt reactance to ensure that sufficient reactive power is provided to the system, end-users and the customers such that secondary voltage can be held essentially constant. Since the OLTC controller is already monitoring and regulating the secondary distribution voltage, a shunt reactance control unit cannot also directly control that secondary distribution voltage [12]. As a result, most utilities typically follow a fairly rigid load cycle or power factor to estimate roughly when a reactance element, such as a capacitor bank, should be switched in shunt across the load to offset a decrease in the secondary distribution voltage from an increased load. After capacitor bank switching, the OLTC controller gradually adjusts the tap to return the low side voltage to the desired value. This rigid scheduling is far from optimal because it fails to accurately respond to actual system needs (as opposed to scheduled estimates) and to detect abnormal system conditions.

6.2 Factors that have been considered for designing the controller

The present method seeks to overcome these problems by flexibly coordinating the OLTC fine tune controller and shunt reactance switching. More specifically, it provides voltage and power regulation using a programmable logic controller for controlling shunt capacitor switching in order to attain the following exemplary objectives:

- (1) Maintain distribution and transmission voltages fairly constant;
- (2) Track station loading;
- (3) Complement the action of OLTC transformers;
- (4) Provide sufficient dead-band and time delays to avoid hunting; and
- (5) Detect and compensate for abnormal system conditions.
- (5). Measure the VAR consumption of the transformer at various loading conditions with respect to the tap operations
- (6). Measure the VAR generation by the transformer when a tap operation occurs

In one embodiment, the present study provides a system for coordinating shunt reactance switching in a power distribution substation which includes a transformer having a primary voltage and a secondary voltage for supplying low voltage power to a load. Voltage and power sensors are provided for measuring the primary voltage and the reactive (or real) power flowing to the load. A programmable logic controller receives as one set of inputs measurements of primary voltage and reactive (or real) power flowing to the load, and as another set of inputs, predetermined ranges establishing high and low limits for the primary voltage and the reactive (or real) power. Based on these inputs, the programmable logic controller connects or disconnects at least one shunt reactance across the load to maintain the load voltage substantially constant.

This is particularly well suited to coordinate shunt reactance switching with OLTC transformers. An OLTC controller monitors the secondary voltage and adjusts the tap contact position in response to secondary voltage variations. The present study is also applicable as well to power transmission lines for delivering secondary voltages to a variety of loads. In both environments, a primary voltage of the OLTC transformer or the transmission line is monitored along with reactive power to a load.

The programmable logic controller uses the predetermined ranges for primary voltage and reactive power to determine a dead-band range of operation in which no reactance switching is necessary. The dead-band range and switching determination are based upon a mathematical model formulated as a function of

- (1) Primary or high side voltage and
- (2) Power (P or Q) flowing to the load.



If that function exceeds a calculated dead-band range, an error is calculated, and integrated, over time. When the integrated error exceeds a preset value, reactance switching occurs.

The present study also includes a method for coordinating shunt reactance switching with an OLTC transformer is having a high voltage side and a low voltage side for supplying low voltage to a load including:

- (1). Adjusting the position of an adjustable tap contacting windings on the high voltage side in response to variations in the low side voltage;
- (2) Measuring the high side voltage and reactive power flowing to the load; and
- (3). Switching at least one reactance in shunt with the load to maintain a substantially constant low side voltage based on the measurements in step (2) and on predetermined ranges for the high side voltage and reactive power. The method may further include calculating a dead-band range of operation in which no reactances are switched and outside of which reactances are switched [12].

The method further includes the steps of inputting predetermined ranges which include a minimum primary voltage, a maximum primary voltage, a minimum reactive power, and a maximum reactive power, and calculating a dead-band range of operation in which no reactances are switched and outside of which reactances are switched based on those predetermined ranges.

6.3 Brief description of the drawings and figures

These and other features and advantages of the study will be readily apparent in the art from the following written description, read in conjunction with the drawings, in which:

Figure 6.4 1 is an exemplary functional block diagram in which this method can be applied to an OLTC transformer with shunt reactances and load residing at physically separate locations;

Figure 6.4.2 is a graphic depiction of the mathematical model employed in the design of controller;

Figure 6.4.3 Shows the single phase arrangement of the schematic diagram.

Figure 6.5.1 is a flow diagram illustrating exemplary processes which may be used for carrying out the in the design; and

Figures 6.5.2 through Figure 6.5.10 are graphs showing the operation of the controller under various operating conditions.

6.4 Detailed description of the design

In the following description, for purposes of explanation and not limitation, specific embodiments are set forth, including particular circuits, circuit components, techniques, etc. in order to provide a thorough understanding of the process. However, it will be apparent to one skilled in the art that the study may be practiced in other related areas that depart from these specific details. In other instances, detailed descriptions of

well known methods, devices, and circuits are omitted so as to not obscure the description of the process with unnecessary detail. The study will be described in one exemplary embodiment in the context of an OLTC transformer in conjunction with Figure 6.4.1. OLTC transformer includes primary (P) and secondary (S) windings respectively, for stepping down a high primary voltage, for example, 132 kV to a lower secondary voltage, for example, 33 kV. An OLTC controller functions in the conventional way as described above to monitor the secondary distribution voltage to a load and to adjust the tap position of variable tap in order to maintain a substantially constant secondary voltage [13].

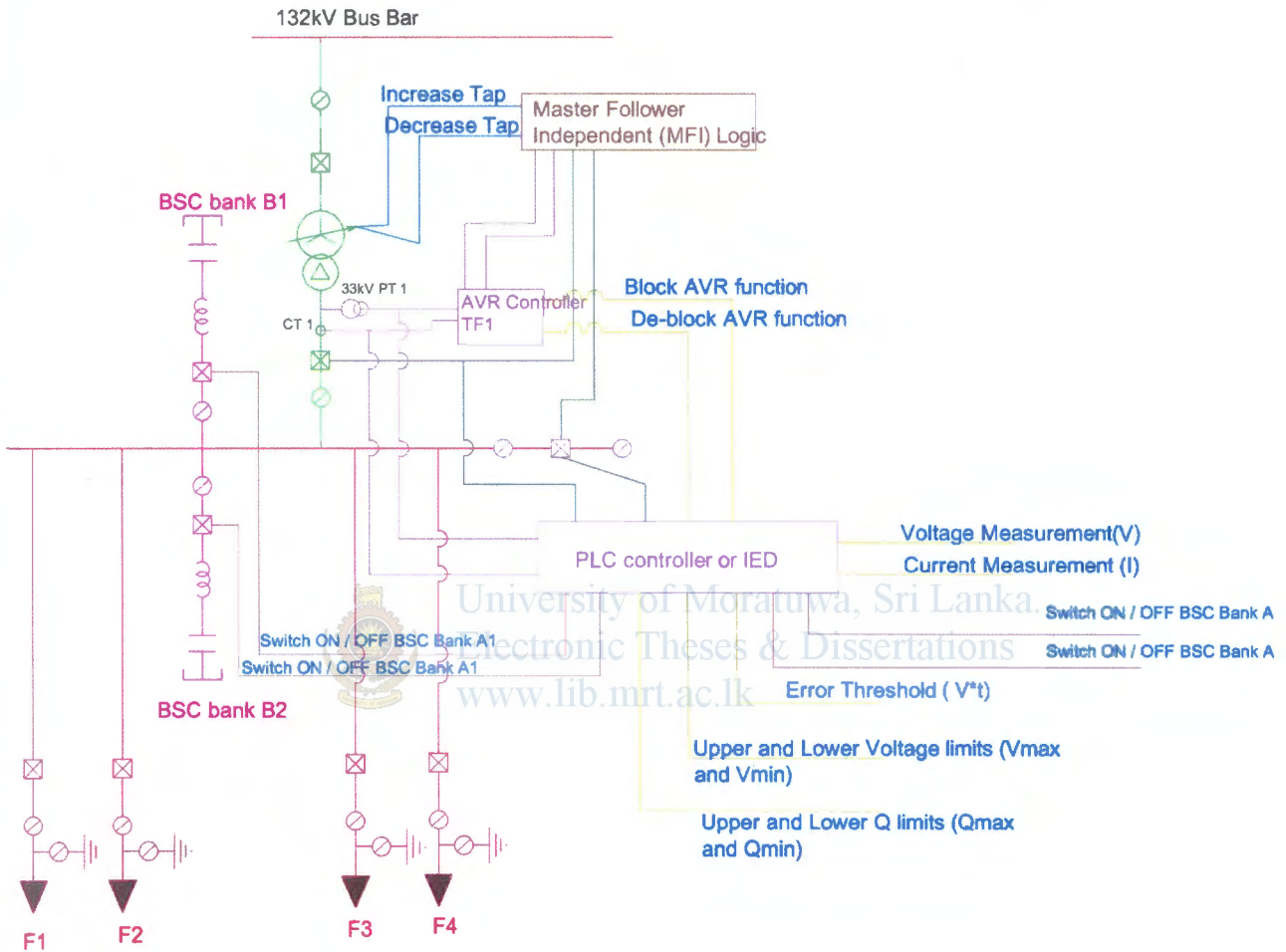


Figure 6.4 1 Circuit diagram and the controller arrangement of the system.

A voltage transformer is shunted across the primary winding in order to detect the primary voltage. A power sensor measures the reactive power flowing to load by measuring the voltage across the load and the current flowing to the load as indicated by Figure 6.4.1. Shunt reactances and (illustrated as capacitors) are connected in shunt to the load via circuit breakers. It will be appreciated that shunt reactances could be either capacitors or inductors and that controlling devices could be any type of circuit breaker or semiconductor (thyristor) switches.

A programmable logic controller receives a number of inputs including voltage readings from VT and reactive power readings from power meter. In addition, the programmable logic controller receives user inputs including an error threshold, upper and lower primary voltage limits, and upper and lower reactive power limits. Outputs of programmable logic controller include control signals to relay drivers for controlling the state of circuit breakers for switching the shunt reactances into or out of the network. It will be understood by

those skilled in the art that any number of shunt reactances may be included in the circuit depending on the installation.

Figure 6.4.1 also illustrates that the reactive devices may if desired be remotely located on a secondary network and may be remotely located from load. It will be understood by those that a variety of locations exist for the measurement devices, circuit breakers, and loads.

For each of the components described above, the controllers operates essentially to regulate the voltage to the load and to switch shunt reactances as necessary to ensure that the load voltage remains essentially constant. The primary "engine" of the study is programmable logic controller, e.g. a suitable programmable logic controller is available from the vendors. Current software for programming programmable logic control is also conventional, e.g. Ladder Logic software is available from vendors. It will, of course appreciate that other conventional programmable logic controllers and suitable software may be used to implement study as described below.

The process will now be described in conjunction with exemplary conditions graphically depicted in Figure 6.4.2.

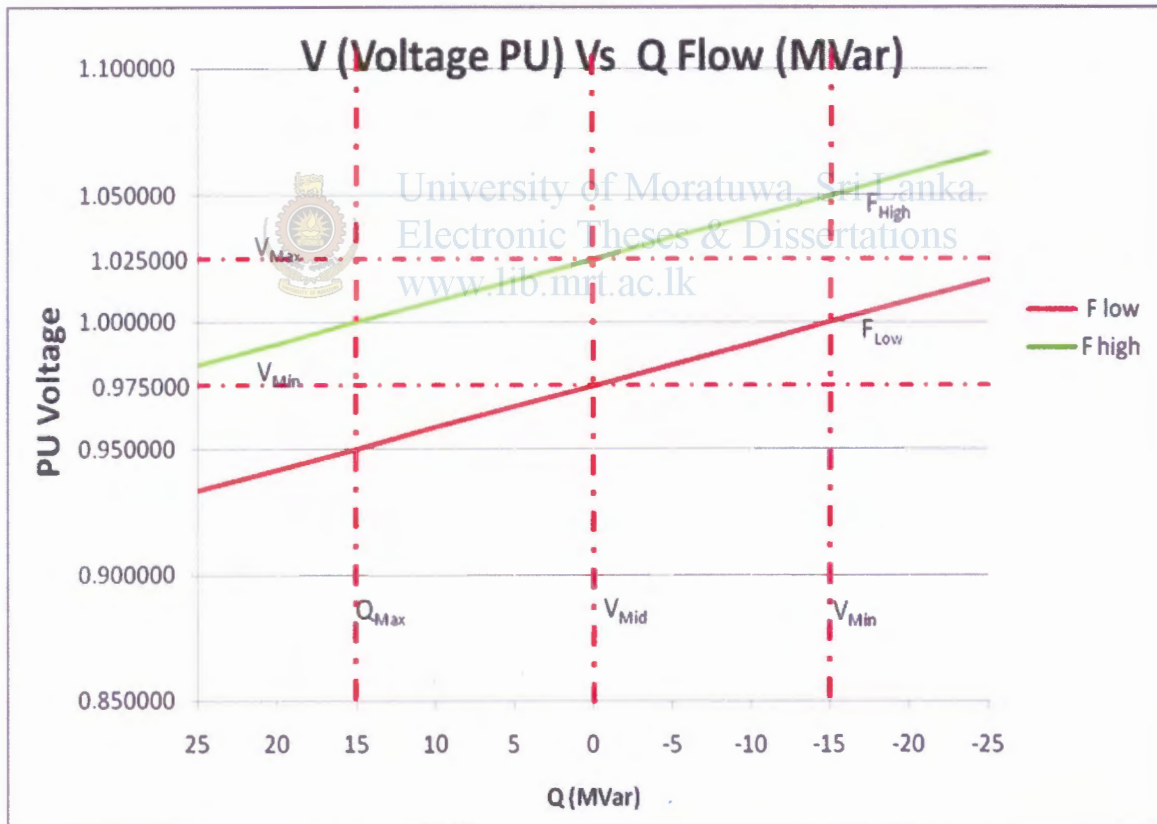


Figure 6.4.2 Mathematical model employed in the controller for decision

The controller determines when and if to switch the shunt reactances either into or out of the network to increase or decrease voltage to the load. However, in order to eliminate hunting and excessive reactance switching (either on or off), it is desirable to include a "dead-band" range around ideal operating voltage and power conditions. This dead-band range is defined as the region between the two solid diagonal lines shown in Figure 6.4.2

The present invention defines the dead-band range based on a decision variable $F(V, Q)$ which is a function of voltage and power flow to the load.

While the present study will be described below using primary voltage and reactive power, it is to be understood by those skilled in the art that other voltages including the secondary voltage as well as real power, could be utilized as the voltage and power parameters, respectively.

Initially, an operator sets predetermined upper and lower limits for both primary voltage and reactive power flow. In the example shown in Figure 6.4.2, reactive power flow (in MVAR) is recorded on the vertical scale with $Q_{\min} = -15$ MVAR and $Q_{\max} = 15$ MVAR. On the horizontal scale, normalized primary voltage (in per unit "pu") includes $V_{\min} = 1.0$ and $V_{\max} = 1.025$. Four midpoints 1-4 are determined for each side of a rectangle formed by the Q_{\min} , Q_{\max} , V_{\min} , and V_{\max} threshold limits (indicated by dashed lines). For example, midpoint 1 is the point at zero reactive power flow halfway between the upper and lower reactive power limits Q_{\max} and Q_{\min} .

Two parallel diagonal lines are determined which intersect midpoints 1 and 2 and midpoints 3 and 4, respectively. These two diagonal lines define the boundaries of the permissible deadband operation and are defined mathematically as

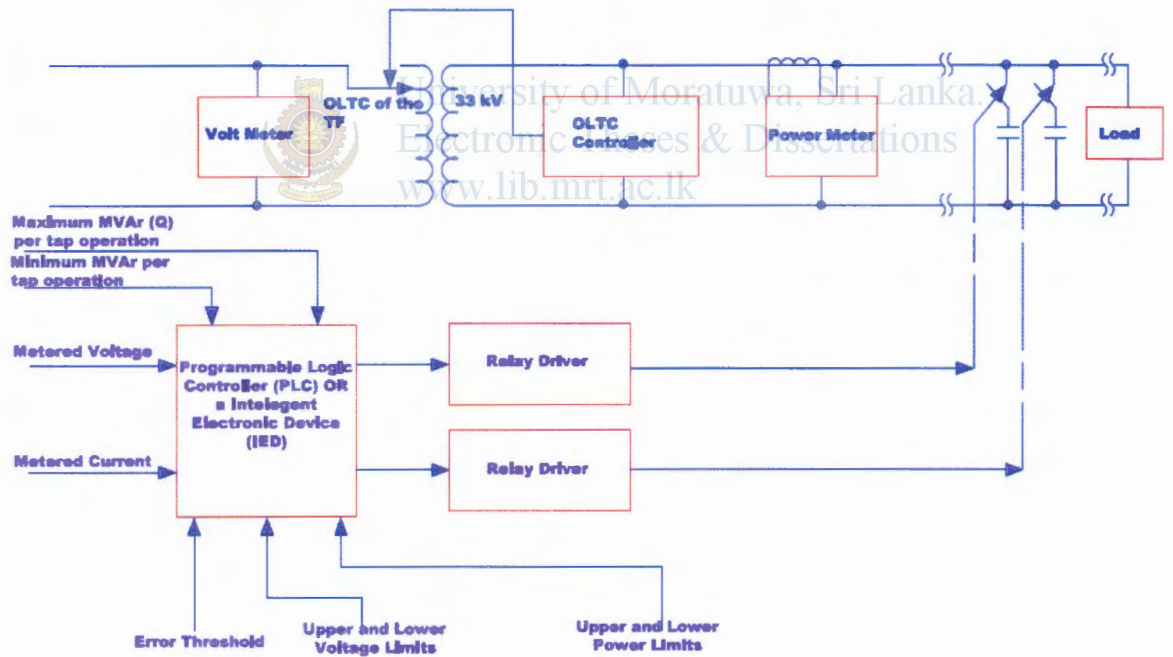


Figure 6.4.3 Shows the single phase arrangement of the schematic diagram

$$F_{\text{low}} = V_{\min} - kQ_{\text{mid}}$$

$$F_{\text{high}} = V_{\max} - kQ_{\text{mid}}$$

The gain or slope variable k is calculated as

$$k = \frac{(V_{\max} - V_{\min})}{(Q_{\max} - Q_{\min})}$$

and Q_{mid} is defined as

$$Q_{mid} = Q_{min} + \frac{(Q_{max} - Q_{min})}{2}$$

The decision function F determines the extent to which actually measured voltage and reactive power vary from the dead-band range defined by diagonal lines F_{high} and F_{low} . Thus, the actual operating point of the system at any point in time can be determined using the function

$F(V_{act}, Q_{flow}) = V_{act} - kQ_{flow}$ where:

V_{act} is the measured high voltage;

k is a gain parameter relating voltage and reactive power flow ranges;

Q_{flow} is the measured reactive power flowing to the load;

V_{min} is the low primary voltage limit;

V_{max} is the high primary voltage limit;

Q_{min} is the low reactive power flow limit;

Q_{max} is the high reactive power flow limit;

Q_{mid} is the midpoint of the reactive flow range.

To calculate the decision function X for the example shown in Figure 6.4.2 consider the following values:

$V_{min} = 1.00$ pu Volts;

$V_{max} = 1.026$ pu Volts;

$V_{mid} = -10.0$ MVAR;

$Q_{max} = 10.0$ MVAR;

$Q_{mid} = 0.0$ MVAR;

k equals $0.026/20.0 = 0.0013$ (pu Volts/MVAR);

$F_{low} = 1.000$ pu Volts;

$F_{high} = 1.026$ pu Volts.

In a first calculation programmable logic controller calculates values k , F_{low} , F_{high} based on input limit values Q_{min} , Q_{max} , V_{min} , V_{max} and the midpoint reactive power value Q_{mid} . Subsequently, based on the actual voltage and reactive power flow measurements from volt meter and power meter, programmable logic controller determines decision function

6.5 Sample calculation of the decision variables

$F(V, Q)$. For example, if the primary voltage is 0.99 pu and the reactive power flow is 5 MVAR, $X=0.99-(0.0013 \times 5.0)=0.9835$. Programmable logic controller then compares F to the F_{low} and F_{high} values to determine if F is outside the dead-band range of operation. Since 0.9835 is less than $F_{low} = 1.000$ programmable logic controller starts a timer to accumulate/integrate a voltage error.

An error for low conditions is defined as $ERR1=F_{low} -F$ and for high conditions is defined as $ERR2=F- F_{high}$. error values $ERR1$ or $ERR2$ are integrated over time and when the integrated value reaches a predetermined threshold, appropriate reactance switching is initiated. As shown in Figure 6.4.2, if $ERR1$ exceeds its threshold, a capacitor reactance bank is switched on.

Conversely, if $ERR2$ exceeds its threshold, the programmable logic controller switches a capacitor reactance bank into the network. The threshold value may be, for example, 1.0 pu Volt seconds to allow for gradual changes in load or voltages and for quick response in contingency conditions. In this instance, a ten percent (0.10 pu) voltage error causes reactance switching in ten seconds while a one percent (0.01 pu) voltage error requires one hundred seconds for switching.

Programmable logic controller only accumulates errors when F is outside of the dead-band range. If F returns inside the dead-band before a reactance switching signal is generated.

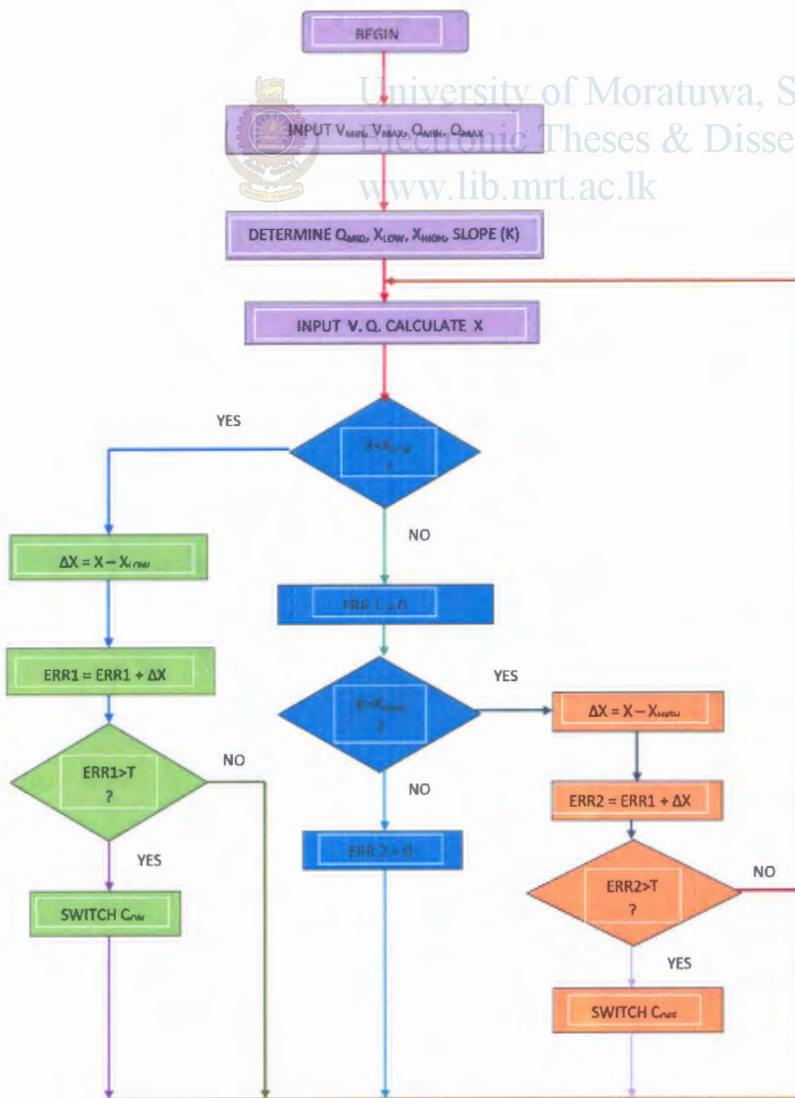


Figure 6.5.1 Flow chart illustrating the process of calculation in the

Figures 6.5.2 to 6.5.4 show the response to a gradual decline in system voltage from 1.04 pu to 0.95 pu over a 30 minute period. As system voltage drops OLTC controller reacts to maintain the secondary voltage within predetermined limits. When high side voltage drops below 1.0pu error starts to accumulate. When error reaches a threshold at 440 seconds a first shunt BSC bank is switched into the network.

As a results both primary and secondary voltage rise. As the system voltage drops further, a second BSC bank is switched ON at 640 seconds. At this point the however the secondary voltage exceeds an upper limits and OLTC controller reacts to decrease the voltage. At approximately 910 seconds reactive power flow drops below the specified Q_{min} with primary voltage depressed causing switching of the third BSC bank.

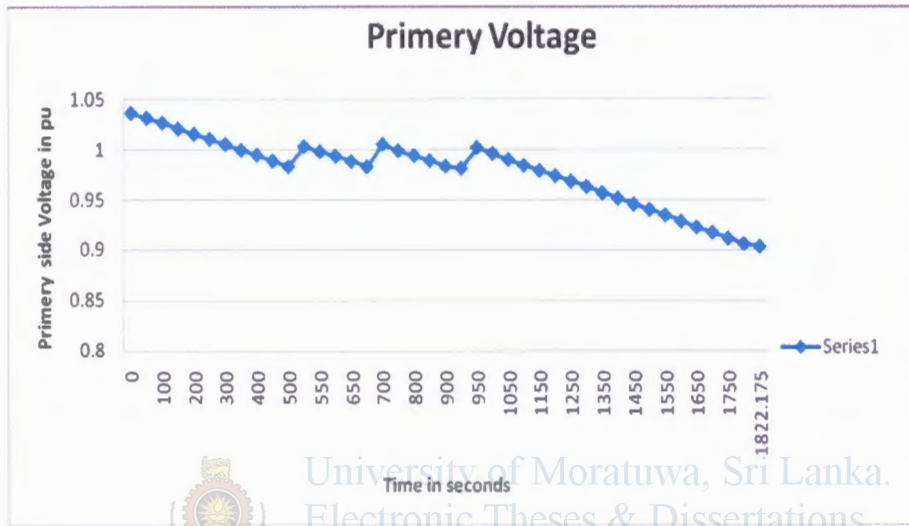


Figure 6.5.2 Primary system voltage variation with BSC bank ON (15MVAR)

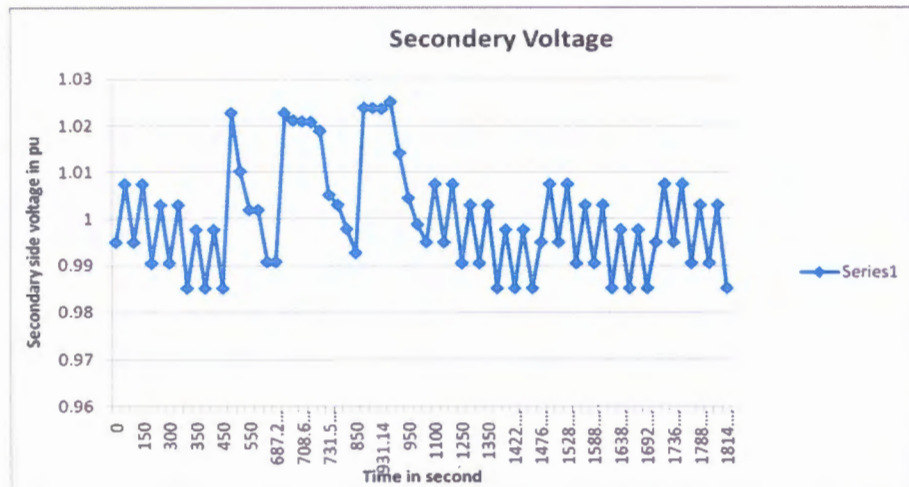


Figure 6.5.3 Secondary system voltage variation with BSC bank ON (5MVAR)



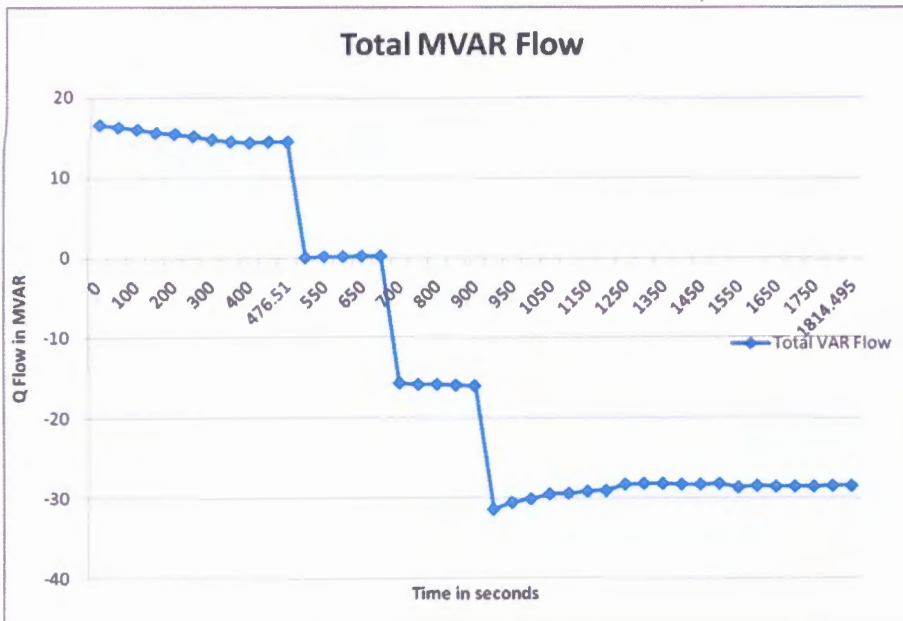


Figure 6.5.4 System MVAR flow through the transformers

Figures 6.5.5 to 6.5.7 illustrates the response to a sharp change in system voltage such as that caused by a system fault. The initial voltage is 1.05 pu which drops to 0.96 pu at 22 seconds. With the sharp drop in the primary voltage the first BSC bank is switched on immediately to increase the primary and secondary voltages

However these voltages do not reach within deadband limits, a second and third BSC banks are also switched on. The OLTC controller adjusts the secondary voltage at approximately 120 seconds. At 220 seconds, system voltage is stepped back up to 1.0 pu with OLTC operating in conjunction with removal of one BSC bank to reduce the secondary voltage.

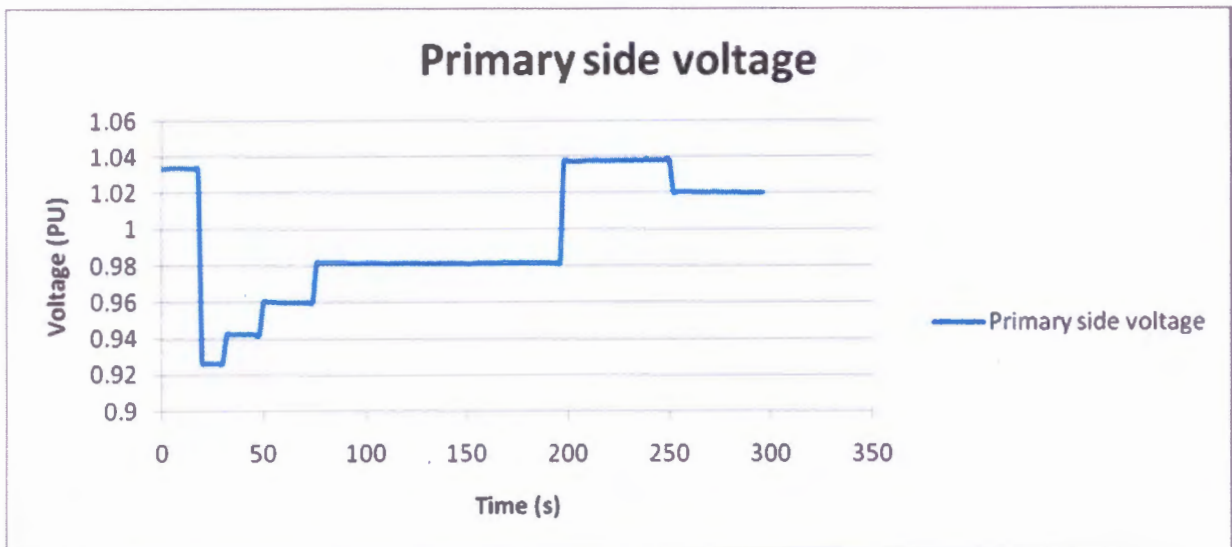


Figure 6.5.5 Sudden voltage dip existed in the primary side for 175 S period

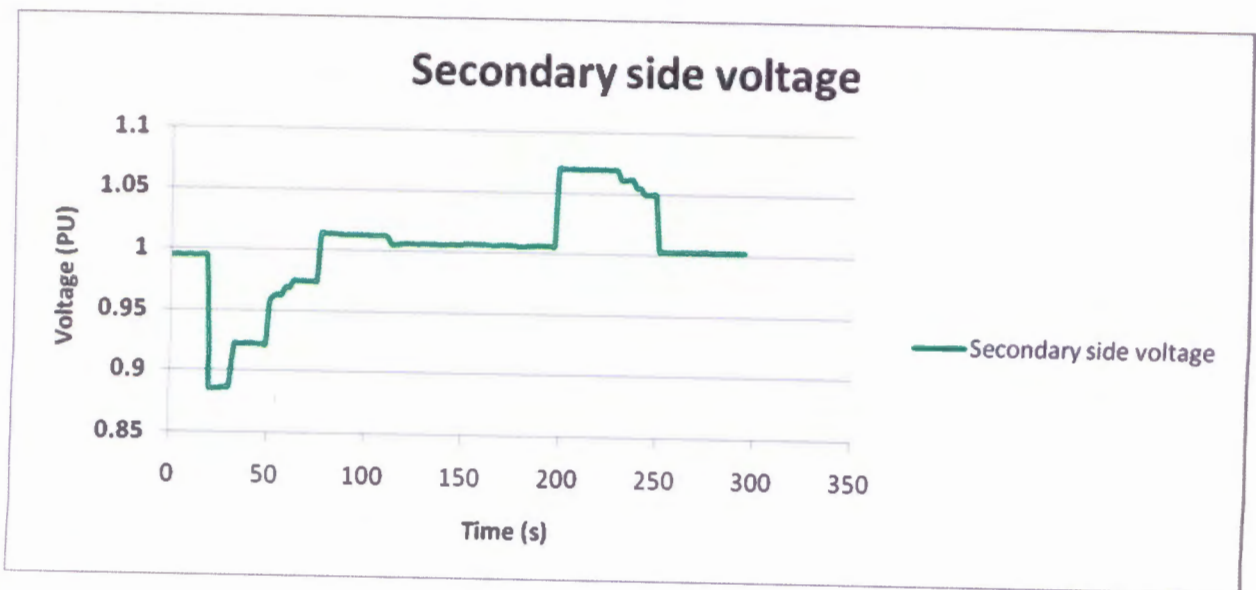


Figure 6.5.6 Secondary side voltage variation with BSC bank switch ON

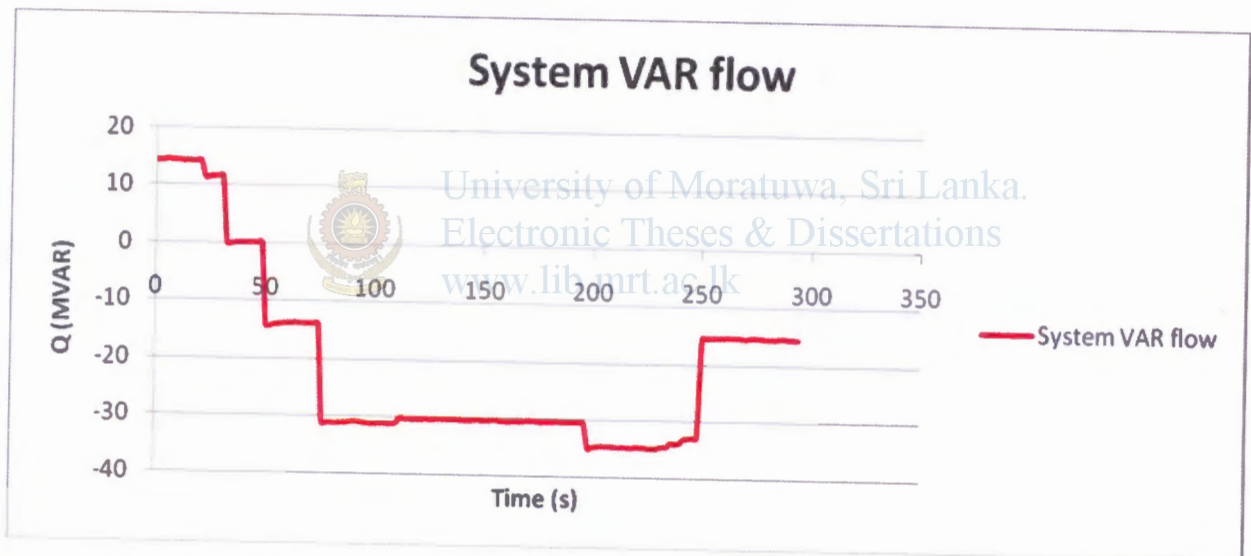


Figure 6.5.7 System VAR flow at that instance with switching the BSC bank

Figures 6.5.8 to 6.5.10 shows a steady increase in load. For the slow changes in system conditions, the OLTC controller acts initially and then at 2340 seconds, a first capacitor bank is switched on followed by a second capacitor bank at 3310 seconds to counteract load increases.

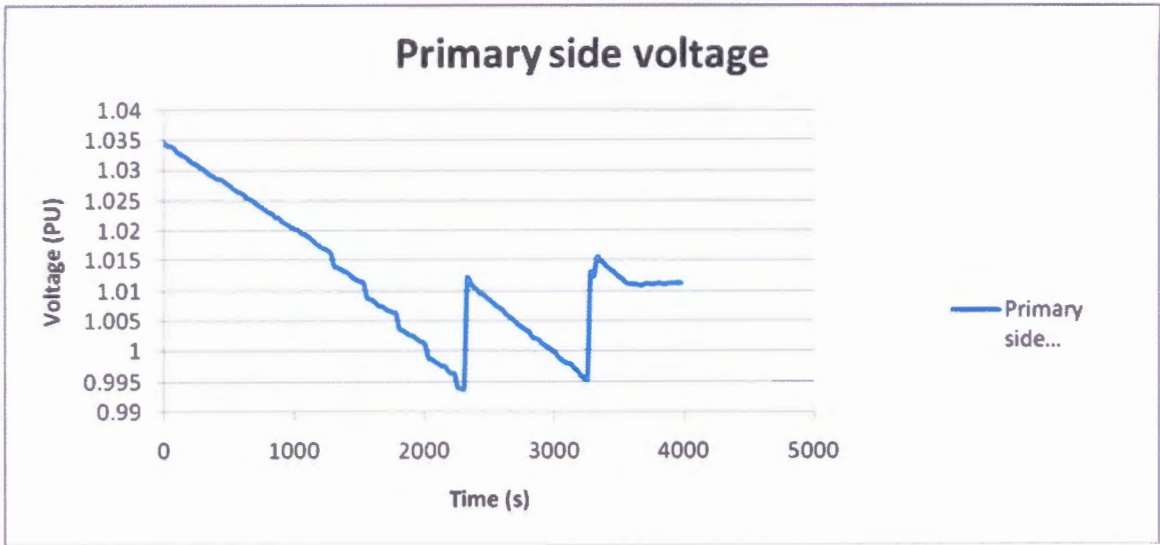


Figure 6.5.8 Primary side voltage variation with steady increase in load

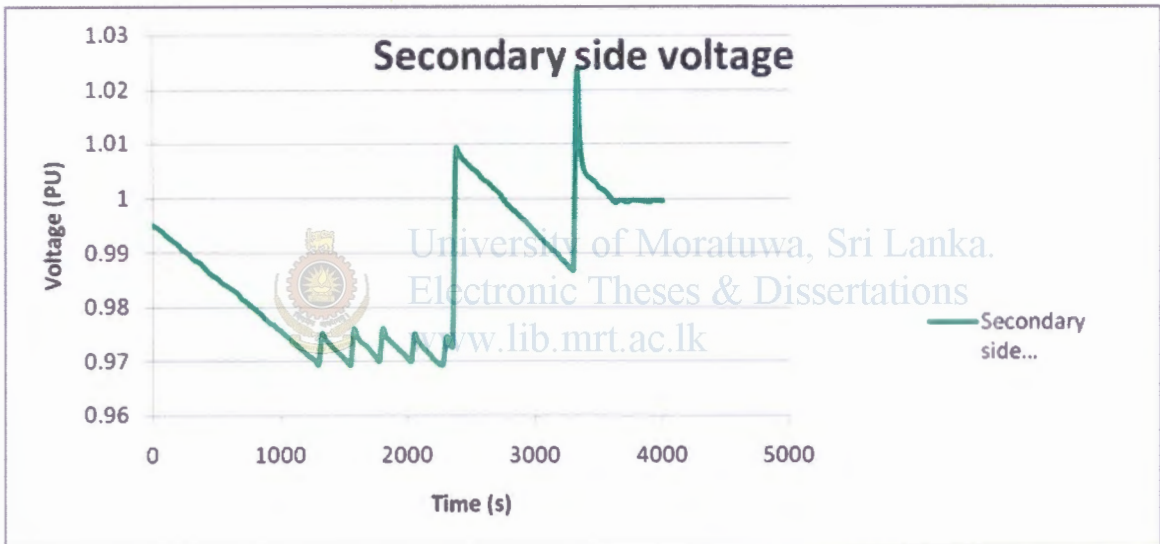


Figure 6.5.9 Secondary side voltage variation with steady increase in load

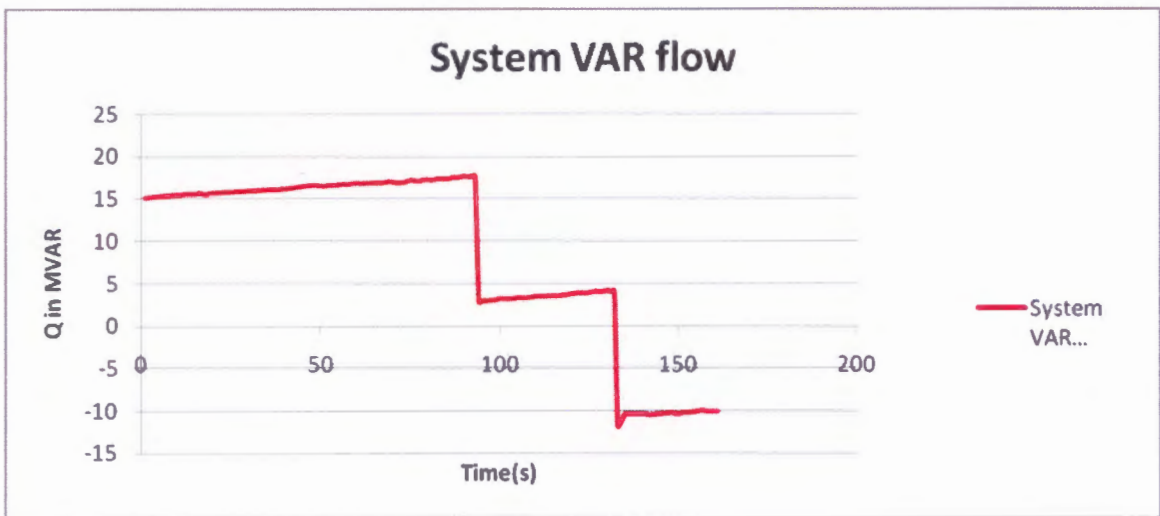


Figure 6.5.10 System MVAR flow through the GSS

In all three scenarios in Figure 6.5.2 to 6.5.10 switching of the BSC bank is well coordinated with the OLTC controller fine tuning adjustments. The coordinated system allows for flexible, programmable, and dynamic response to actual changing load conditions whether normal or abnormal, steady state or transient. Moreover, variable deadband response is programmable controlled simply by changing the user input to programmable controller.

While the study has been described in conjunction with what is presently considered to be the most practical and preferred, it is to be understood that this study is not be limited to the above but on contrary is intended to cover various modifications and equivalent arrangements included within the spirit and scope of the following section.

6.6. Factors that can be included in the design for further improvements

6.6.1 VAR controlling of the BSC bank

Capacitor bank switching based on reactive power requirements is a more flexible and natural means of capacitor control concepts. It adds a fixed amount of lagging reactive power into the system regardless of most other conditions. Since the reduction of losses and the capacity release directly proportional to the reactive current drawn, injecting the reactive power at substation bus level reduces losses beyond bus towards source including the transformer.

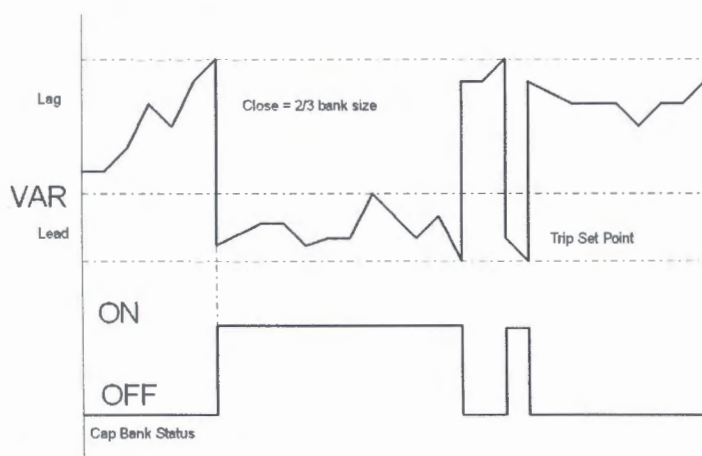


Figure 6.6.1 Typical VAR control concept

To avoid responding to sudden reactive power changes, restraint control or integration of inputs over certain time period can be used. These are available in most of the capacitor bank controllers.

- When transformers are paralleled, one controller feels only a half of the capacity of a switched bank.

- Step size of a bank is 5Mvar.
- Switching ON when lagging reactive power exceeds $2.5 * 2/3 = 1.6\text{Mvar}$ (lag)
- Switching OFF when leading reactive power exceeds $(2.5 * 1/3) * 1.4 \approx 1.2\text{Mvar}$ (lead)

Switching points were selected from simulation results with approximated AVR control and shown in Figure 6.6.1 the switching points based on lowest reactive power drawn from system and power factor close to unity (optimum compared to losses) was also show in the diagram.

A typical capacitor bank switch can operate 6times per day considering 50,000 no of operations and 20 years life time. The no of operations of the breakers are within the acceptable limits [3].

Date	Number of switching			
	Bank 1	Bank 2	Bank 3	Bank 4
24.07.09	0	0	2	2
28.07.09	0	0	2	2
31.07.09	0	0	1	2

Table 6.6.1 No of switching operations under proposed var control scheme

The utilization factor is calculated based on the same criteria described early in the chapter and equals to 80%. The utilization is approximately same as the present system but the new scheme is closer to the loss optimized pattern.

6.6.2. Voltage controlling of the BSC bank

Voltage control based capacitor switching in a utility substation has to follow a complex algorithm. The difficulty in voltage control based switching is due to the voltage regulator of the power transformers. When both functions try to control voltage at the same time without any coordination between them, then there will be severe malfunctioning of the two controllers. This will cause hunting of capacitor banks and tap changer. Therefore, for such a control scheme, an algorithm to coordinate AVR and capacitor bank controller is required. The factors that has to be considered in such a system are,

- During switching on for decreasing bus bar voltages, the capacitors shall come first if the reactive power load is more than a portion of the minimum step of a bank otherwise the tap changer can increase the voltage. The purpose of this is to minimize the losses and adding excess leading reactive power [8].
- During switching off for increasing terminal voltages, AVR and the capacitor controller shall follow the same philosophy. The reactive power at the time of decision must be considered in deciding whether to reduce the tap or to switch off a capacitor bank.

- Algorithm for an above control is necessary to optimize the use of capacitor banks. If the only requirement is to control the voltage, then proper dead band selection for two controllers also can serve the purpose.

One other thing to be considered is that when the network control centre increases the voltage at some other station having no capacitor banks by generator voltage adjustments, the substation having capacitor banks also will feel that and the bus voltage will improve. Then the capacitors will tend to switch off responding to outside voltage adjustments. This is not an economical solution [9].

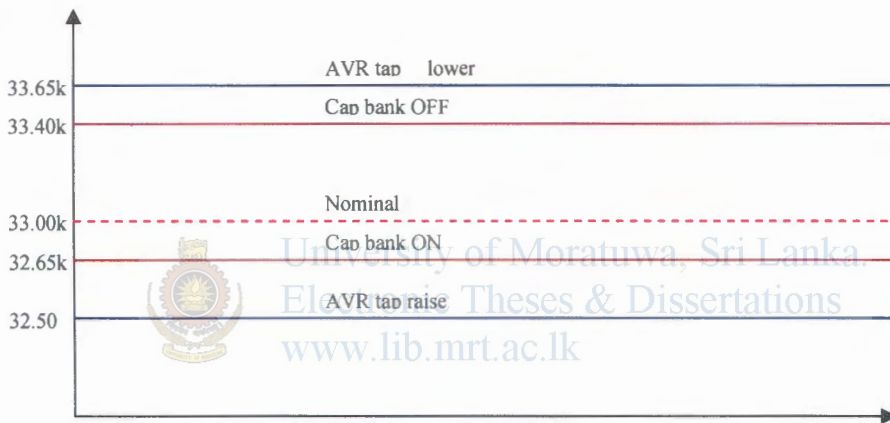


Figure 6.6.2.1 Proposal for dead bands for AVR and capacitor controller

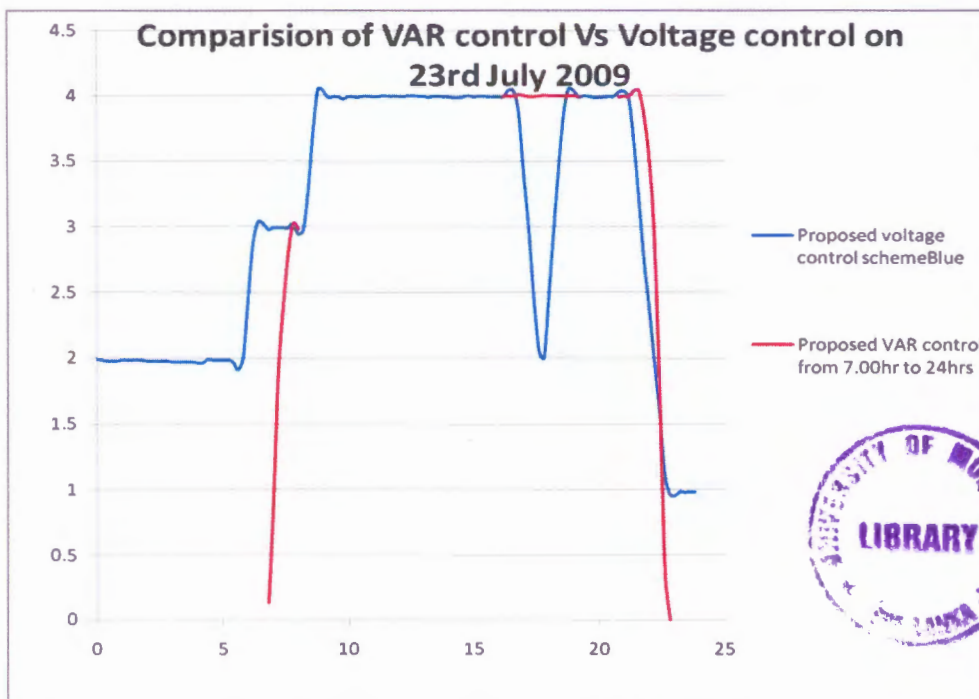


Figure 6.6.2.2 Comparison of switched banks under voltage control & var control schemes

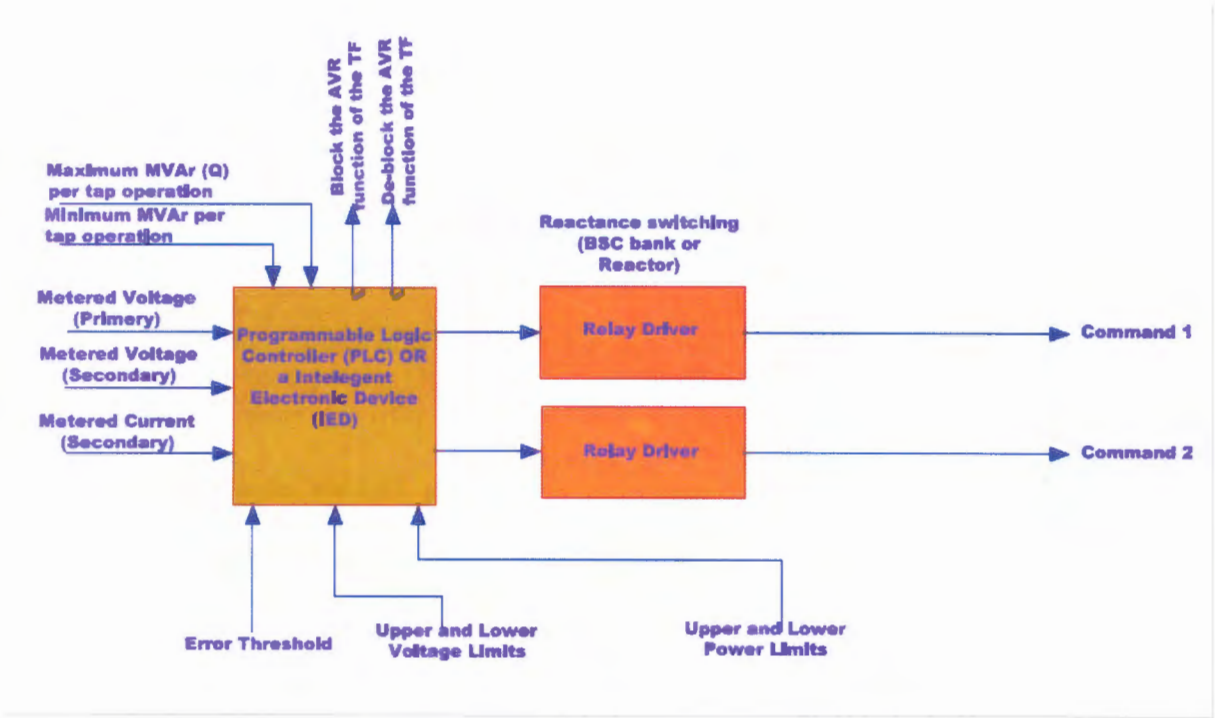
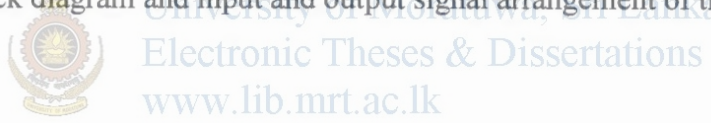


Figure 6.6.2.3 Block diagram and input and output signal arrangement of the controller



1. Concluding remarks and recommendations

7.1 Analysis and results

- i. Step size of the BSC bank is so small to effect the voltage variation in the 33kV bus. For, eg. normally the voltage rise of the 33kV bus when 5MVAR bank switching is about half the step size voltage of the OLTC with two transformers are in parallel
- ii. Therefore coordination of these two existing controllers is difficult with their present parameters. Occasions where the capacitor banks are switched ON and OFF manually by over-riding the auto controller was frequently observed.
- iii. Simulations models prove that unnecessary tap changing operations of the substation transformer occurred. The switching of the BSC bank in and out, and OLTC operation with feeder tripping has to be taken into account because this will reduce the life time of the switching device. The results and analysis reveals that it is possible to achieve the purpose of optimising the OLTC and BSC bank with modifications to the existing control system [6].
- iv. Simulation shows that the maximum voltage rising under different capacitor bank combinations (with effective Tap control) are 77.67kV, 77.89kV & 77.27kV respectively. The maximum percentage rise for high voltage side is 0.43% and that for low voltage side is 1.15%.
- v. The response time of transformer AVR and BSC bank controller are very slow compared to SVC or TCR. [5] Therefore risk of overvoltage during sudden load rejection may affect the equipment life time. We cannot increase the integration time or error threshold of the two controllers as required by the study to coordinate the controllers.
- vi. Simulation results indicate that the High Voltage side voltage measurement needed for the coordination of the two controlling system. This new parameter check the system Q-V variation to implement the capacitor banks switching which is well coordinated with the downstream OLTC operation which try to maintain the constant voltage at 33kV bus [1].
- vii. Downstream voltage (33kV) variation with added reactive power can be handled by the transformer AVR and tap changer controls so that any combination of banks is feasible to connect or disconnect.
- viii. The OLTC is capable enough to divert leading reactive power to upstream of the network without violating current carrying capacity of the OLTC.
- ix. Power factor based controlling is a very much economical method of capacitor bank controlling compared with other methods. One of the main problem a utility may face is that, some times especially in light load conditions with long

transmission lines (Galle GSS is currently facing), there may be a necessity of some lagging reactive power has to be injected to reduce the Ferranti effects.

- x. CEB faced real challenge maintaining voltage stability at the 132kV bus which far away from the generation. This happened most of the utilities in the world because production of the electricity was concentrated in one place due to resource availability. In such a case, voltage control based capacitor switching will be a good solution.

7.2 Conclusion

Considering all these factors discussed so far, followings are the conclusions from this research study.

- i. Existing control philosophy does not give maximum benefits to the CEB transmission network. Two schemes neither maximizes nor optimises the utilization of the BSC and the tap operation.
- ii. From the simulation the var consumption of the transformer is much high compared to delivering to the 33kV system when increasing tap operation to make the voltage constant. For example the transformer consumes 1.102MVAR vars when increasing tap from 8 to 12 for maintaining constant voltage at 33kV bus only delivering 1.479MVAR vars to the loads at 33kV.
- iii. Switching in of the BSC bank on the 33kV bus has increased only half of the tap step size of the voltage. Simulation result shows that ; it is technically possible to utilize the full installed capacities in all substations without violating the technical standards.
- iv. The study reveals that it is possible to consider the controllers with multi-parameter or boolean switching options. Reactive power and voltage can be the parameters to be considered in the switching decisions.
- v. The study will allow for controlled switching at a location within the "load" network that is physically outside of the power distribution substation. That is, the switched reactances can be at other buses which are electrically connected through low side system impedances (lines, cables, etc.) to the OLTC transformer. This switching of remotely located reactive elements will require communication circuitry of the variety readily available through normal SCADA (system control and data acquisition) systems.

7.3 Recommendations for future studies

1. Specially the most of the future substations were unmanned and automated one can look for the possibility of integrating this system for distribution management system (DSM) to minimise losses and optimise voltage and var flow through transmission and distribution network.
2. Suitable architecture for hardware and software should be decided and total variable and the calculation that has to be handled by the controller has to be studied. The

decision variables and command can be implemented on the controller (IED) or (PLC) as studied by this research [10].

3. Further studied can be done including embedded generation which play more vital role in future (say it is planned to add 20% renewable energy by year 2020 to minimise the GHG emission) generation as renewable energy to the 33kV bus of the GSS [6].
- 4 The study also includes a method for regulating shunt reactance-switching in a power transmission system providing a plurality of distribution voltages including a first voltage and a second voltage for supplying power to a load including the steps of
 - (1) Measuring the first voltage and reactive power flowing towards the load, and
 - (2).Switching at least one shunt reactance to maintain the second voltage substantially constant based on the measurements made in step (1) and predetermined ranges for the first voltage and reactive power.
5. This study can be extended to investigate performance of the slow voltage collapse phenomena in the HV side because the existing system further deteriorate the voltage collapse by doing tap operations [1]



University of Moratuwa, Sri Lanka.
Electronic Theses & Dissertations
www.lib.mrt.ac.lk

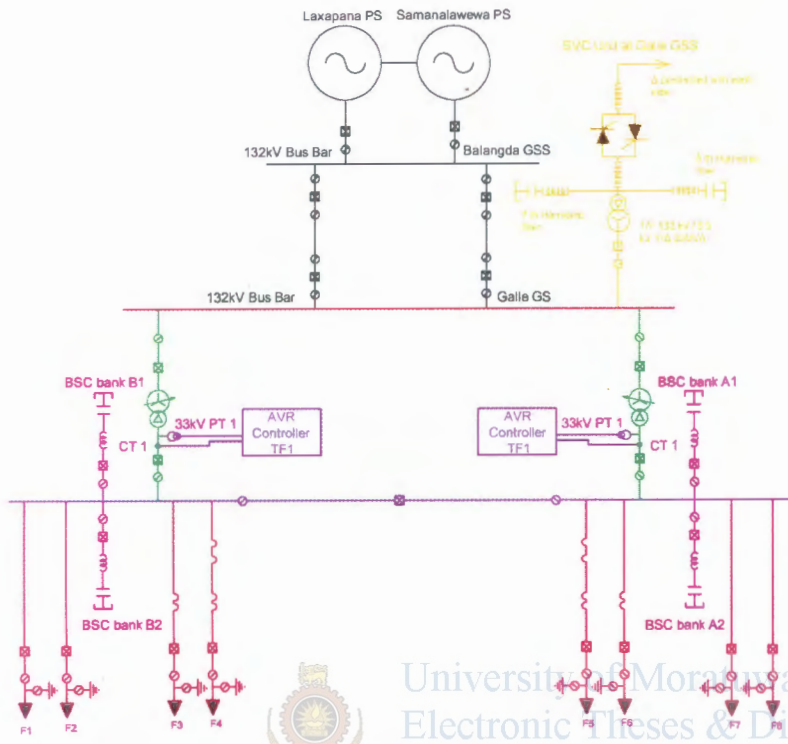
References

- [1] Zoran Gajic, Daniel Karisson, Mike Kockott, “Advanced OLTC control to counteract power system voltage instability”
- [2] Kusumshanthi K.P “Benchmark the Sri Lankan power system by power quality monitoring & analysis” Master Thesis, University of Moratuwa , 2005. Chapter 8.2 pp 42
- [3] DDU Dopage “Optimising the use of breaker switch capacitor bank in CEB transmission network” Master Thesis, University of Moratuwa, 2009. Chapter 6 pp 42-48.
- [4] IEC 60871-1 Shunt capacitors for AC power systems having a rated voltage above 1000 V Part 1: General – Performance, testing and rating. Safety requirements – Guide for installation and operation – Section 4.
- [5] Taylor C.W. “Power system voltage stability” McGraw-Hill, 1993 Chapter 10. pp 242-251
- [6] ABB review 2009 part 3 pp 33-37
- [7] User Manual for PSCAD
- [8] Website <http://w.w.w.nepsi.com> (Reading reference)
- [9] Website <http://w.w.w.nokiancapacitors.com> “Reactors and shunt capacitor banks- An application note –EN TH08 11/2004” pp 2-4
- [10] MR- Tapcon transformer AVR controller manual
- [11] ABB Switch gear manual (For theoretical calculations)
- [12] Website <http://w.w.w.cooper capacitor.com> (Reading reference)
- [13] Suresh Kumar K.S “Applications of power capacitors in electrical distribution systems” pp 1-5

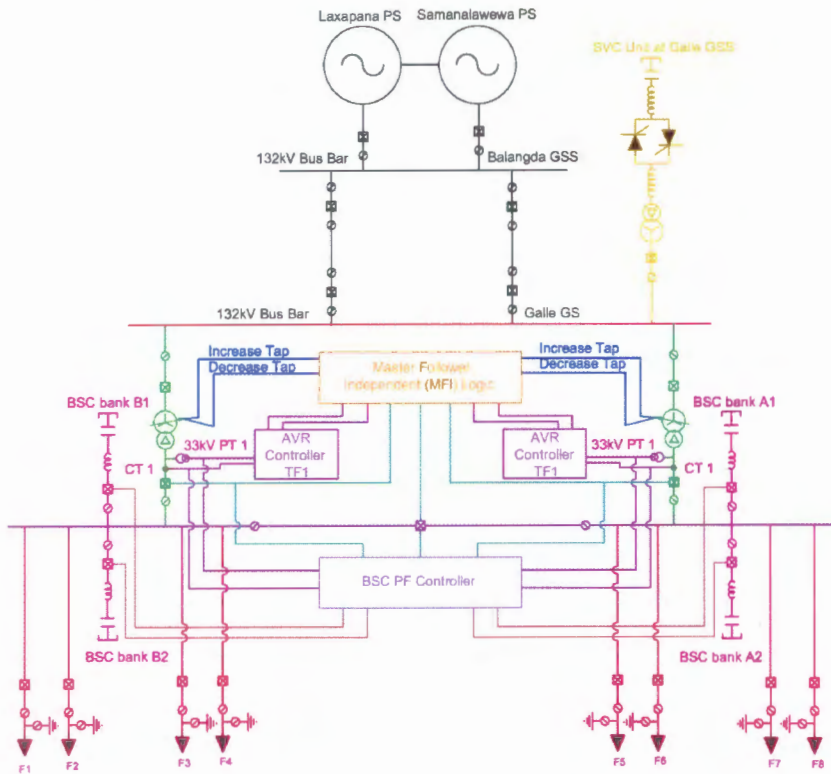
Appendices

Appendix A

Appendix A1- Single line arrangement of the Galle GSS



Appendix A2 - AVR and PF control circuit arrangement of the GSS



Appendix A3- Single unit (5MVA_r) of the BSC bank at Galle GSS



Appendix B

Appendix (B1.1) - Fixed tap at rated V BSC are OFF (TA11 Tap 08)

Pload	Qload	Q33kv	P33kv	V33kv	Q132kV	P132kV	Vmax	Vmin	PF angle
4.500000	2.666667	14.65727	25.3598	31.6009	19.3146	25.6573	33.33	32.67	37.0047
4.855556	2.855556	15.5879	27.145	31.5082	20.468	27.4421			36.3762
5.211111	3.044444	16.50565	28.9047	31.4158	21.6215	29.2016			35.806
5.566667	3.233333	17.4106	30.6392	31.3233	22.7746	30.936			35.28425
5.922222	3.422222	18.30293	32.3489	31.2306	23.9275	32.6459			34.8156
6.277778	3.611111	19.18271	34.0346	31.1377	25.0799	34.3315			
6.633333	3.800000	20.0502	35.6963	31.045	26.2318	35.9941			33.96505
6.988889	3.988889	20.9095	37.3346	30.9524	27.3832	37.633			33.5936
7.344444	4.177778	21.6118	38.95	30.8594	28.5338	39.2491			33.25
7.700000	4.366667	22.5796	40.5425	30.7667	29.6837	40.8424			32.9321
8.055556	4.555556	23.3987	42.1124	30.674	30.8328	42.4134			32.63785
8.411111	4.744444	24.206	43.6605	30.5811	31.9808	43.9623			32.3643
8.766667	4.933333	25.0015	45.1866	30.4882	33.1279	45.4895			32.1104
9.122222	5.122222	25.7856	46.6911	30.3955	34.2738	46.995			31.87425
9.477778	5.311111	26.5568	48.1741	30.303	35.4185	48.4793			31.65445
9.833333	5.500000	27.319	49.6361	30.2102	36.5619	49.9424			31.44935

Appendix (B1.2) - Tap is varying to bring the voltage to set BW limits BSC are OFF (TA11 Tap 10)

Pload	Qload	Q33kv	P33kv	V33kv	Q132kV	P132kV	Vmax	Vmin	PF angle
4.500000	2.666667	15.37391	26.6066	32.3607	20.9883	26.919	33.33	32.67	37.01835
4.855556	2.855556	16.34856	28.477	32.2646	22.186	28.7883			36.4023
5.211111	3.044444	17.3097	30.3204	32.1686	23.3842	30.6309			35.8379
5.566667	3.233333	18.25729	32.137	32.0726	24.5819	32.4469			35.3212
5.922222	3.422222	19.19127	33.9272	31.9762	25.779	34.237			34.8464
6.277778	3.611111	20.1121	35.6918	31.8801	26.9759	36.0016			34.41215
6.633333	3.800000	21.0198	37.4311	31.7836	28.1723	37.741			34.0118
6.988889	3.988889	21.9144	39.5138	31.6874	29.3679	39.4557			33.6419
7.344444	4.177778	22.7961	40.8352	31.5908	30.5627	41.1461			33.3006
7.700000	4.366667	23.6651	42.5009	31.4945	31.7568	42.8124			32.98465
8.055556	4.555556	24.5213	44.1425	31.3982	32.9498	44.4549			32.6916
8.411111	4.744444	25.365	45.7607	31.3017	34.1419	46.0739			32.41935
8.766667	4.933333	26.1961	47.3557	31.2053	35.3327	47.6699			32.1666
9.122222	5.122222	27.0151	48.9276	31.109	36.5224	49.2429			31.93125
9.477778	5.311111	27.8217	50.4768	31.0129	37.7106	50.7932			31.71195
9.833333	5.500000	28.6165	52.0034	30.9164	38.8973	52.3211			31.50715

Appendix (B1.3) - Tap is varying to bring the voltage to set BW limits BSC are OFF (TA11 Tap 12)

Pload	Qload	Q33kv	P33kv	V33kv	Q132kv	P132kv	Vmax	Vmin	PF angle
4.500000	2.666667	16.13711	27.9375	33.1497	22.9931	28.2721	33.33	32.67	37.02775
4.855556	2.855556	17.15891	29.8987	33.0496	24.237	30.2314			36.41805
5.211111	3.044444	18.16598	31.8306	32.9499	25.4802	32.1619			35.8548
5.566667	3.233333	19.1588	33.7344	32.8501	26.7332	34.0645			35.3438
5.922222	3.422222	20.1371	35.6102	32.7499	27.9654	35.9396			34.87475
6.277778	3.611111	21.1015	37.4585	32.6499	29.207	37.7875			34.4441
6.633333	3.800000	22.0518	39.2799	32.5499	30.4479	39.6087			34.04775
6.988889	3.988889	22.9881	41.0748	32.4497	31.6836	41.4036			33.68075
7.344444	4.177778	23.9109	42.8438	32.3494	32.9268	43.1728			33.34375
7.700000	4.366667	24.8201	44.5868	32.2493	34.1648	44.9162			33.0308
8.055556	4.555556	25.7157	46.3041	32.1493	35.4017	46.6344			32.7406
8.411111	4.744444	26.5979	47.9969	32.0491	36.6373	48.3278			32.4712
8.766667	4.933333	27.4669	49.6646	31.9489	37.8714	49.9963			32.21985
9.122222	5.122222	28.3228	51.3076	31.8491	39.1045	51.6403			31.98685
9.477778	5.311111	29.1655	52.9269	31.7488	40.3357	53.2607			31.7688
9.833333	5.500000	29.9954	54.5222	31.6486	41.5655	54.1571			31.5685

Appendix (B1.4)



University of Moratuwa, Sri Lanka.
Electronic Theses & Dissertations

Tap is varying to bring the voltage to set BW limits BSC are OFF (TA11 Tap 14)

Pload	Qload	Q33kv	P33kv	V33kv	Q132kv	P132kv	Vmax	Vmin	PF angle
4.500000	2.666667	15.74952	27.2611	32.7516	21.9438	27.5836	33.33	32.67	37.03205
4.855556	2.855556	16.74743	29.1764	32.6537	23.1646	29.4974		Tap 11	36.41235
5.211111	3.044444	18.61444	32.623	33.351	26.6813	32.9678		Tap 13	35.86065
5.566667	3.233333	19.63077	34.5722	33.2492	27.9469	34.9156		Tap 13	35.3505
5.922222	3.422222	20.632	36.4927	33.147	29.2115	36.835		Tap 13	34.88325
6.277778	3.611111	21.6194	38.3848	33.0451	30.4754	38.7265		Tap 13	34.4553
6.633333	3.800000	22.592	40.2491	32.9431	31.7384	40.5904		Tap 13	34.0605
6.988889	3.988889	23.5503	42.0861	32.8409	33.0002	42.4273		Tap 13	33.6961
7.344444	4.177778	24.4945	43.896	32.7387	34.2612	44.2373		Tap 13	33.35985
7.700000	4.366667	25.4245	45.6795	32.6367	35.5208	46.0211		Tap 13	33.0488
8.055556	4.555556	26.9846	48.6044	32.9268	38.2716	48.9608		Tap 14	32.7753
8.411111	4.744444	27.9077	50.376	32.8222	39.5509	50.7329		Tap 14	32.50995
8.766667	4.933333	28.8167	52.1206	32.7183	40.8268	52.4782		Tap 14	32.2615
9.122222	5.122222	29.7117	53.8392	32.6146	42.1019	54.1976		Tap 14	32.0305
		30.4377	55.1637	33.0068	43.781	55.5385		Tap 15	32.04815
9.477778	5.311111	30.5928	55.5322	32.5101	43.3752	55.8916		Tap 14	31.81545
		31.3386	56.895	32.9004	45.0745	57.2708		Tap 15	31.83385
9.833333	5.500000	31.4602	57.1995	32.4063	44.6465	57.5601		Tap 14	31.6146
		33.0134	60.0429	33.1896	48.2172	60.4385		Tap 16	

Appendix (B2.1)

One BSC bank is ON 5Mvar

Pload	Qload	Q33kv	P33kv	V33kv	Q132kv	P132kv	Vmax	Vmin	PF angle
4.500000	2.666667	10.3323	25.9544	31.952	15.1069	26.2479	33.33	Tap 08	30.20765
		10.83654	27.2274	32.7237	16.6337	27.5385		Tap 10	30.3885
4.855556	2.855556	11.23831	27.7787	31.8579	16.297	28.0714		Tap 08	30.00265
		12.15258	29.8529	33.02	18.7786	30.1741		Tap 11	30.00235
5.211111	3.044444	12.27842	29.5753	31.7632	17.4662	29.8675		Tap 08	29.7939
		13.2312	31.781	32.9201	20.0731	32.1007		Tap 11	30.01725
5.566667	3.233333	13.2312	31.3467	31.6691	18.6752	31.6387		Tap 08	29.60075
		14.2102	33.681	32.8202	21.2942	34.0003		Tap 11	29.79855
5.922222	3.422222	14.17099	33.0926	31.5741	19.864	33.3846		Tap 08	29.41805
		15.21926	35.5521	32.7206	22.5525	35.8698		Tap 11	29.5914
6.277778	3.611111	15.09732	17.5933	31.4801	21.0516	35.1047		Tap 08	29.9378
		16.21245	37.796	32.6203	23.8091	37.7132		Tap 11	29.39765
6.633333	3.800000	16.0104	36.5082	31.3854	22.2385	36.8008		Tap 08	29.06865
		17.61033	40.1734	32.912	26.1869	40.5031		Tap 12	29.28745
6.988889	3.988889	16.91076	38.1796	31.2908	23.4245	38.4728		Tap 08	28.9104
		18.59892	42.0058	32.8098	27.4655	42.3352		Tap 12	29.12005
7.344444	4.177778	17.79903	39.8276	31.1958	24.6106	40.12114		Tap 08	28.76745
		19.57159	43.8111	32.7075	28.7415	44.1406		Tap 12	28.95825
7.700000	4.366667	18.67417	41.4319	31.101	25.7951	41.7459		Tap 08	28.62685
		20.5307	45.5896	32.6052	30.0169	45.9192		Tap 12	28.8093
8.055556	4.555556	19.53705	43.0524	31.0063	26.9791	43.3479		Tap 08	28.5007
		21.9994	48.5001	32.8936	32.6107	48.8448		Tap 13	28.7266
8.411111	4.744444	20.3876	44.63	30.9113	28.1617	44.9267		Tap 08	28.3804
		22.9518	50.2666	32.7891	33.906	50.6117		Tap 13	28.59945
8.766667	4.933333	21.2256	46.1855	30.8163	29.3427	46.4832		Tap 08	28.26895
		23.8901	52.0061	32.6848	35.1996	52.3519		Tap 13	28.48005
9.122222	5.122222	22.0519	47.7178	30.7215	30.5232	48.0167		Tap 08	28.1629
		24.8141	53.7201	32.5807	36.4919	54.0667		Tap 13	28.37165
		25.419	55.0346	32.9719	37.9925	55.3982		Tap 14	28.41325
9.477778	5.311111	22.8659	49.2288	30.6269	31.7021	49.529		Tap 08	28.0679
		25.7248	55.4074	32.4763	37.7822	55.7549		Tap 13	28.27055
		26.3509	56.7601	32.8654	39.3045	57.1244		Tap 14	28.3112
9.833333	5.500000	23.6679	50.7186	30.532	32.8801	51.0202		Tap 08	27.98295
		26.6208	57.0695	31.372	39.0704	57.418		Tap 13	28.176
		27.267	58.4602	32.7591	40.617	58.8255		Tap 14	28.21665

Appendix (B2.2) two capacitor banks on

Pload	Qload	Q33kv	P33kv	V33kv	Q132kV	P132kV	Vmax	Vmin	PF angle
4.500000	2.666667	5.79073	26.7043	32.3197	10.7224	26.9832	33.33	Tap 08	23.09325
		6.07324	28.0255	33.1049	12.0582	28.3195		Tap 10	
4.855556	2.855556	6.8217	28.5662	32.2228	11.9658	28.8445		Tap 08	23.43645
		7.15511	29.9775	33.0047	13.3436	30.267		Tap 10	23.469
5.211111	3.044444	7.83855	30.3999	32.1255	13.2019	30.6779		Tap 08	23.69695
		8.22192	31.8995	32.904	14.6275	32.186		Tap 10	23.7137
5.566667	3.233333	8.8413	32.2062	32.0289	14.4364	32.4842		Tap 08	23.8961
		9.27364	33.7926	32.8039	15.9098	34.0804		Tap 10	23.9028
5.922222	3.422222	9.83005	33.9859	31.932	15.6694	34.2641		Tap 08	24.05045
		10.31058	35.6572	32.7036	17.1907	35.9445		Tap 10	24.0524
6.277778	3.611111	10.80528	35.7389	31.8342	16.9008	36.0177		Tap 08	24.16905
		11.6069	38.4132	32.9965	19.3812	38.7082		Tap 11	24.21075
6.633333	3.800000	11.767	37.4664	31.7375	18.1308	37.7459		Tap 08	24.2631
		12.64109	40.2649	32.8943	20.6824	40.5601		Tap 11	24.29755
6.988889	3.988889	12.71531	39.1682	31.6406	19.3591	39.4489		Tap 08	24.337
		13.6585	42.0893	32.7915	21.9818	42.3848		Tap 11	24.36825
7.344444	4.177778	13.65032	40.8457	31.5431	20.5856	41.1273		Tap 08	24.396
		14.66141	43.8861	32.6813	23.2795	44.1823		Tap 11	24.4258
7.700000	4.366667	14.57227	42.4987	31.4458	21.8107	42.7813		Tap 08	24.44405
		16.03108	46.7754	32.9788	25.6793	48.0812		Tap 12	24.5276
8.055556	4.555556	15.48121	44.1274	31.3488	23.0342	44.4114		Tap 08	24.5836
		17.02831	48.5596	32.874	26.9964	48.8662		Tap 12	24.56405
8.411111	4.744444	16.37715	45.7326	31.2515	24.2558	46.0176		Tap 08	24.51675
		18.01085	50.3168	32.769	28.3118	50.6245		Tap 12	24.59575
8.766667	4.933333	17.26044	47.3142	31.1539	25.4759	47.6009		Tap 08	24.54545
		18.97911	52.0472	32.6639	29.6249	52.3562		Tap 12	24.62315
9.122222	5.122222	18.13119	48.8726	31.0569	26.6941	49.1608		Tap 08	24.5703
		19.93282	53.7515	32.5592	30.9359	54.0619		Tap 12	24.6475
		20.4179	55.0674	32.951	32.2385	55.3885		Tap 13	24.71135
9.477778	5.311111	18.98931	50.4082	30.9599	27.9104	50.698		Tap 08	24.59225
		20.8724	55.43	32.4544	32.2449	55.7419		Tap 12	24.52095
		21.3794	56.785	32.8441	33.5701	57.1066		Tap 13	24.73115
9.833333	5.500000	19.83486	51.9213	30.8625	29.1247	52.2158		Tap 08	24.613
		21.7979	57.0829	32.3491	33.5514	57.3963		Tap 12	24.6921
		22.3264	58.4743	32.7368	34.8996	58.7985		Tap 13	24.75085

Appendix (B2.3) three capacitor bank on

Pload	Qload	Q33kv	P33kv	V33kv	Q132kV	P132kV	Vmax	Vmin	PF angle	Tap
4.500000	2.666667	0.988573	27.2229	32.7095	5.86058	27.5112	33.33	32.67	11.9661	Tap 0
		1.011018	27.8917	33.1066	6.38655	28.1874			11.82285	Tap 0
4.855556	2.855556	2.0777	29.1275	32.6107	7.13354	29.4144			13.1104	Tap 0
		2.12212	29.8418	33.0061	7.6851	30.1395			13.03685	Tap 0
5.211111	3.044444	3.15174	31.0033	32.5114	8.40558	31.2895			14.1561	Tap 0
		3.22261	31.7619	32.9048	8.98233	32.0549			14.05295	Tap 0
5.566667	3.233333	4.2116	32.8507	32.4124	9.67751	33.1368			15.01575	Tap 0
		4.40719	34.4826	33.2034	10.9561	34.7835			14.8634	Tap 1
5.922222	3.422222	5.25472	34.6691	32.3129	10.9451	34.9549			15.72625	Tap 0
		5.50401	36.3895	33.1	12.2773	36.6898			15.60725	Tap 1
6.277778	3.611111	6.28583	36.4636	32.213	12.2164	36.7503			16.3843	Tap 0
		6.58498	38.2685	32.9962	13.5971	38.5685			16.25665	Tap 1
6.633333	3.800000	7.30163	38.231	32.1133	13.4843	38.5175			16.93905	Tap 0
		7.65125	40.1191	32.8932	14.916	40.419			16.82455	Tap 1
6.988889	3.988889	8.30362	39.9717	32.014	14.7514	40.2588			17.4276	Tap 0
		8.70178	41.9421	32.7889	16.2329	42.2422			17.3237	Tap 1
7.344444	4.177778	9.29152	41.6866	31.9134	16.0171	41.9745			17.8588	Tap 0
		9.7376	42.7373	32.6848	17.5485	44.031			17.76415	Tap 1
7.700000	4.366667	10.26526	43.3767	31.8133	17.2815	43.6656			18.24675	Tap 0
		11.01652	46.6228	32.9762	19.7783	46.9333			18.1547	Tap 1
8.055556	4.555556	11.22564	45.0416	31.7135	18.5443	45.3315			18.59355	Tap 0
		12.047	48.4052	32.8697	21.1155	48.7165			18.5108	Tap 1
8.411111	4.744444	12.17235	46.6816	31.6135	19.8057	46.9727			18.9056	Tap 0
		13.06266	50.1608	32.7634	22.4512	50.4728			18.83385	Tap 1
8.766667	4.933333	13.10548	48.2978	31.5138	21.0655	48.5902			19.1918	Tap 0
		14.06389	51.89	32.6573	23.786	52.203			19.1368	Tap 1
9.122222	5.122222	14.02568	49.8903	31.4135	22.3242	50.1882			19.4576	Tap 0
		15.05037	53.592	32.5514	25.1176	53.906			19.39785	Tap 1
		15.41358	54.906	32.9448	26.2295	55.231			19.4282	Tap 1
9.477778	5.311111	14.93258	51.3984	31.3137	23.5804	51.7535			19.6948	Tap 0
		16.02219	55.2689	32.4454	26.4478	55.5843			19.64895	Tap 1
		16.40744	56.6204	32.8367	27.5827	56.9467			19.672	Tap 1
9.833333	5.500000	15.82614	53.0029	31.2137	24.835	53.3			19.915	Tap 0
		16.97971	56.9195	32.3393	27.7758	57.2363			19.8775	Tap 1
		17.3875	58.3085	32.7284	28.9348	58.6361			19.90155	Tap 1