

PARAMETER OPTIMIZATION FOR HIGH PERFORMANCE COMPUTING SYSTEMS USING GENETIC ALGORITHM

K. I. A. I. KARIYAWASAM

208558H

MSC IN ARTIFICIAL INTELLIGENCE

**DEPARTMENT OF COMPUTATIONAL MATHEMATICS
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**University of Moratuwa
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DECLARATION

I declare that this is my own work, and this thesis/dissertation does not incorporate without acknowledgement any material previously submitted for a degree or diploma in any other University or Institute of higher learning and to the best of my knowledge and belief it does not contain any material previously published or written by another person except where the acknowledgement is made in the text. I retain the right to use this content in whole or part in future works (such as articles or books).

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Date: 11th July 2023

The above candidate has carried out research for the Master's thesis/dissertation under my supervision. I confirm that the declaration made above by the student is true and correct.

Name of Supervisor: Dr. Thushari Silva

Signature of the Supervisor:

Date: 12/07/2023

DEDICATION

I would also like to dedicate this thesis to my wife, Anuradha, who has been my rock and my constant source of motivation. Also, my two children Dhyana and Veditha; their patience, understanding, and steadfast support have been invaluable to me throughout this journey. I am grateful for their unwavering love, and for always believing in me, even when I didn't believe in myself.

I would like to dedicate this thesis to my parents, who have always supported me throughout my academic journey. Their unwavering encouragement and belief in me have been instrumental in helping me achieve my goals. I am grateful for their unwavering love and guidance.

I would also like to dedicate this thesis to my colleagues Romain Bottier and Indika Prasad Kumara at Dell Technologies and London Stock Exchange Group for their support on accessing real life scenarios and their valuable technical inputs to shape my work into success.

Finally, I would like to dedicate this thesis to all the people who have supported and encouraged me along the way, including my friends, family, and mentors. Without their guidance and support, this achievement would not have been possible.

Thank you all for your love and support.

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K. I. A. I. Kariyawasam

ABSTRACT

Though Von Neumann Architecture (vNa) has had unprecedented success for general-purpose computing for the past seven decades. While being heavily used in High Performance Computing (HPC) systems, vNa is becoming unpopular among industry professionals due to vNa bottleneck and unable to address the ever-increasing demand for performance gain by latest HPC applications. Though there are few methodologies to overcome vNa bottleneck; namely Processor caching, Prefetching, multithreading, Processing in Memory (PIM) and RAMBUS, which we will not discuss in this paper, the latency between ALU and memory still hold back the performance of vNa systems, even in HPC environments. Alternatively, there are few different technologies are emerging as opposed to vNa such as Quantum computing, Parallel computing, Harvard Computing architecture (HCA) which are addressing the vNa bottleneck and taking computing performance in to a whole new level in terms of performance in Floating Points (Flops). On the other hand, another alternative is to use accelerators like Graphic Processing Units (GPU, Field Programmable Gate Arrays (FPGA) and Dell Process Acceleration Tool (DPAT) to overcome the latency between ALU and Memory subsystem.

Even though there are several alternatives available to overcome vNa bottleneck, the performance requirement from almost every HPC application seems never to be achieved by the underlying HPC hardware systems. Hardware system configurations are always performed at a sub-optimal level, and no one has the time or patience to go through thousands of different permutations of hardware parameter finetuning. Moreover, we simply cannot blame any system administrator who is responsible for HPC system configurations, especially processor, memory, and network parameter finetuning to provide best performance benchmarks, as it's a very time consuming and tedious task of many man-days of manually configuring all those parameters to find an optimal convergence point. On the other hand, one cannot be satisfied of a particular combination of parameters is the peak performance point as there always be a doubt whether there can be another set of combination exist for the optimal performance. Thus, it will be a never-ending manual task to find the optimal performance of HPC hardware systems.

To overcome HPC hardware parameter finetuning to find the best performance benchmarks, we proposed use of Genetic Algorithm based approach to find the best combination of Processor, memory, and network parameters to deliver highest hardware performance for any HPC application.

TABLE OF CONTENTS

DECLARATION.....	i
DEDICATION.....	ii
ACKNOWLEDGEMENT.....	iii
ABSTRACT.....	iv
TABLE OF CONTENTS	v
List of Figures.....	viii
LIST OF TABLES	ix
Chapter 1	1
INTRODUCTION.....	1
1.1 Prolegomena	1
1.2 Objectives.....	1
1.3 Background and Motivation	2
1.4 Problem in Brief.....	2
1.5 Parameter Optimization for High Performance Computing Systems using Genetic Algorithm.....	3
1.6 System Requirement.....	4
1.7 Structure of the Thesis.....	4
1.8 Summary.....	4
Chapter 2	5
LITERATURE REVIEW ON PARAMETER OPTIMIZATION FOR HIGH PERFORMANCE COMPUTING SYSTEMS USING GENETIC ALGORITHM.....	5
2.1 Introduction.....	5
2.2 High-Performance Computing Systems.....	5
2.3 Use of Genetic Algorithms for HPC	6
2.4 Analysis literature.....	8
2.5 Research Problem definition.....	9
2.6 Summary.....	10
Chapter 3	11
TECHNOLOGY ADOPTED.....	11

3.1.	Introduction.....	11
3.2.	Technology Overview	11
3.3.	Methodology	12
3.3.1.	CPU parameters.....	12
3.3.2.	Memory parameters	12
3.3.3.	Network parameters	12
3.4.	Genetic Algorithm and Fitness Function	13
3.4.1.	Fitness Function	13
3.5.	Summary.....	14
Chapter 4		15
PARAMETER OPTIMIZATION FOR HIGH PERFORMANCE COMPUTING SYSTEMS USING GENETIC ALGORITHM.....		15
4.1.	Introduction.....	15
4.2.	Hypothesis.....	15
4.3.	Input	15
4.4.	Output	16
4.5.	Process (Parameter collection, Modification and finetuning).....	16
3.5.1.	Parameter Collection	16
3.5.2.	Modification and Finetuning.....	16
4.6.	Users	16
4.7.	Features.....	16
4.8.	Summary.....	17
Chapter 5		18
DESIGN		18
5.1.	Introduction.....	18
5.2.	Input.....	18
5.3.	Process.....	18
5.3.1.	Parameter Collection and Modification.....	18
5.3.2.	Defining Parameters in Genetic Algorithm	19
5.3.2.1.	The Memory Parameter	19
5.3.2.2.	The Memory Parameter	20
5.3.2.3.	The Memory Parameter	20
5.3.2.4.	Crossover and Mutation.....	21

5.4. Summary.....	24
Chapter 6	25
IMPLEMENTATION	25
6.1. Introduction.....	25
6.2. Research Design	25
6.3. Data Collection and Analysis	26
6.4. Summary.....	28
Chapter 7	29
EVALUATION	29
7.1. Introduction.....	29
7.2. Data analysis and findings.....	29
7.3. Limitations.....	32
7.4. Summary.....	32
Chapter 8	33
CONCLUSION AND FUTURE WORK	33
8.1. Introduction.....	33
8.2. Limitations.....	33
8.3. Future work.....	33
8.4. Summary.....	34
References.....	35

List of Figures

Figure 1	19
Figure 2	23
Figure 3- 100Mb/S	26
Figure 4- 1Gb/S	27
Figure 5- 10Gb/S	27
Figure 6- 25Gb/S	28
Figure 7- 100Mb-SET_TIGHT	29
Figure 8- 1Gb-SET_TIGHT	30
Figure 9- 10Gb-SET_TIGHT	30
Figure 10- 25G-SET_TIGHT	31
Figure 11-25Gb-openload	32

LIST OF TABLES

Table 1..... 9

Table 2..... 20