PERFORMANCE EVALUATION OF A GENERALIZED MULTILEVEL INVERTER WITH DIFFERENT OPERATING MODES

V.K. Ruchira Sampath

(168531X)

Degree of Master of Science in Electrical Engineering

Department of Electrical Engineering

University of Moratuwa

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Vidana Kankanamge Ruchira Sampath

(168531X)

Dissertation submitted in partial fulfillment of the requirements for the

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Name of the Supervisor: Prof. J.P. Karunadasa

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Abstract

Multilevel inverters are found in many applications in high power levels. These converters are available in different topological options, such as Cascaded Half Bridge, Neutral Point Clamp, Flying Capacitor, Hybrid and so on. By selecting appropriate switching sub-circuit, generalized multilevel inverter can be used to derive all common topologies.

A Generalized 9 Level Inverter is developed and controlled to operate in Cascaded Half Bridge, Neutral Point Clamped and Flying Capacitor modes for operation in 3, 5, 7 and 9 levels with square-wave and Pulse Width Modulation control. Relative performances were investigated in terms of Total Harmonic Distortion and efficiency.

Acknowledgement

I would like to express my heartfelt gratitude to all the people who have helped me in successfully achieve the targets of my MSc Electrical Engineering research project.

First of all, I take this opportunity thank my project Supervisor Prof. J.P. Karunadasa for providing the concept and for his continuous guidance and support throughout the period.

My sincere thanks go to all my colleagues at Ceylon Electricity Board who supported me in several ways to achieve my targets during this busy time period.

Finally, I would like to take this opportunity to say my heart felt respect and gratitude to my family members, for helping me to complete my MSc Research Project during this busy and difficult time period.

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LIST OF ABBREVIATIONS

Abbreviation	Description
PWM	Pulse Width Modulation
SWM	Square Wave Modulation
NPC	Neutral Point Clamped
CHB	Cascaded Half Bridge
FC	Flying Capacitor
THD	Total Harmonic Distortion
G9LI	Generalized 9 Lever Inverter
SV	Space Vector

CHAPTER 1

1. INTRODUCTION

1.1 Background

Multilevel inverters are found in many applications in high power levels due to their significantly improved Total Harmonic Distortion levels both at the output voltage (or current) and the input voltage (or current). Due to falling of cost of power electronics, these converters have begun to penetrate medium power application domain as well.

These converters are available in different topological options, such as Cascaded Half Bridge, Neutral Point Clamped, Flying Capacitor, Hybrid and so on each having its own relative strengths and limitations. Different applications according to their character select the best topology for the implementation.

By selecting appropriate switching sub-circuit from a switching matrix, generalized multilevel inverter is an arrangement that can be used to derive all common topologies. This arrangement needs greater number of switching devices. It can be tolerated over the flexibility it offers with respect to customizing the most suitable topology for the application in hand.

CHAPTER 2

2. PROJECT OVERVIEW

2.1 Scope of my Project

Identify switching paths within a generalized 9-level inverter for Cascaded Half Bridge, Neutral Point Clamp and Flying Capacitor modes of 3, 5, 7 and 9 levels. Design switching algorithms corresponding to square-wave and Pulse Width Modulation control of each mode of operation. Simulate each mode and level with different controls in MATLAB and investigate input output performances. Evaluate performances and draw recommendations.

2.2 Objectives of the study

Main objectives of the Research Project are as follows.

- To develop control and switching interfaces to operate a 9-level generalized inverter in Cascaded Half Bridge, Neutral Point Clamped and Flying Capacitor modes for operation in 3, 5, 7 and 9 levels with square-wave and Pulse Width Modulation control.
- To investigate relative performances, in terms of Total Harmonic Distortion and efficiency, when the Generalized Multilevel Inverter is operated in different topological-modes in each number of levels, with square-wave and Pulse Width Modulation control.

2.3 Methodology

Methodology of the Research Project is as follows.

- Literature review on the operation of multilevel converters of the common categories and generalized type.
- Identifying switching paths within a generalized 9-level inverter for Cascaded Half Bridge, Neutral Point Clamp and Flying Capacitor modes of different levels.
- Designing of switching algorithms corresponding to square-wave and Pulse Width Modulation control of each mode of operation.
- Simulation of each mode and level with different controls in MATLAB and investigate input output performances.
- Evaluation of performances and drawing recommendations.

CHAPTER 3

3. GENERALIZED MULTI LEVEL INVERTER

3.1 Literature Survey

Akira Nabae, Isao Takahashi and Hirofumi Akagi have presented in their research paper [1], a new Neutral Point Clamped PWM converter they have modeled and presented the findings of investigations done analytically and experimentally. They have compared the facilities of these inverter types and presented the short falls they have found. Further, they have introduced a brand new PWM technique match for an ac motor drive system. The Neutral Point Clamped PWM converter adopting this brand new PWM technique expresses excellent motor drive system efficiency, including motor efficiency, and it is excellent for a wide range variable speed motor drive system.

T. A. Meynard, M. Fadel and N. Aouda have presented in their research paper [2], for multilevel converters a static and dynamic model with imbricated cells. They have studied and identified the phenomena that take place within a switching period of this multilevel converter. The model explained in this paper uses present sources of which harmonic spectra are identified by the current flowing through the switches. The topology of this equivalent circuit is then applied to construct the state equation of the model to show accurately the operation of the inverter. This model can be used to identify the steady state mode and also the dynamic response of the capacitor voltages. Linearization of this model will also be very helpful to find the control strategy of the whole system.

Xiaoming Yuan, Herbert Stemmler, and Ivo Barbi have presented in their research paper [3], the findings of the study of current control loops of spontaneous coupled clamping capacitor and the clamping capacitor voltages resultant self balancing property of the multilevel capacitor clamped converter.

They have first analyzed the three level capacitor clamped converter under sub harmonic PWM modulation and then analyzed the multilevel capacitor clamped converter under sub harmonic PWM modulation.

From the analyses and test results, they have drawn following conclusions.

1. Due to the spontaneous clamping-capacitor-current control loop, when the load is not pure-reactive, the voltage of clamping capacitor in the three level capacitor clamped converter is self balancing under sub harmonic PWM modulation and it is similar to the nominal value. The time constant of the voltage transient of clamping capacitor increases with the clamping capacitor capacitance, the amplitude and angle of load impedance and decreases with the modulation index.
2. For multilevel capacitor clamped converter in sub harmonic PWM modulation, individual clamping capacitor of the spontaneous current control loop is coupled with remaining clamping capacitors remaining control loops by the load current. Similarly, when the load is not pure reactive the voltages of clamping capacitor are self balancing and the time constants of the transients dependent in the same relationships similar to three level inverter.

Gui-Jia Su has presented in their research paper [4], a brand new class of multilevel converters using a multilevel dc link and a bridge converter to decrease the amount of capacitors, switches, gate drivers and clamping diodes when number of voltage levels increases. This new MLDCL converters has substantially reduced number of components as a result of that cost low and become smaller size and volume. In the half bridge cells, the diode clamped or capacitor clamped phase legs and IGBT's in the single phase bridges, this new converters can be accommodate this fast switching low cost low voltage MOSFETs to lower the current and torque ripples and to increase motor efficiency by lowering the associated copper and iron losses as a result of current ripple.

3.2 Proposed Generalized Nine Level Inverter

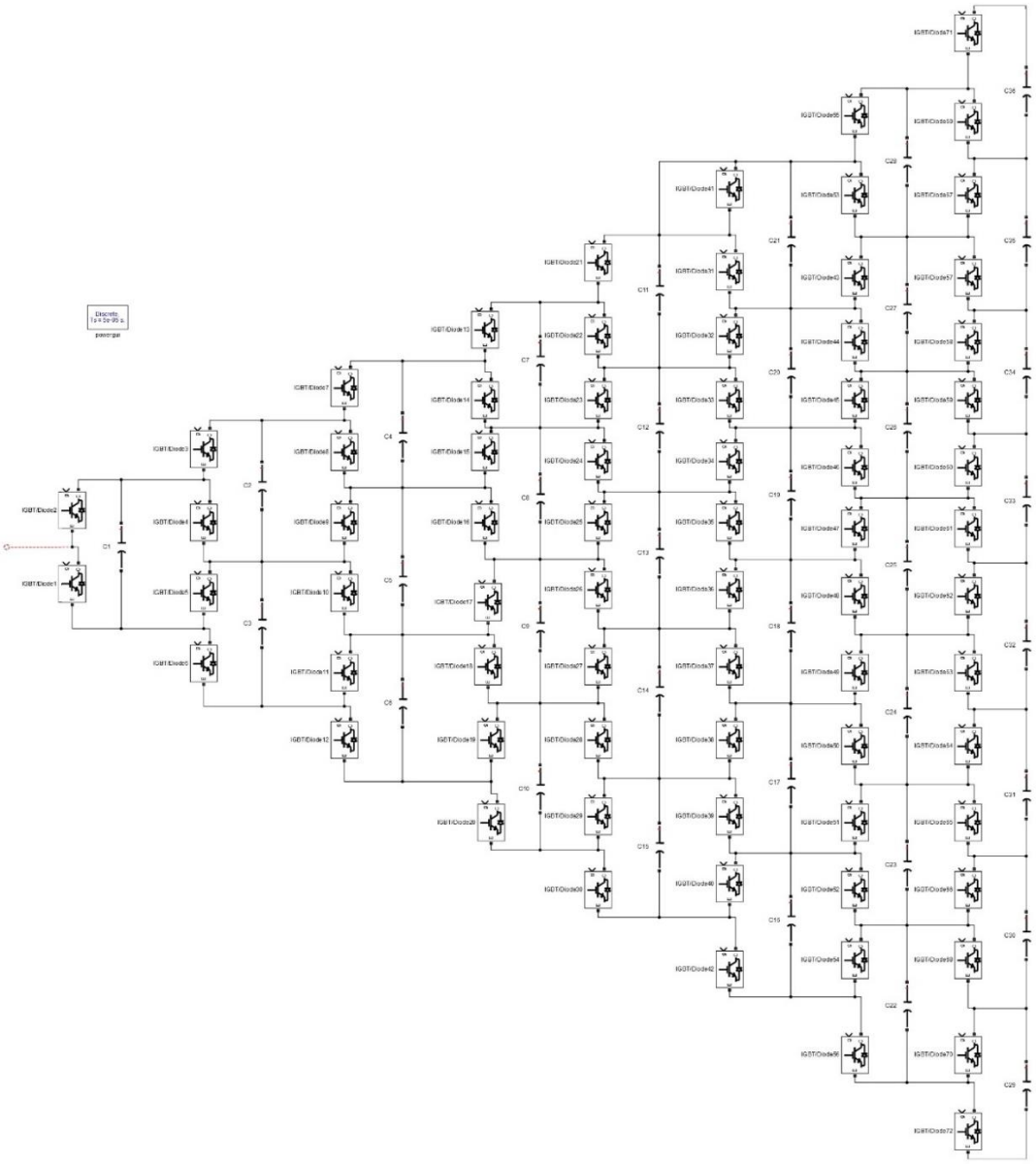

Figure 1: G9LI of a one phase

Generalized Nine Level Inverter has 3 legs for 3 phases. Each leg has 72 IGBTs and 36 capacitors. Refer to Figure 1. Also, it has separate sub circuits to create switching signals, switching time calculation and create switching signals for each phase leg.

Algorithms were written in Matlab to select the appropriate switch, based on the level of operation and mode of operation of the Generalized Multi-Level Inverter.

For all 3 legs DC supply was provided form a single DC source. And it was supplied to the top end and bottom ends of the last series of switches (9^{th} level) in each phase leg.

A separate sub circuit was created to generate switching signals and calculate switching times. These switching signals are then fed to each phase leg of the inverter.

3.3 Operation of the Generalized Nine Level Inverter

Proposed Generalized Nine Level Inverter can operate in Flying Capacitor mode, Neutral Point Clamped mode and Cascaded Half Bridge mode. As this is a nine-level inverter this inverter can be operated in 3 levels, 5 levels, 7 levels and 9 levels in each mode of operation. According to the mode of operation and number of levels, switching sub circuits are identified in each phase leg as follows,

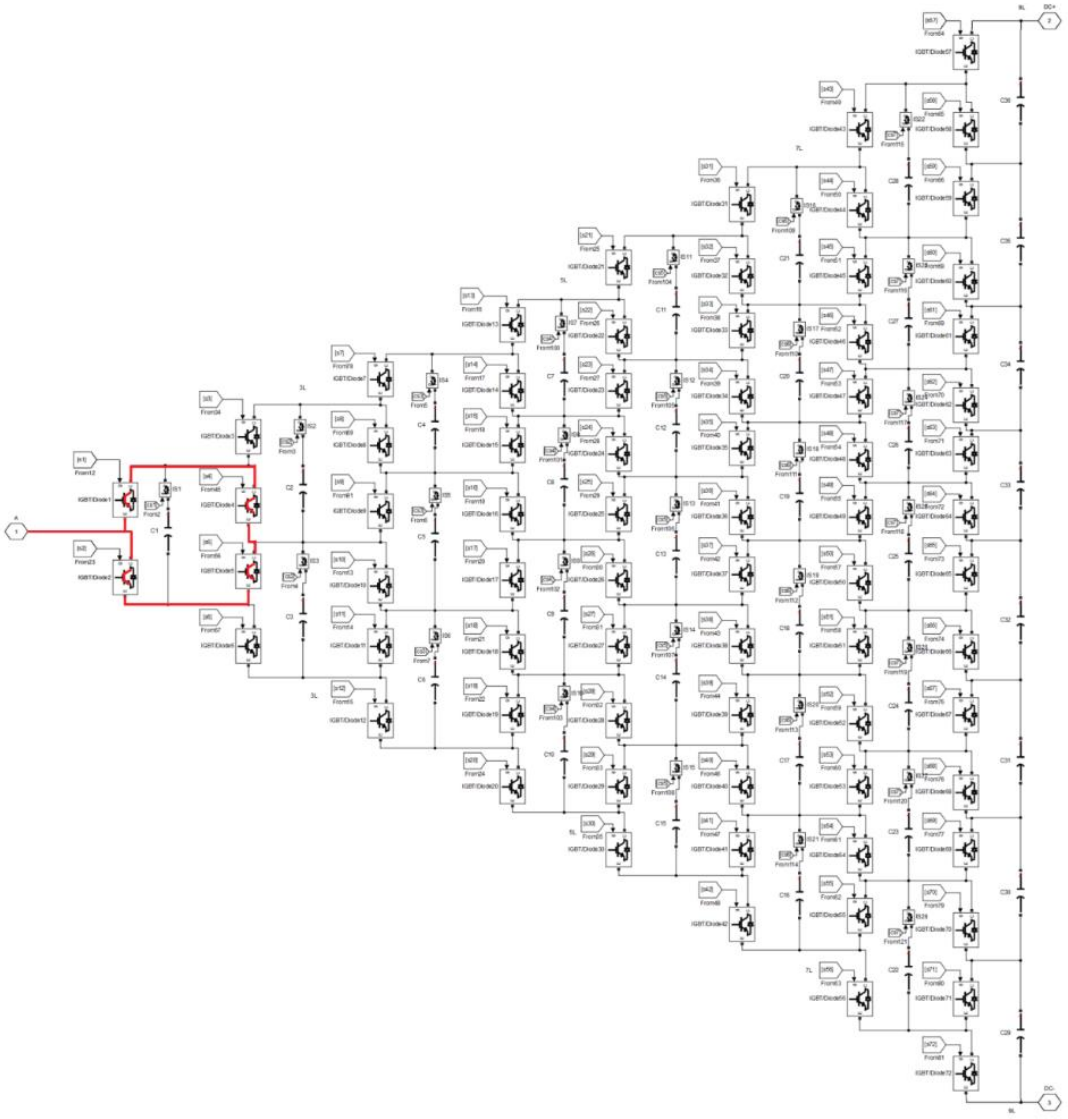

Figure 2: Sub circuit of 3 Level CHB

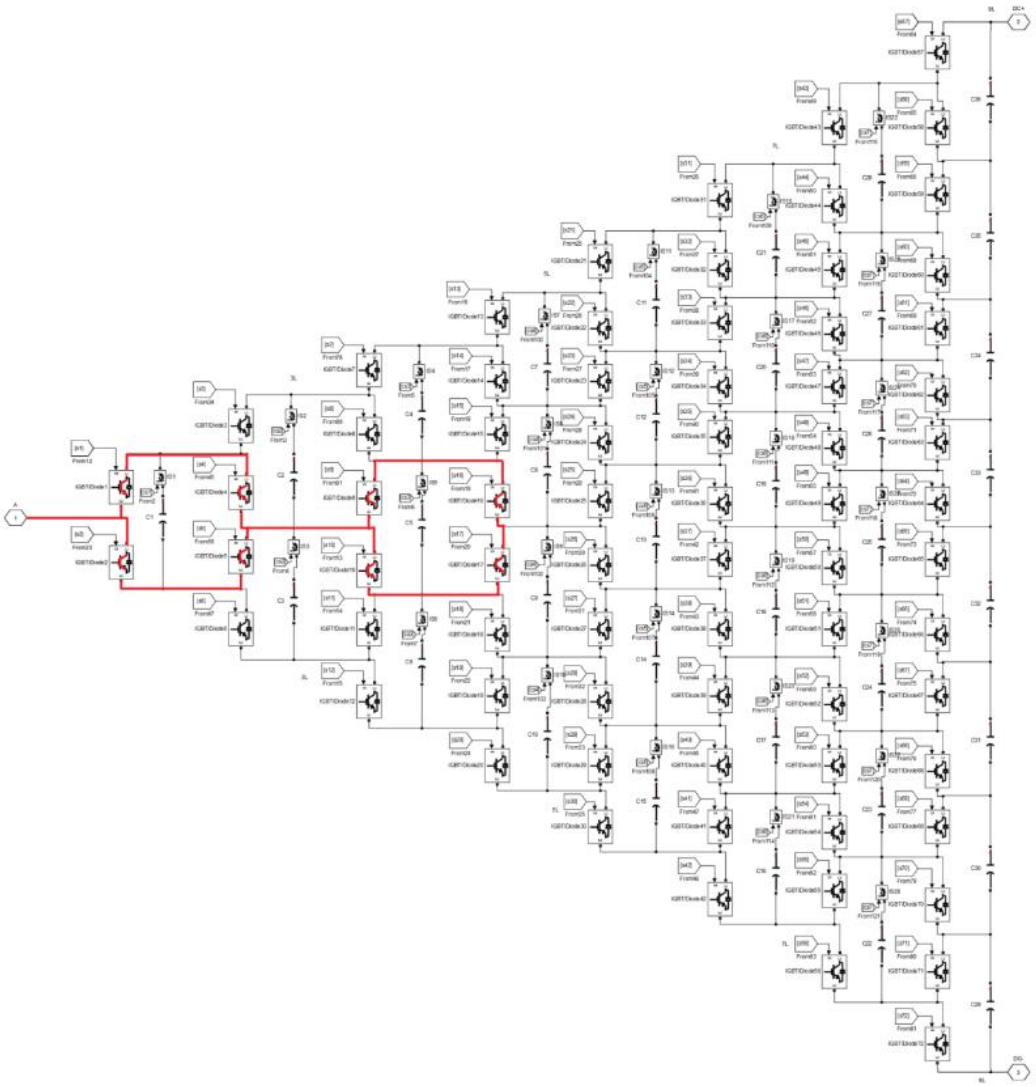

Figure 3: Sub circuit of 5 Level CHB

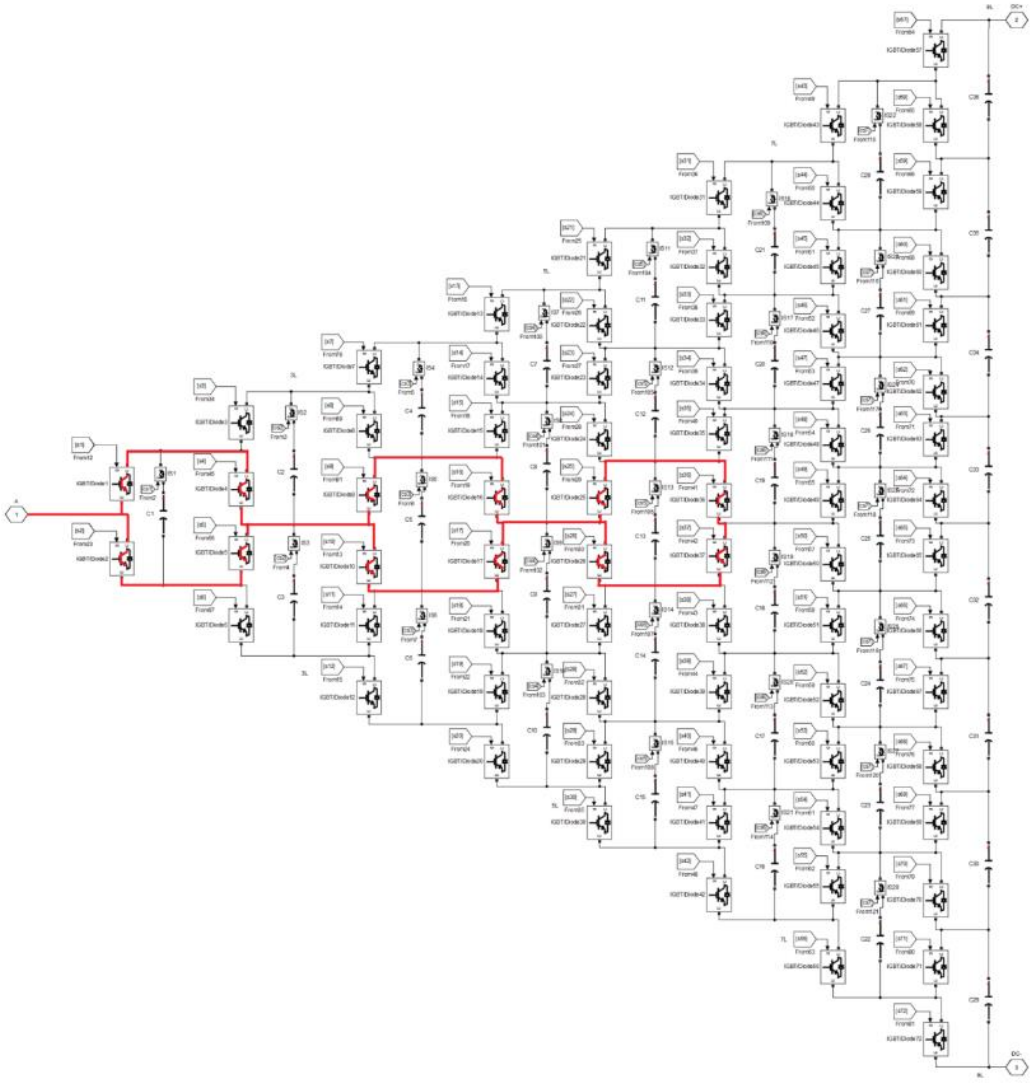

Figure 4: Sub circuit of 7 Level CHB

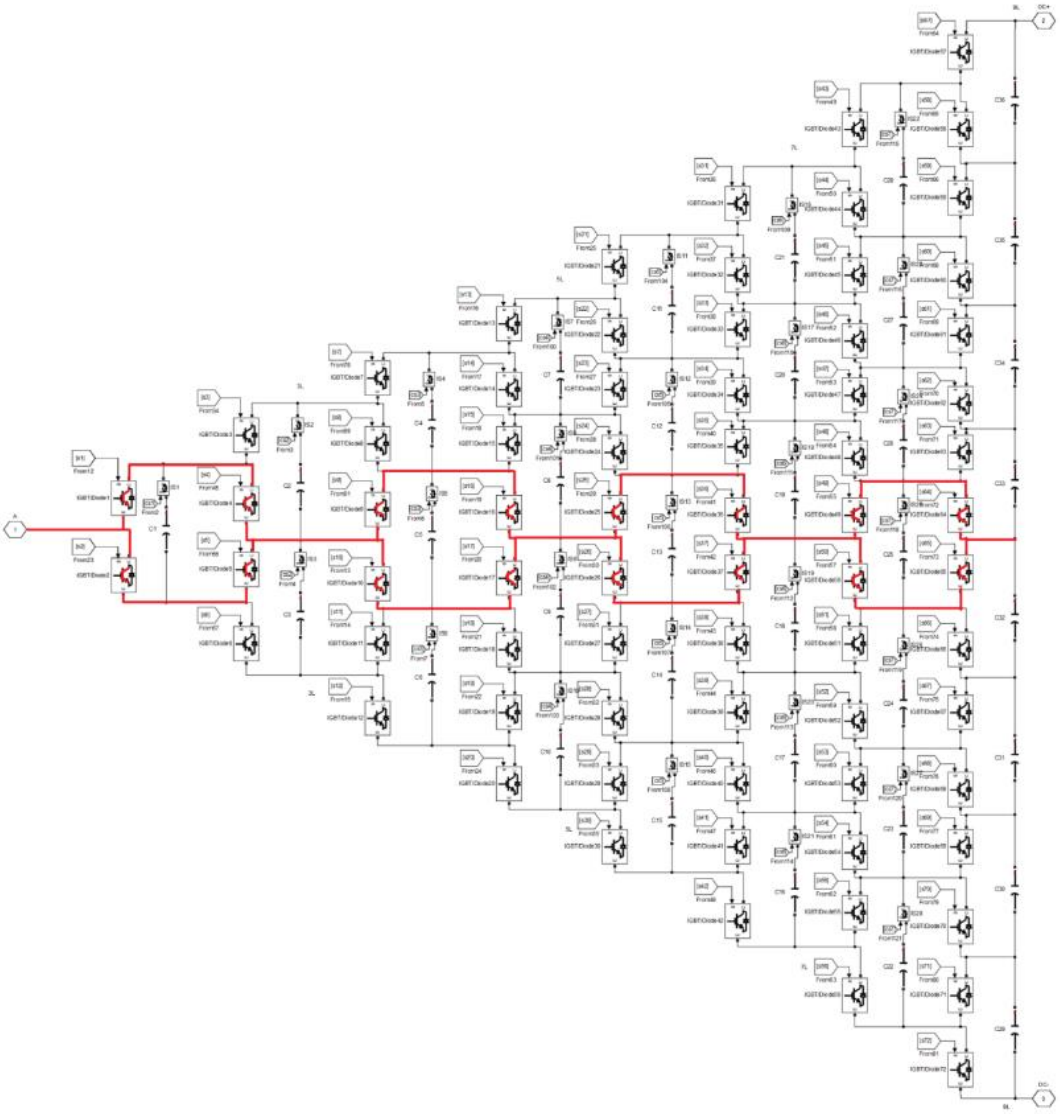

Figure 5: Sub circuit of 9 Level CHB

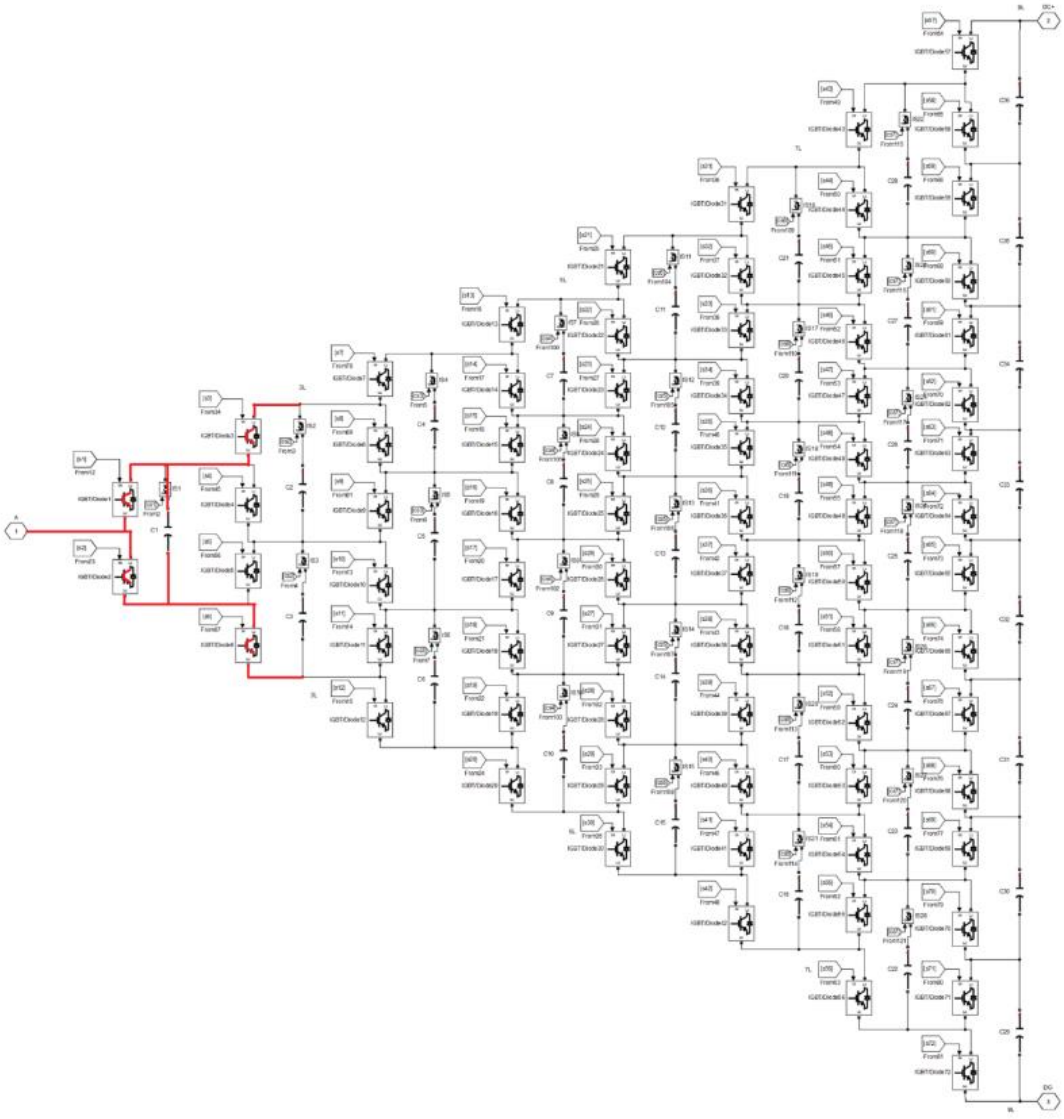

Figure 6: Sub circuit of 3 Level FC

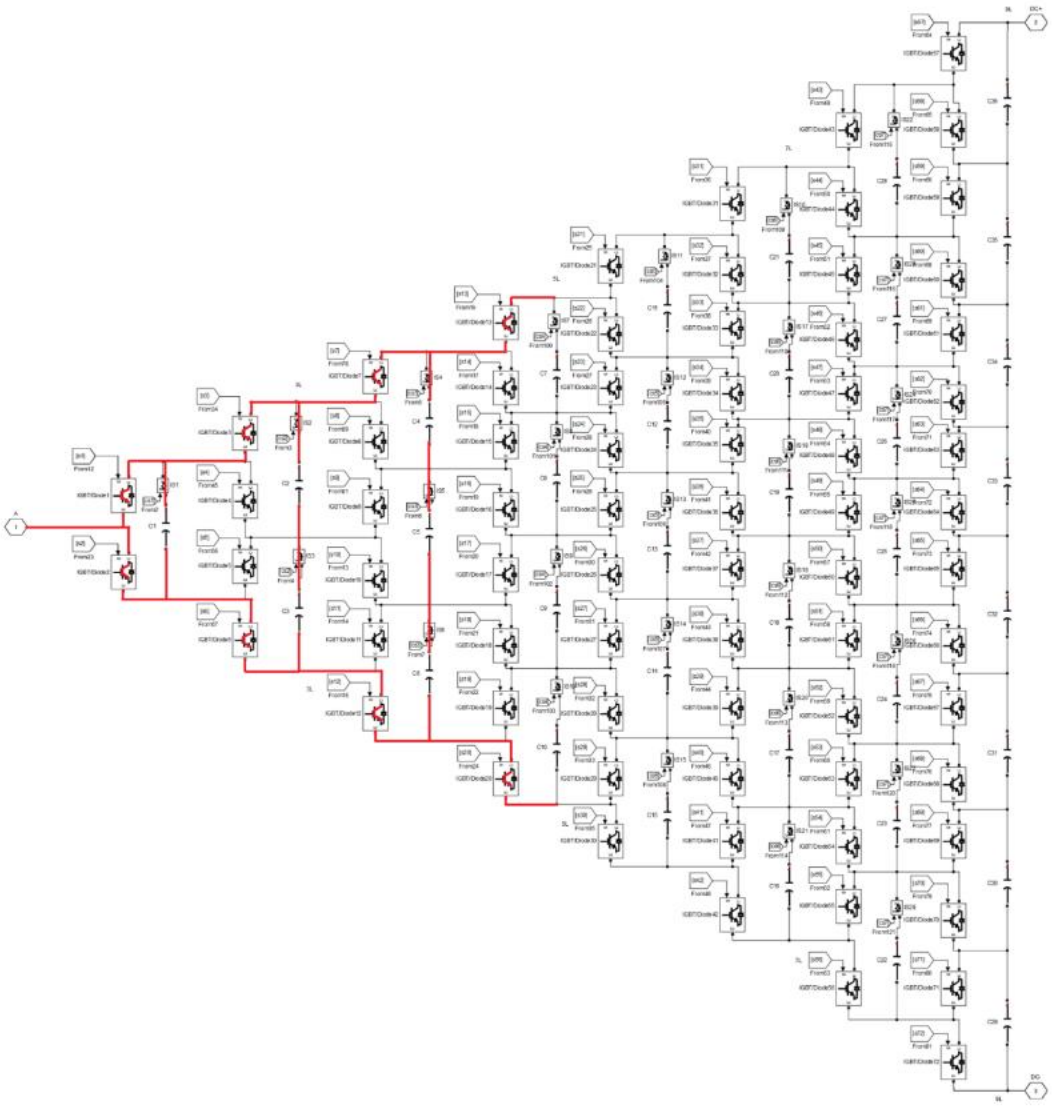

Figure 7: Sub circuit of 5 Level FC

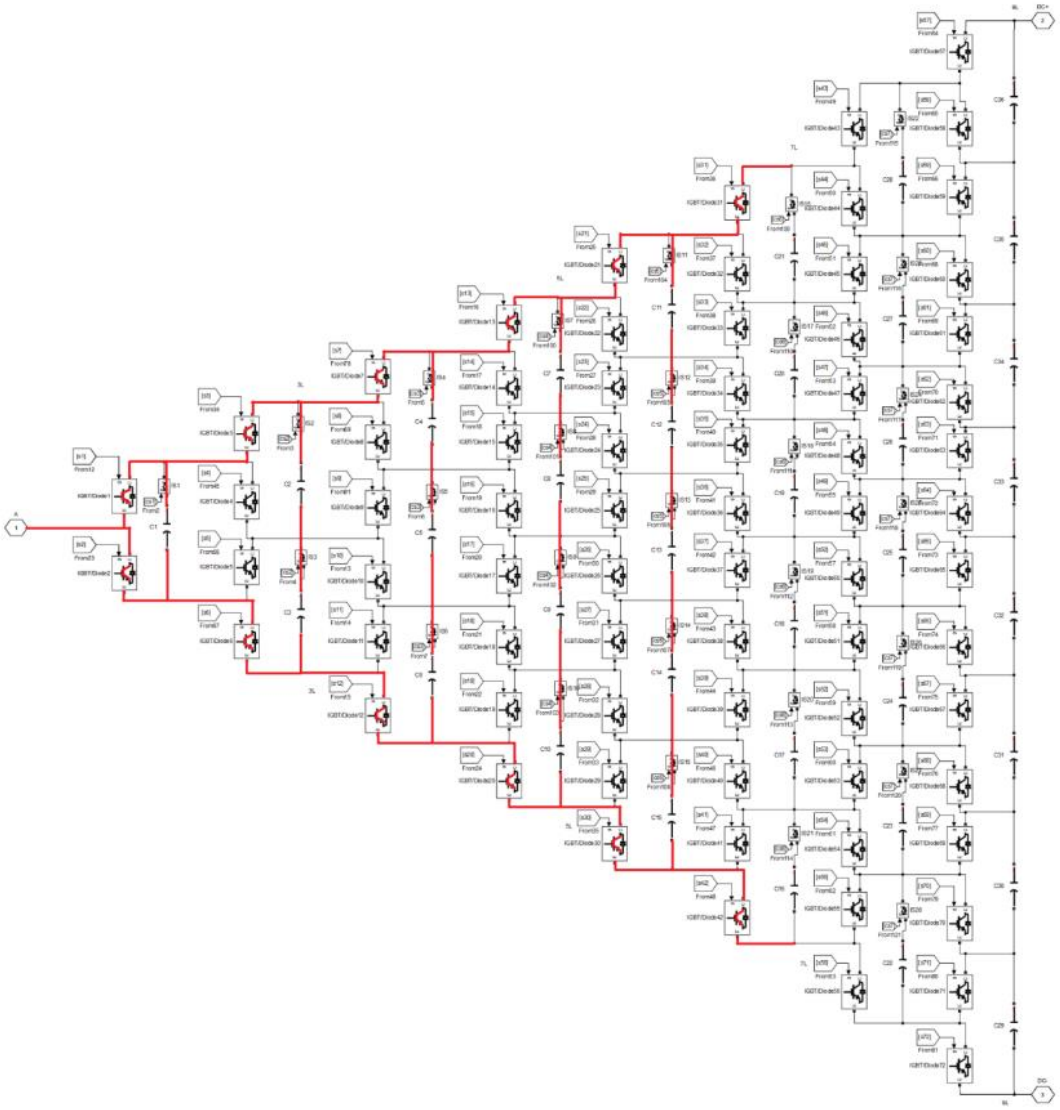

Figure 8: Sub circuit of 7 Level FC

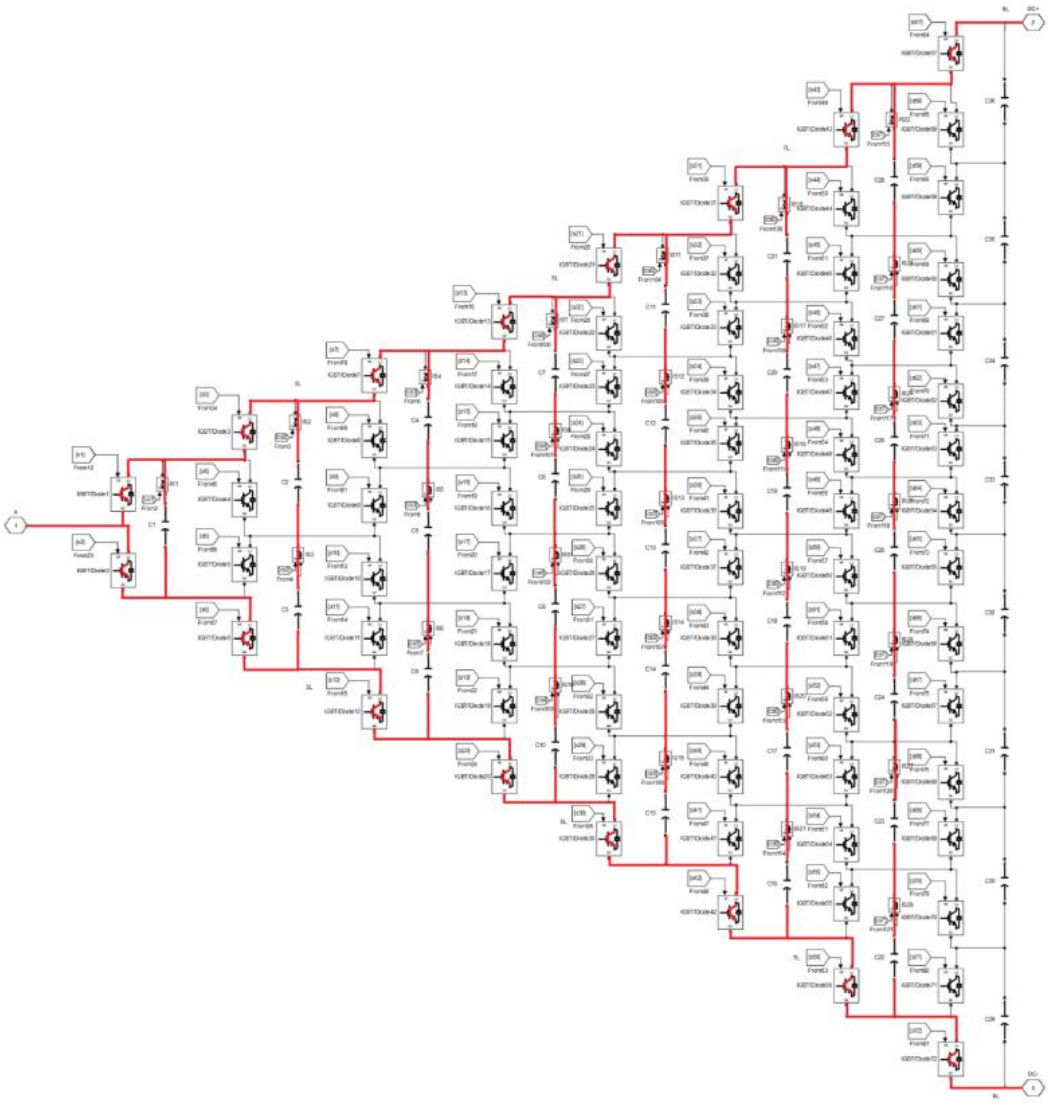

Figure 9: Sub circuit of 9 Level FC

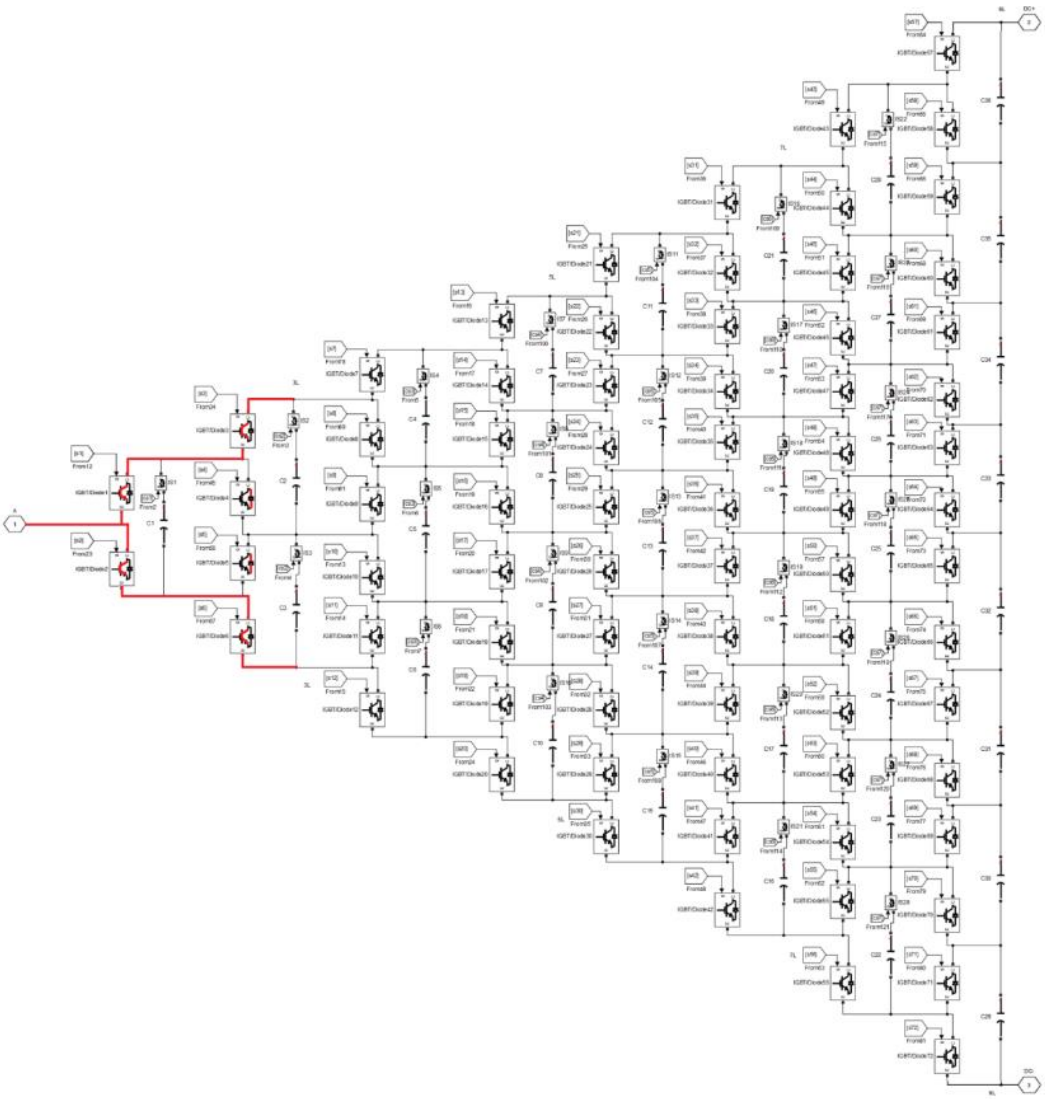

Figure 10: Sub circuit of 3 Level NPC

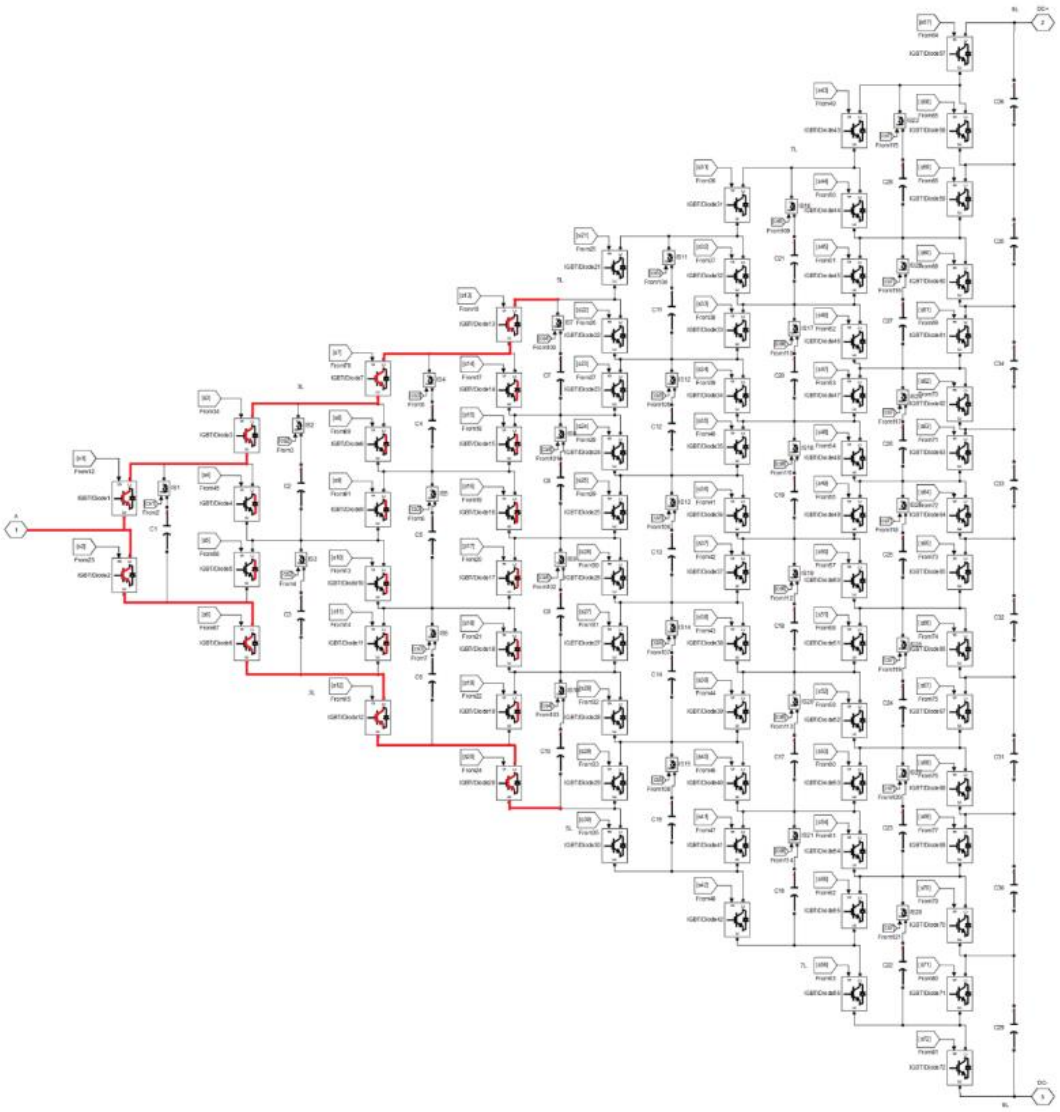

Figure 11: Sub circuit of 5 Level NPC

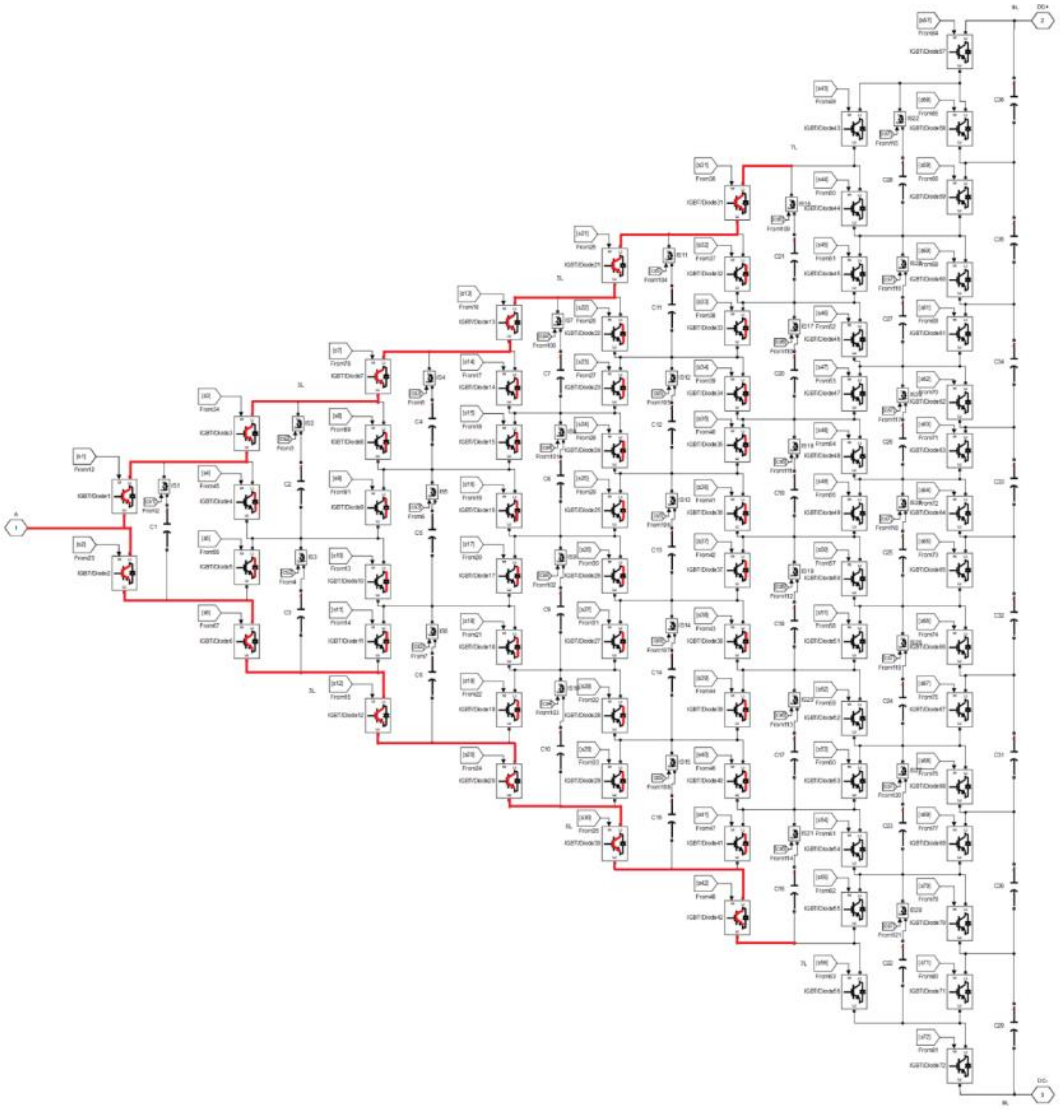

Figure 12: Sub circuit of 7 Level NPC

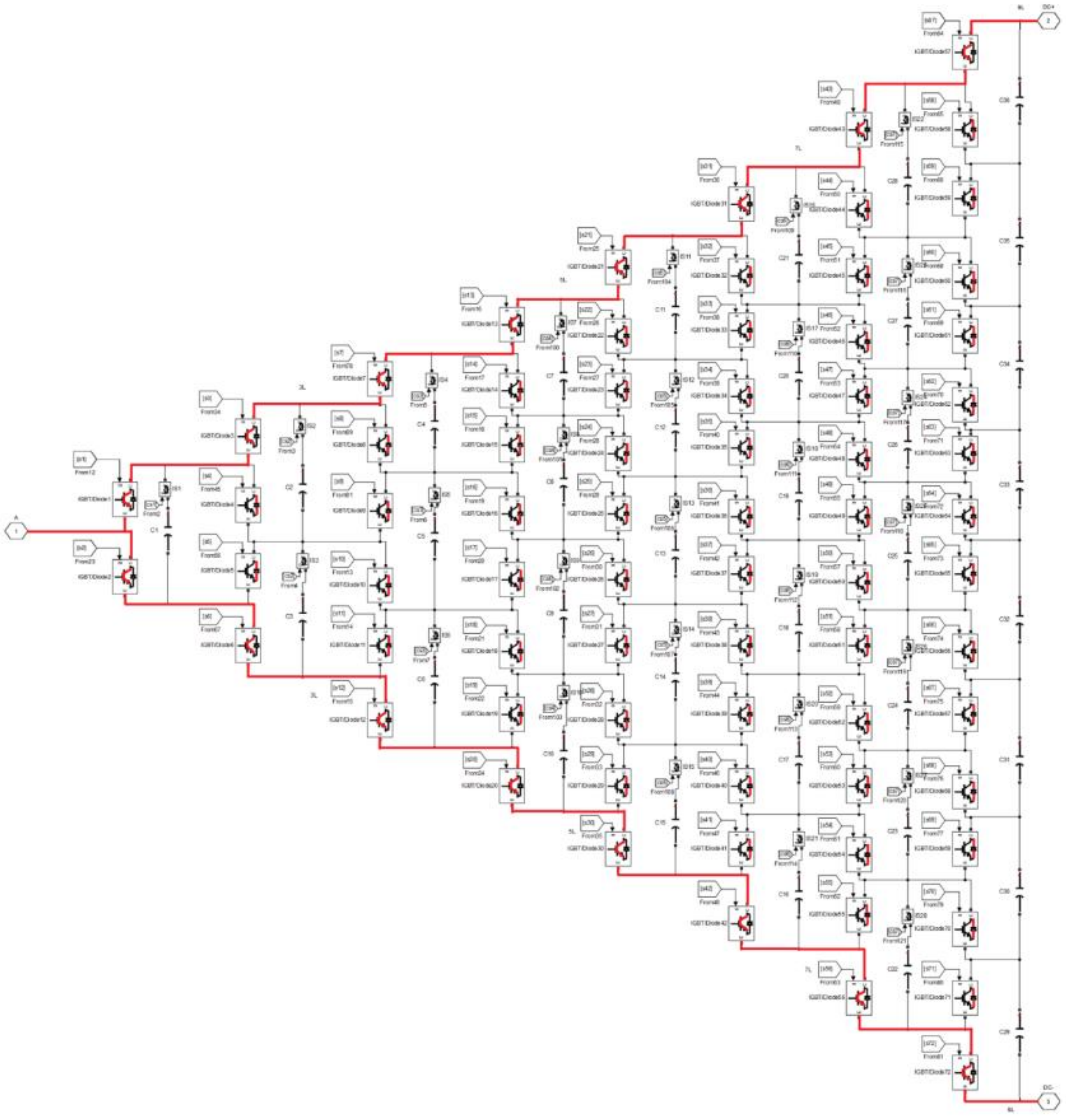

Figure 13: Sub circuit of 9 Level NPC

To accomplish this task Generalized Nine Level Inverter consists of several sub circuits.

“Switching Signal and Time Calculator” sub circuit generates the switching signals for 72 numbers of IGBT switches in each phase leg. Also, this sub circuit generates the time signals required by each phase leg to provide timing information for the Space Vector Pulse Width Modulation for each phase leg.

The generated signals were then fed to power module and the power module allocates these switching signals to the relevant phase leg. Power module also consists of the DC power source to provide DC supply to each phase leg.

Each phase leg contains a Generalized Nine Level Inverter and the output voltage produced based on the switching signals received is fed to the Star connected load.

3.4 Generalized Nine Level Inverter Control

Space Vector Pulse Width Modulation is used by the proposed Generalized Nine Level Inverter to generate the required output signals.

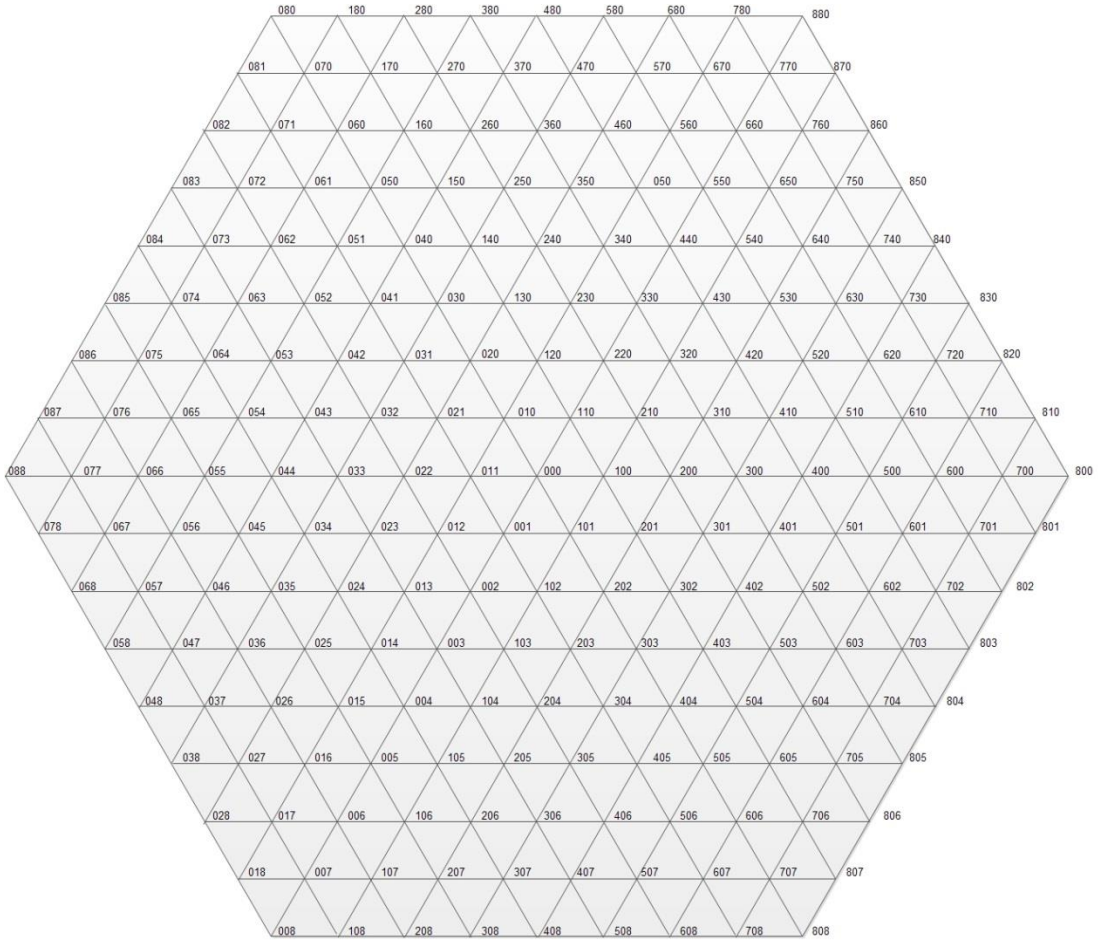

Figure 14: SV Diagram of G9LI

Generalized Nine Level Inverter can synthesize output voltage form 9 discrete voltage levels. Each switching state produces a define set of three phase sinusoidal voltages, which can be represented as vectors.

Space vector diagram of the Generalized Nine Level Inverter when operated as 3 levels, 5 levels, 7 levels and 9 levels have 27, 64, 343 and 729 vectors respectively. These vectors are relevant to the line to line voltages of the inverter.

The Space Vector Diagram of the 9 level converter is spread into sectors and each sector is then spread into 64 triangular regions to visualize the vectors nearest to the reference.

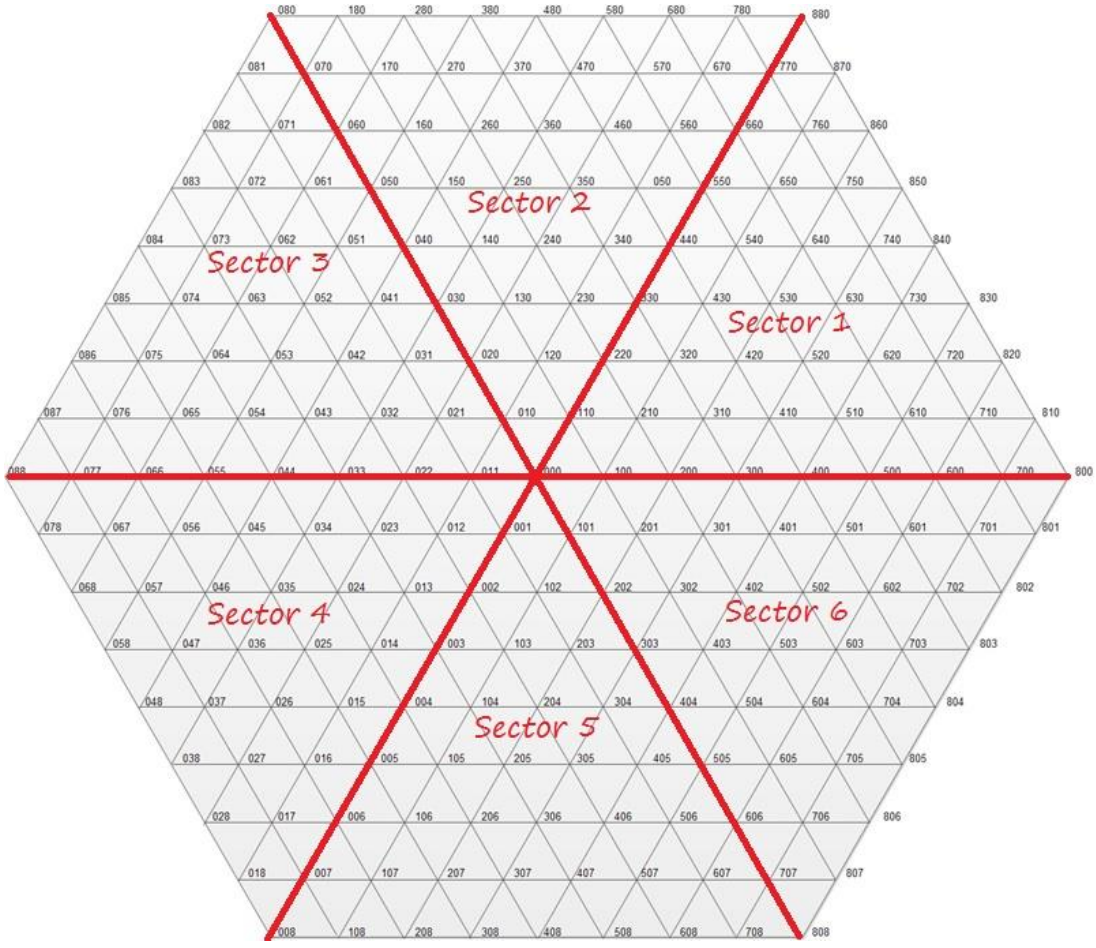

Figure 15: Six sectors of SV Diagram of G9LI

In the Space Vector Modulation, a reference vector is generated in the identical plane for each cycle of modulation. As this inverter is operated at steady state condition, the reference vector rotates at constant angular velocity, which defines the frequency of the output signals which is 50 Hz. Voltage vector has constant amplitude 3Vm/2 and rotates counter clockwise at ω. When space vector falls within ± 30 deg. of inverter vector, switching happens between that vector & zero vector at frequency fs (1kHz).

Once the V_{ref} is matched with the discrete switching states, the relevant reference voltage is simulated at the inverter output. Refer Figure 16.

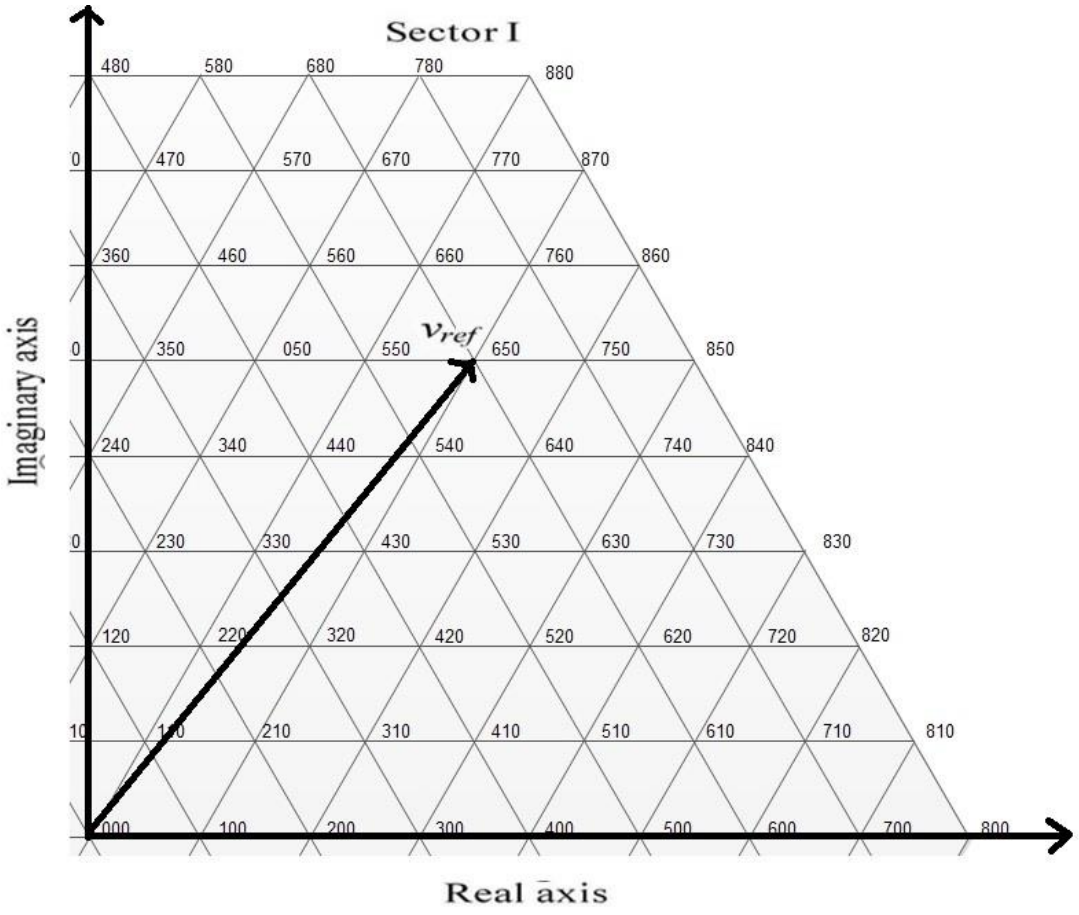

Figure 16: Reference vector in sector 1

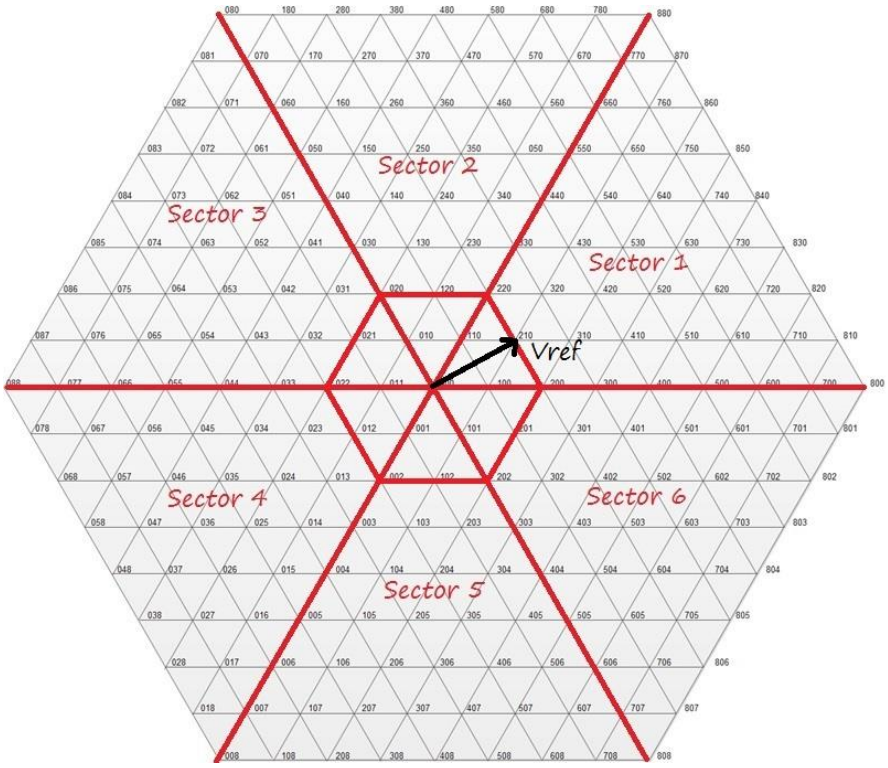

Figure 17: SV Diagram and Ref. Vector of 3 Level PWM

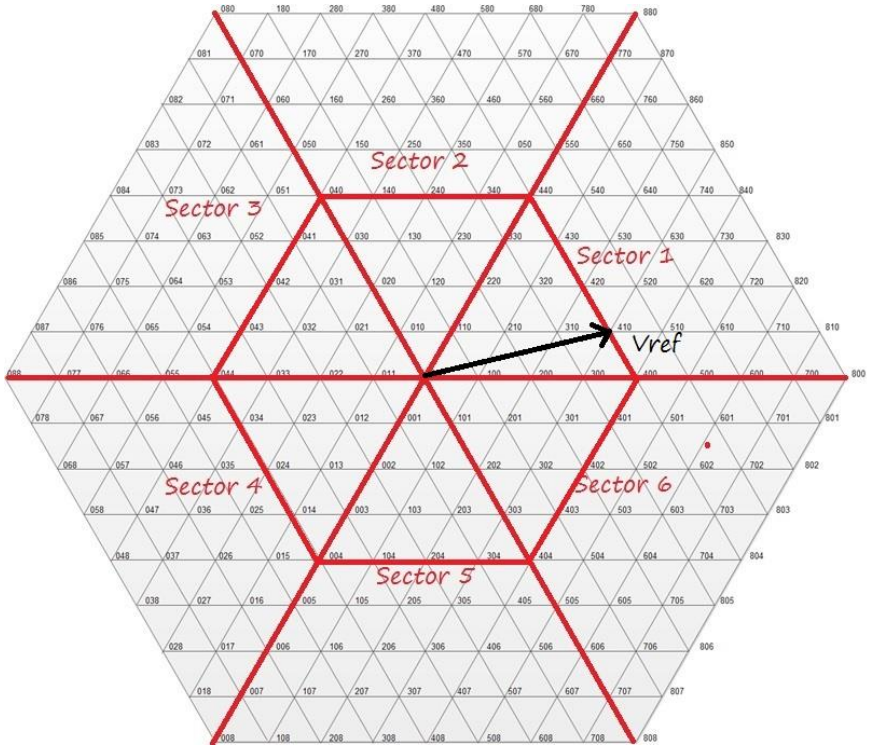

Figure 18: SV Diagram and Ref. Vector of 5 Level PWM

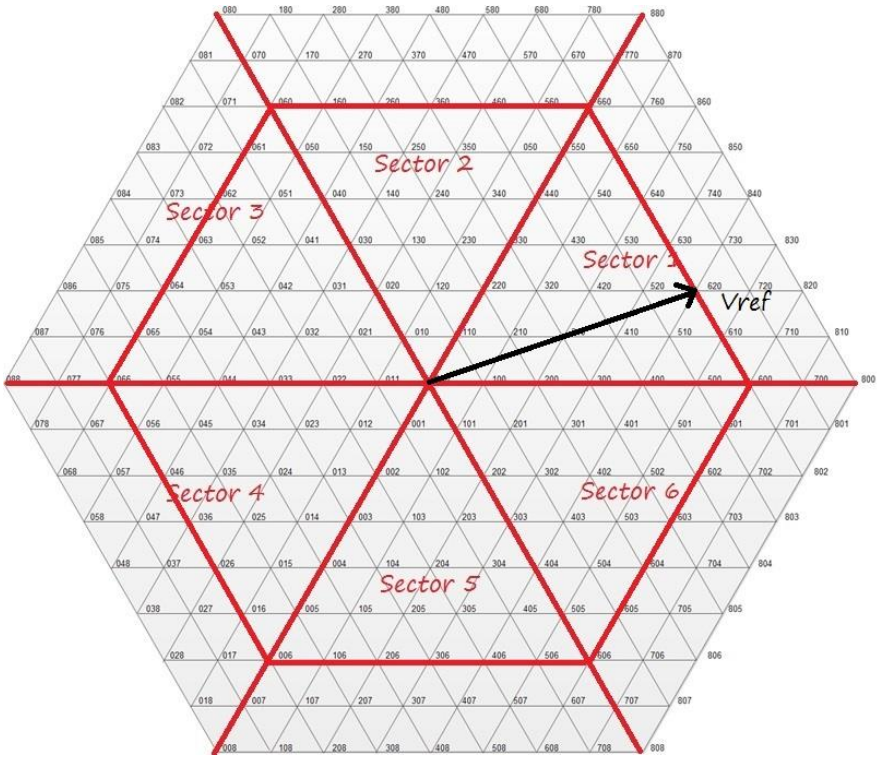

Figure 19: SV Diagram and Ref. Vector of 7 Level PWM

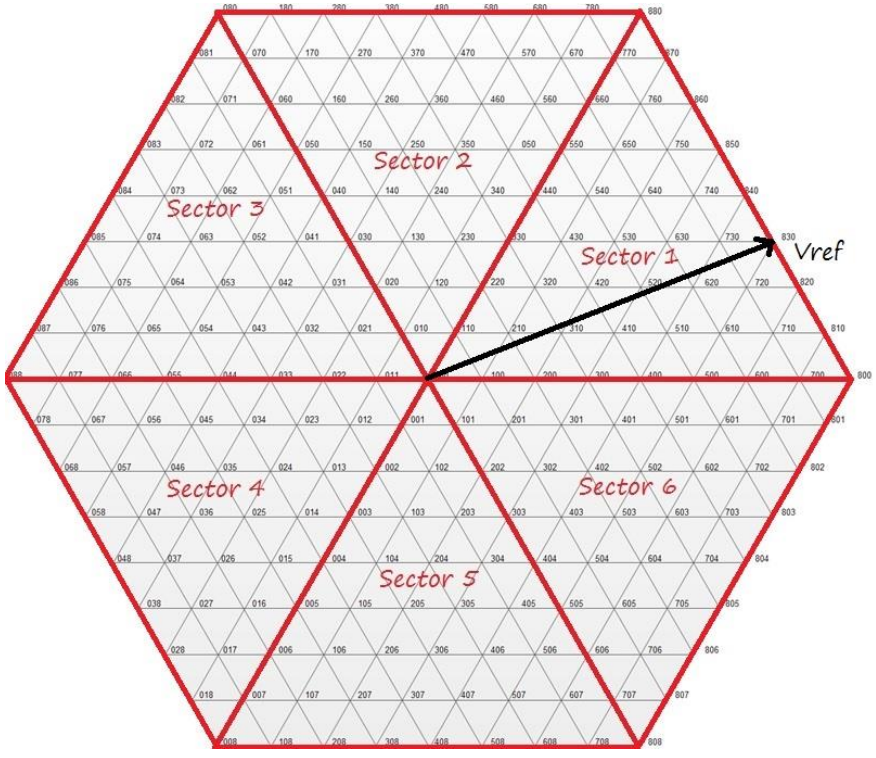

Figure 20: SV Diagram and Ref. Vector of 9 Level PWM

In the Space vector Diagram, there are redundant vectors which produce the same line to line voltages. As an example, when the inverter is operated as a three-level inverter it has six double vectors and one triple vector in the origin. These redundant vectors are utilized to achieve capacitor voltages balance, minimize the switching frequencies of IGBTs, improve the quality of the output voltage spectra and to reduce the electromagnetic interference (EMI).

4. SIMULATION OF THE GENERALIZED NINE LEVEL INVERTER

4.1 Generalized Nine Level Inverter Simulation

Matlab Simulink R2020a software package has been used for the simulation of the Generalized Nine Level Inverter.

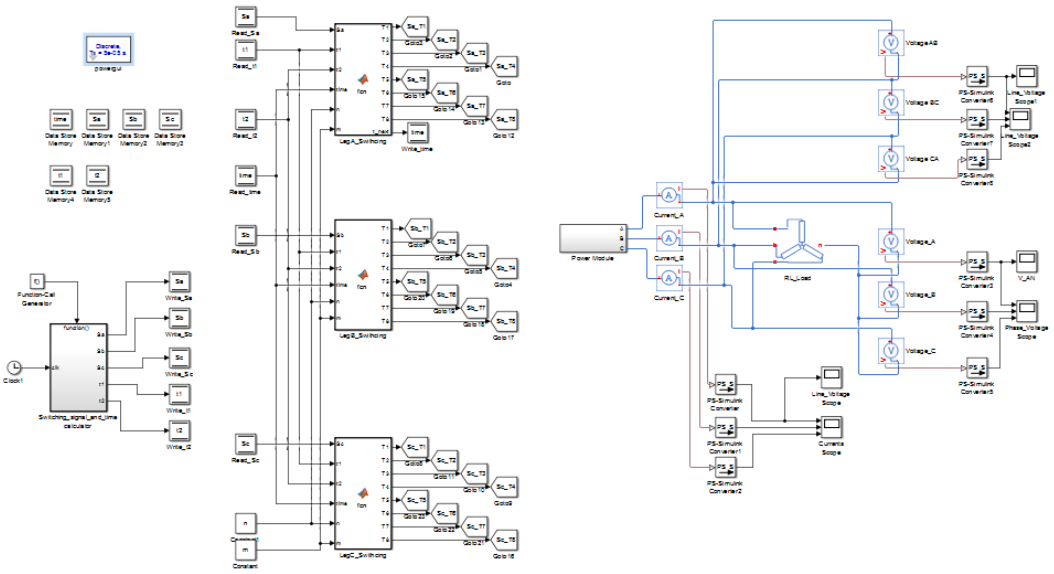

Figure 21: Simulated Generalized Nine Level Inverter Model

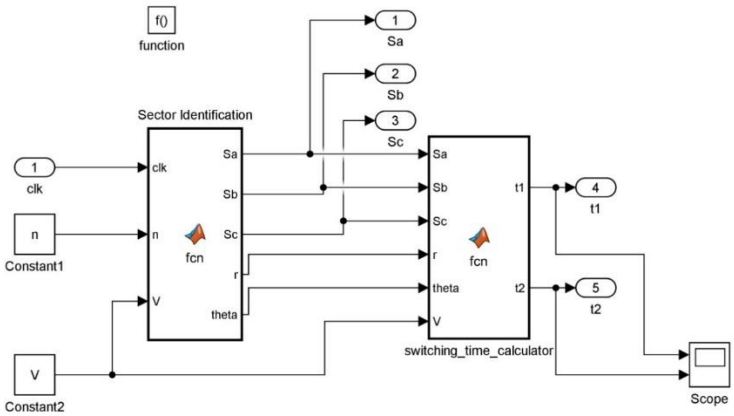

Figure 22: Switching signal and timing calculation sub circuit

The circuit diagram of power module is shown in Figure 23. Power module has DC power sources which feed DC power to the 3 phases of the inverter.

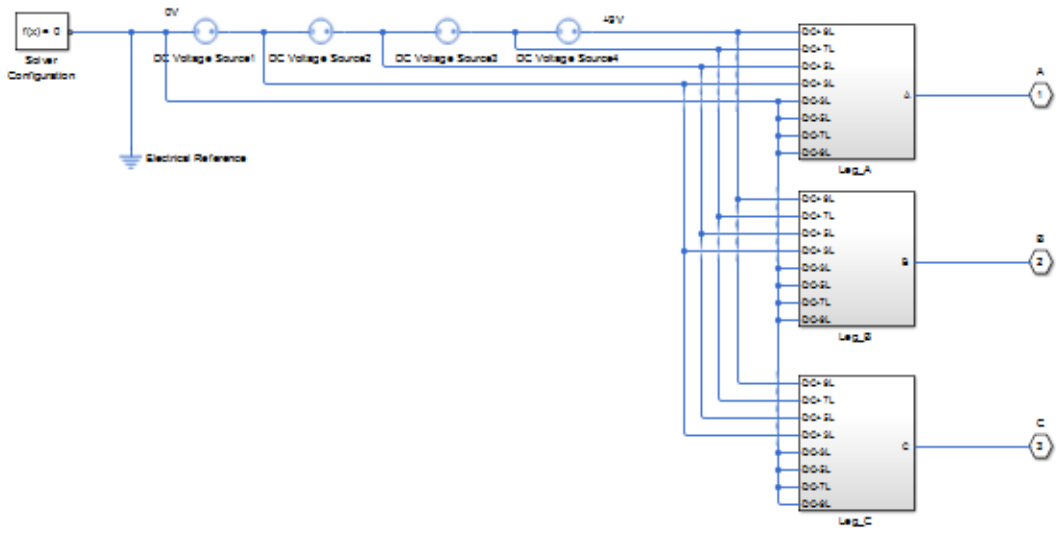

Figure 23: DC source connection for 3 phases sub circuits

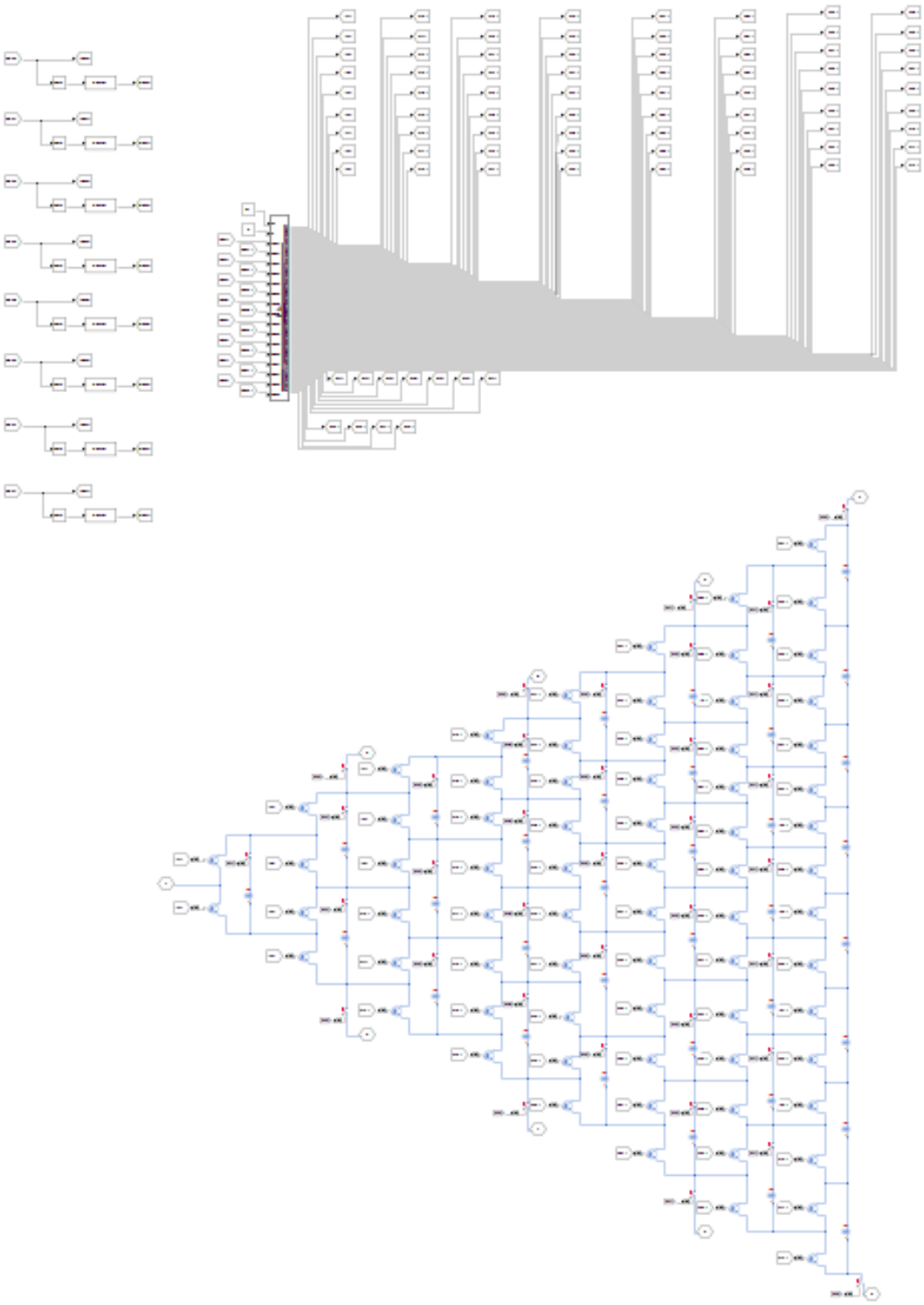

Figure 24: Simulated model of a phase consists of G9LI and the sub circuit handling switching signals

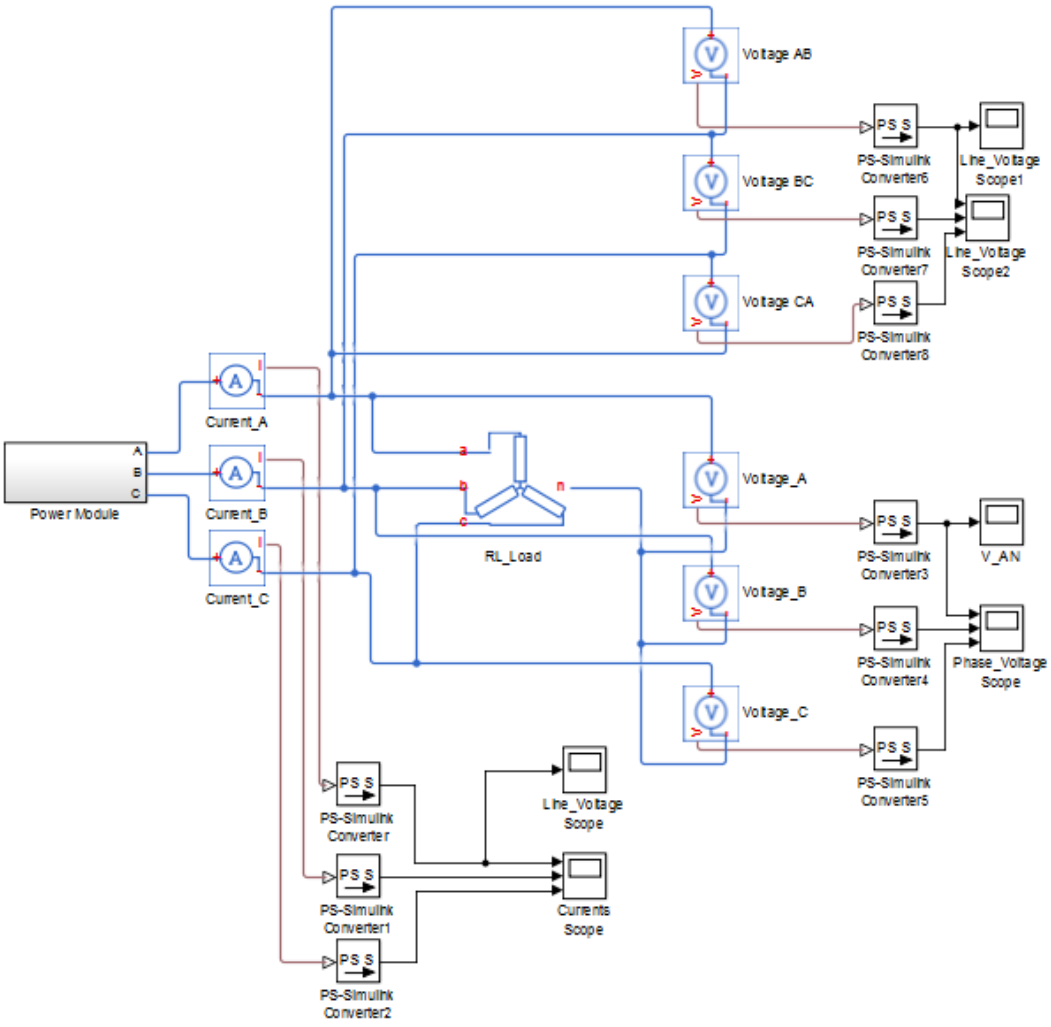

Figure 25: Power Module of the G9LI

A 3-phase star connected resistive and inductive load is attached to the Power Module of the Generalized Nine Level Converter as shown in Figure 25.

Matlab code in Figure 26 use to identify sectors in the Space Vector Diagram.

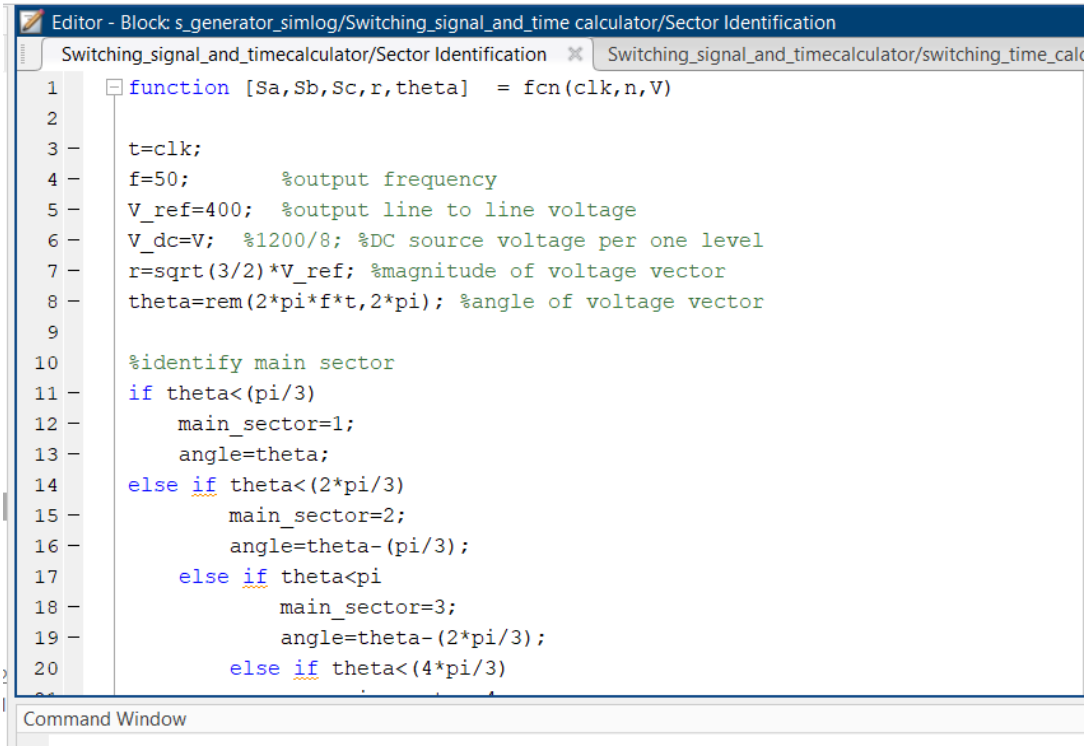

Figure 26: Matlab Simulink code for sector identification

Matlab code in Figure 27 use to calculate switching cycle time and time duration allocated for adjacent two vectors in a triangular region of Space Vector Diagram.

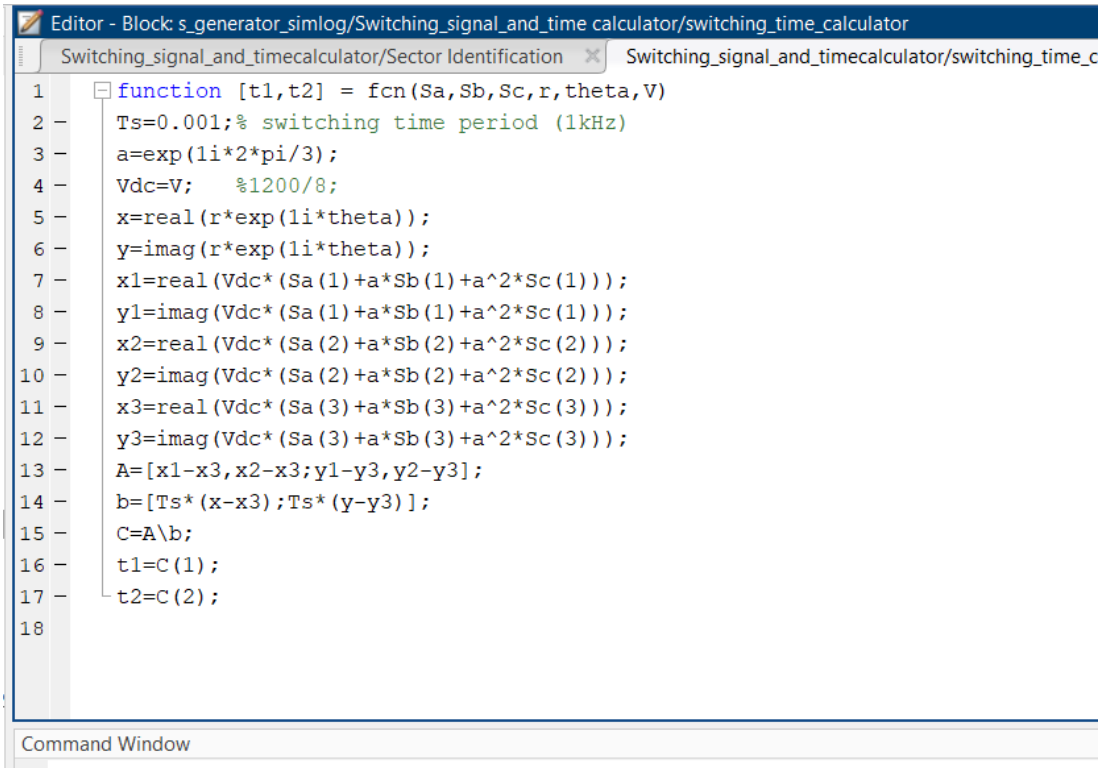

Figure 27: Matlab-Simulink program for Switching Time Calculator

Matlab code in Figure 28 use the switching signals S_a, S_b and S_c and time values t_1 and t_2 generated from Sector Identification and Time Calculator sub circuit to generate switching signals to be fed to Power Module to inform the voltage level the inverter should be operated.

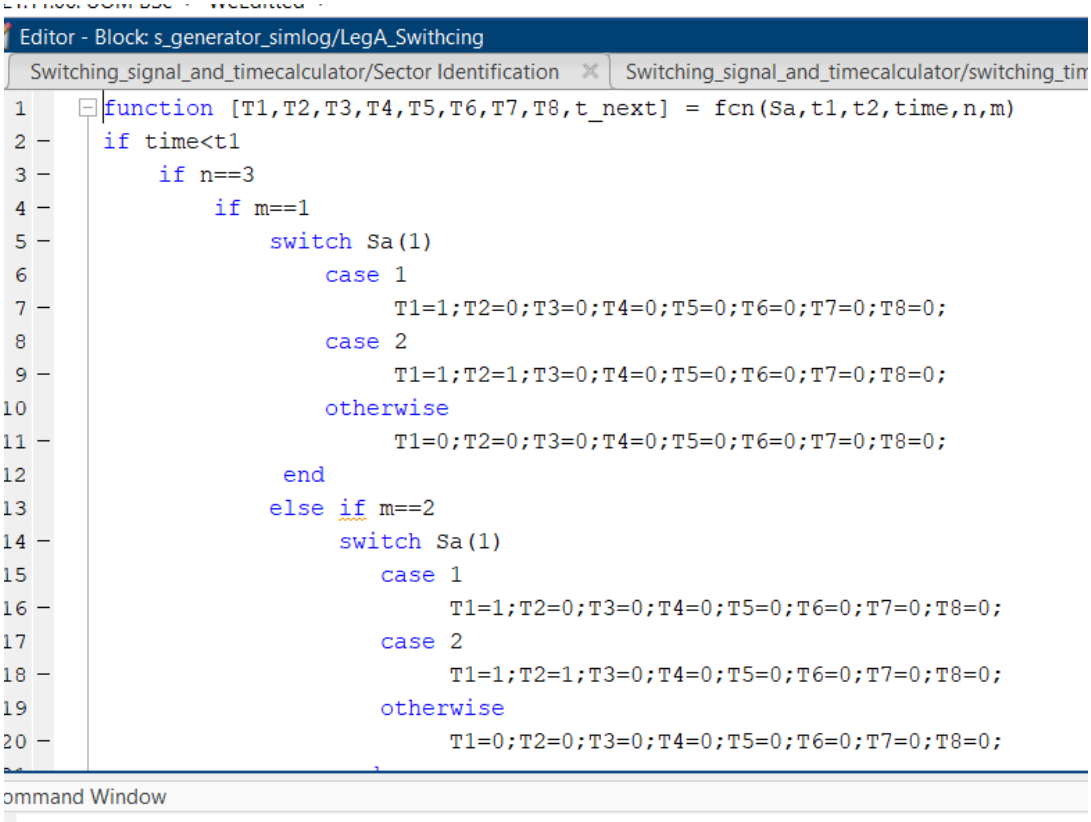

Figure 28: Matlab Simulink program to generate switching signals for 9 levels of a phase

Matlab code in Figure 29 generate switching signals for IGBTs in Generalized Nine Level Inverter to operate in Flying Capacitor, Neutral Point Clamp and Cascaded Half Bridge modes.

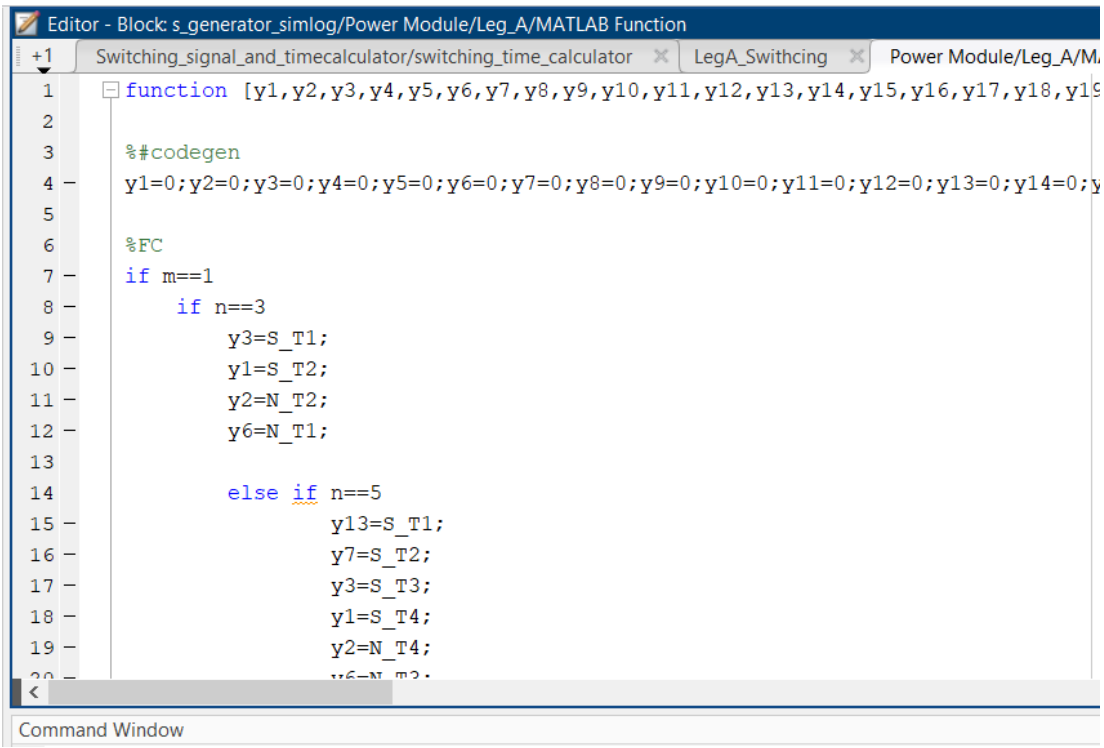

Figure 29: Matlab-Simulink program to generate switching signals for mode of operation (FC, NPC and CHB) for each IGBT of a phase leg

5. SIMULATION RESULTS

5.1 Pulse Width Modulation

Voltage and current graphs of Generalized 9 Level converter operated in 3 level Pulse Width Modulation is shown in Figure 30 and 31 respectively.

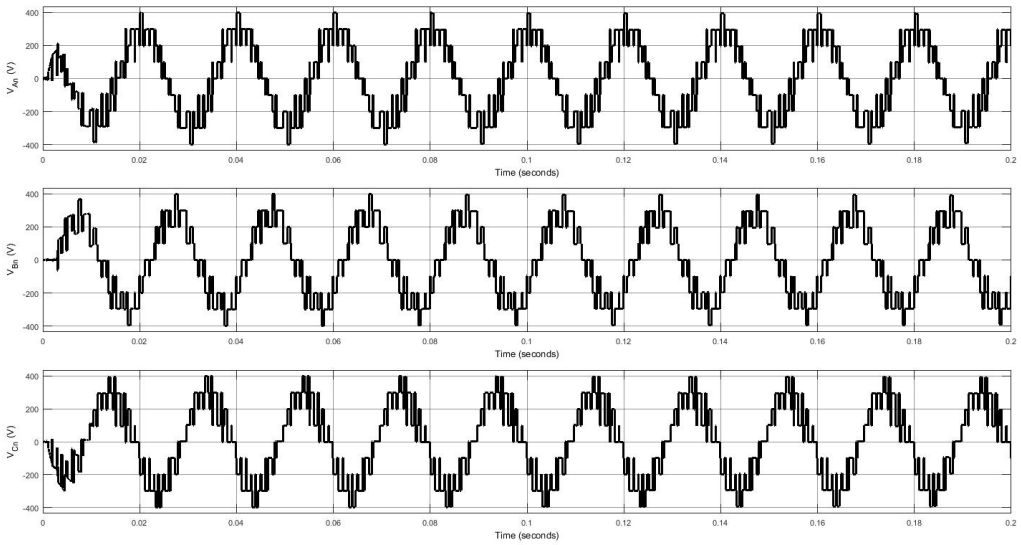

Figure 30: 3 Level Inverter Voltage Graphs in PWM

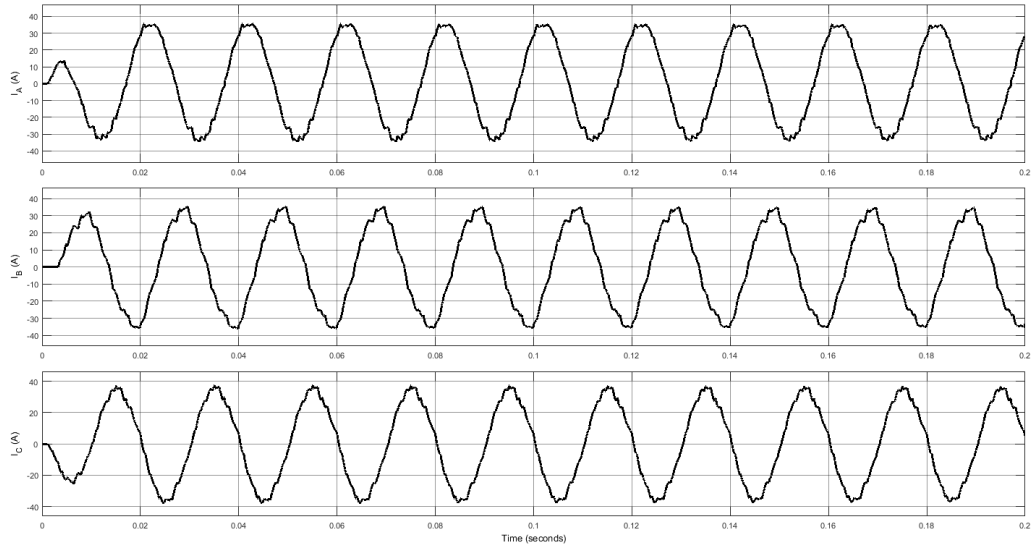

Figure 31: 3 Level Inverter Current Graphs in PWM

Voltage and current graphs of Generalized 9 level Inverter operated in 5 level Pulse Width Modulation is shown in Figure 32 and 33 respectively.

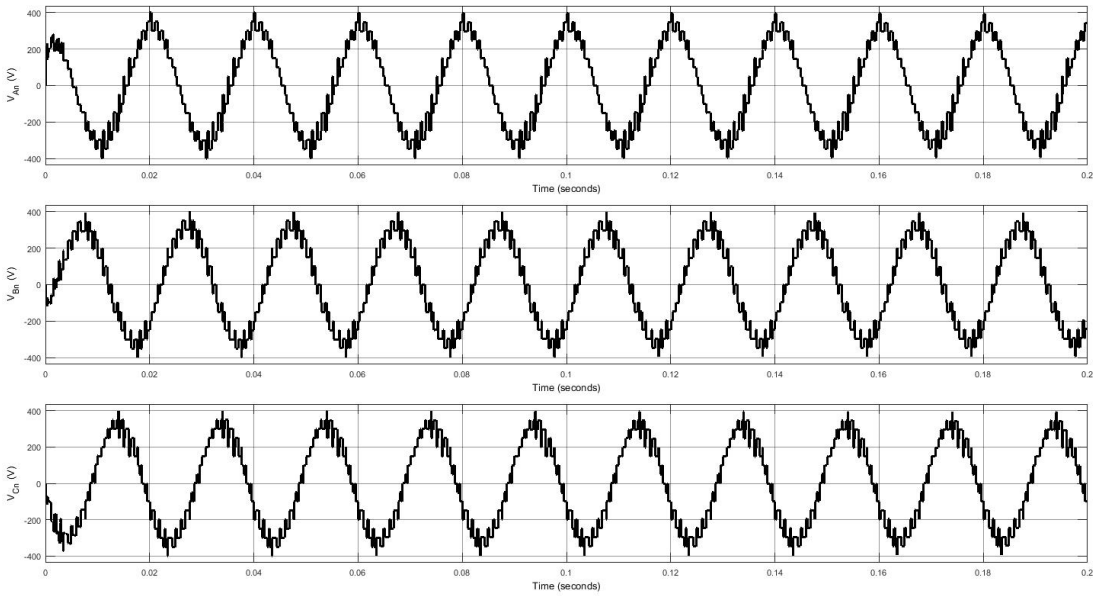

Figure 32: 5 Level Inverter Voltage Graphs in PWM

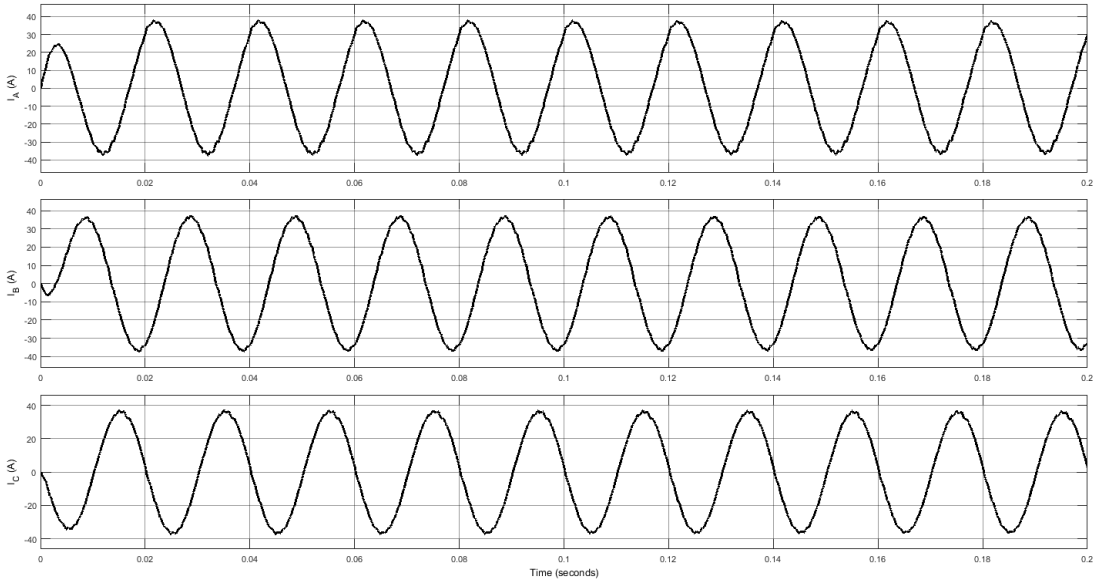

Figure 33: 5 Level Inverter Current Graphs in PWM

Voltage and current graphs of Generalized 9 level converter operated in 7 level Pulse Width Modulation is shown in Figure 34 and 35 respectively.

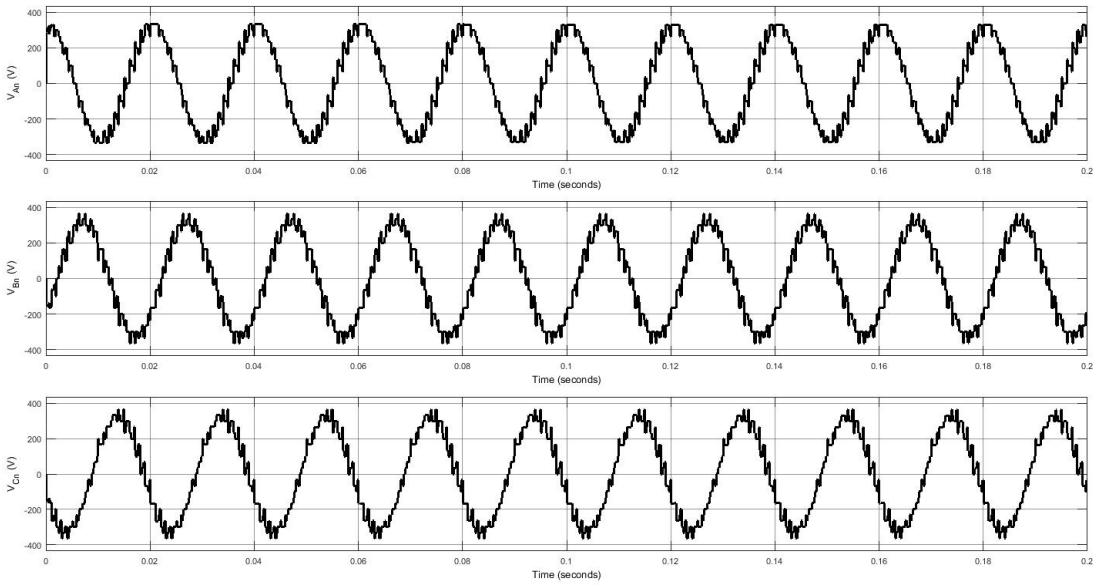

Figure 34: 7 Level Inverter Voltage Graphs in PWM

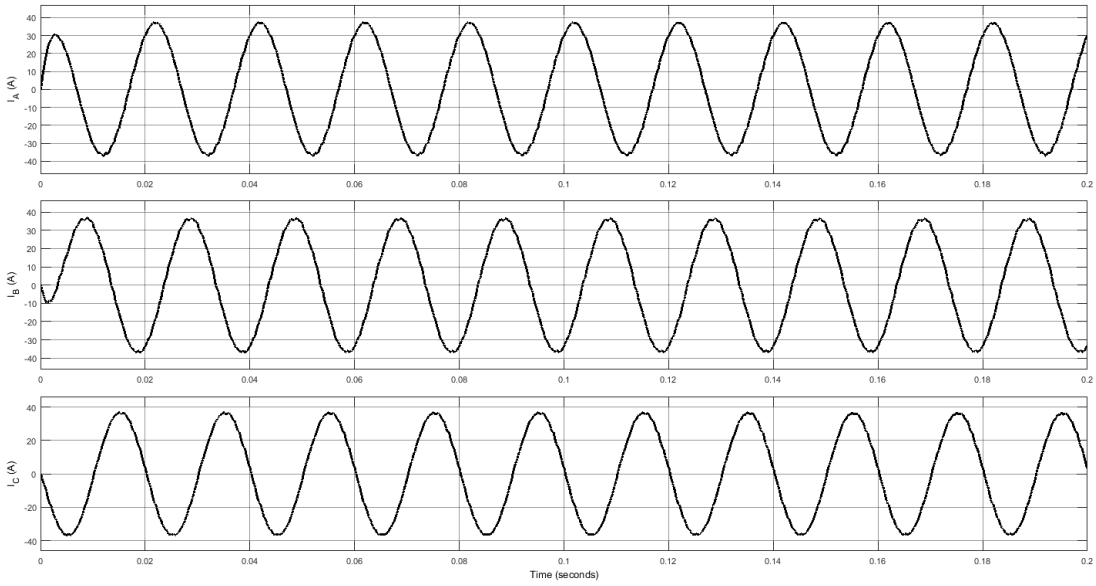

Figure 35: 7 Level Inverter Current Graphs in PWM

Voltage and current graphs of Generalized 9 level converter operated in 9 level Pulse Width Modulation is shown in Figure 36 and 37 respectively.

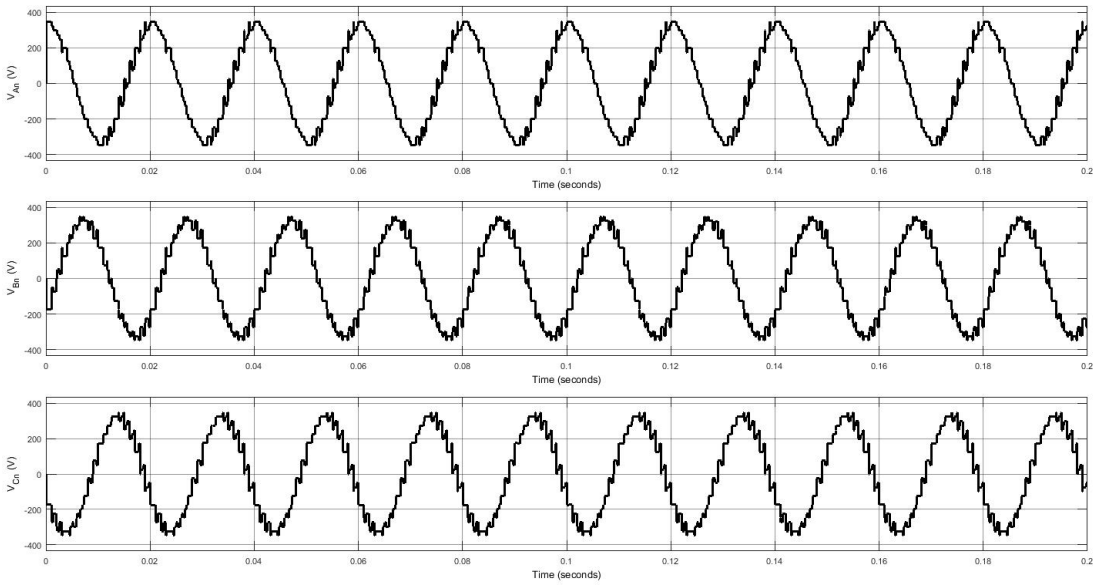

Figure 36: 9 Level Inverter Voltage Graphs in PWM

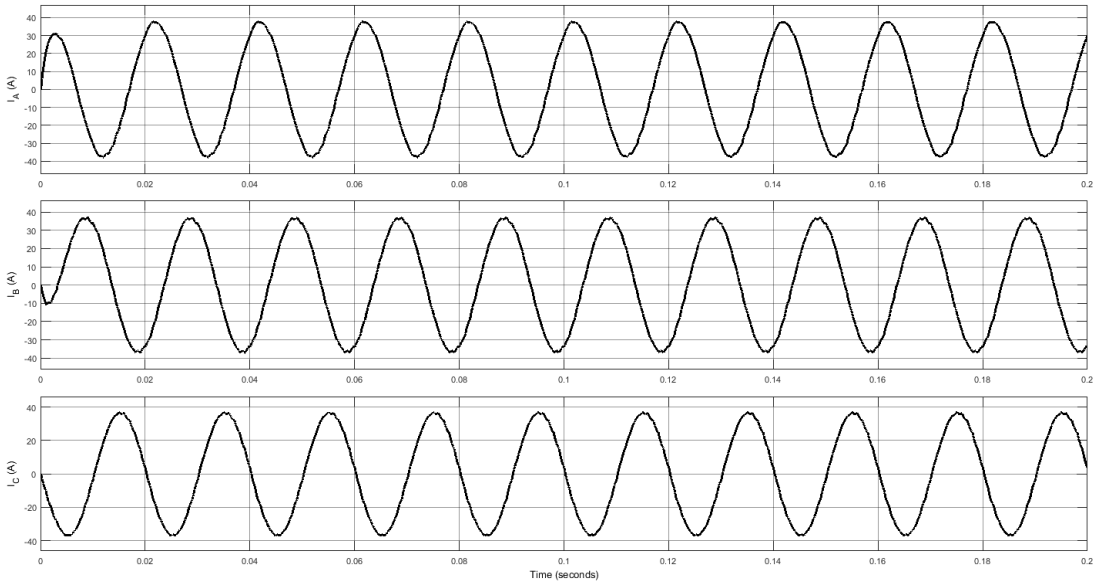

Figure 37: 9 Level Inverter Current Graphs in PWM

5.2 Square Wave Modulation

Voltage and current graphs of Generalized 9 level converter operated in 3 level Square Wave Modulation is shown in Figure 38 and 39 respectively.

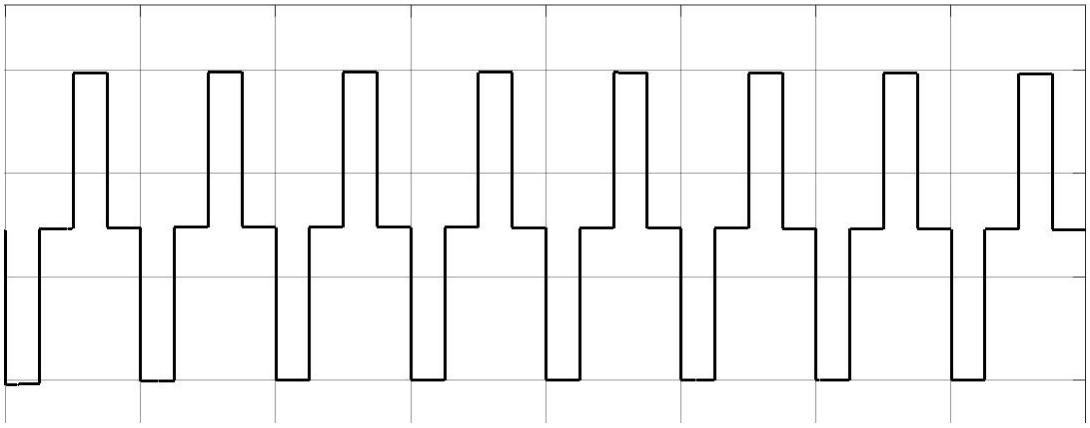

Figure 38: 3 Level Inverter Voltage Graphs in SWM

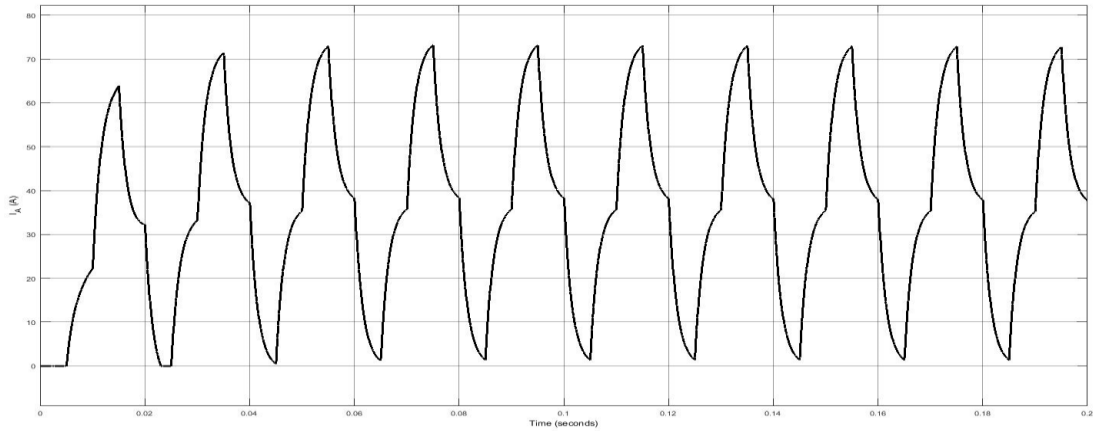

Figure 39: 3 Level Inverter Current Graphs of in SWM

Voltage and current graphs of Generalized 9 level converter operated in 5 level Square Wave Modulation is shown in Figure 40 and 41 respectively.

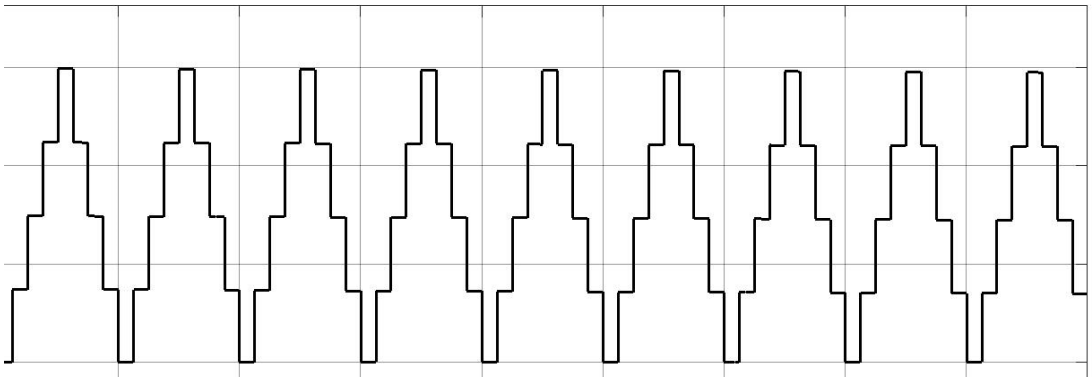

Figure 40: 5 Level Inverter Voltage Graphs of in SWM

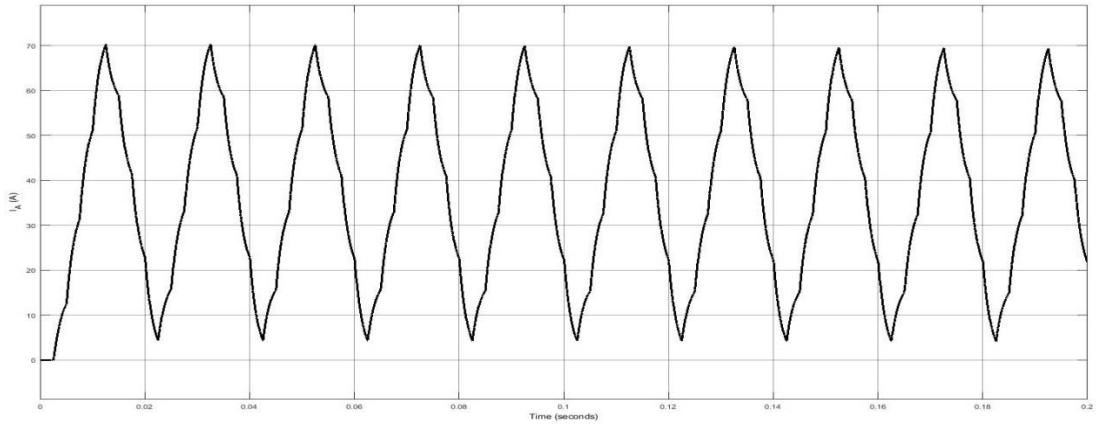

Figure 41: 5 Level Inverter Current Graphs of in SWM

Voltage and current graphs of Generalized 9 level converter operated in 7 level Square Wave Modulation is shown in Figure 42 and 43 respectively.

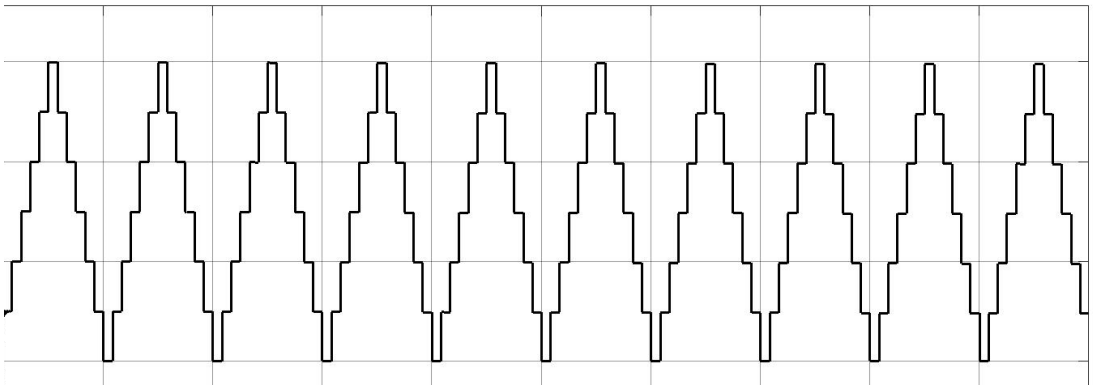

Figure 42: 7 Level Inverter Voltage Graphs of in SWM

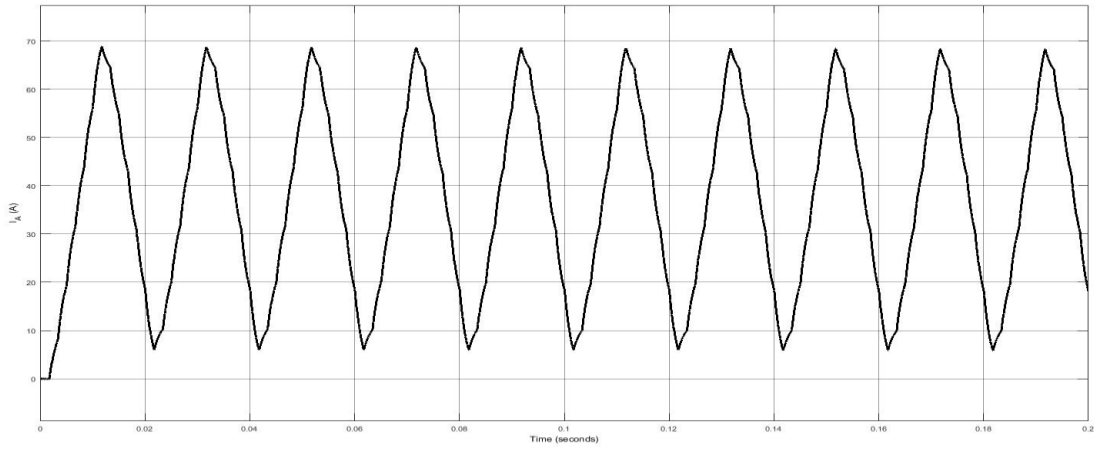

Figure 43: 7 Level Inverter Current Graphs of in SWM

Voltage and current graphs of Generalized 9 level converter operated in 9 level Square Wave Modulation is shown in Figure 44 and 45 respectively.

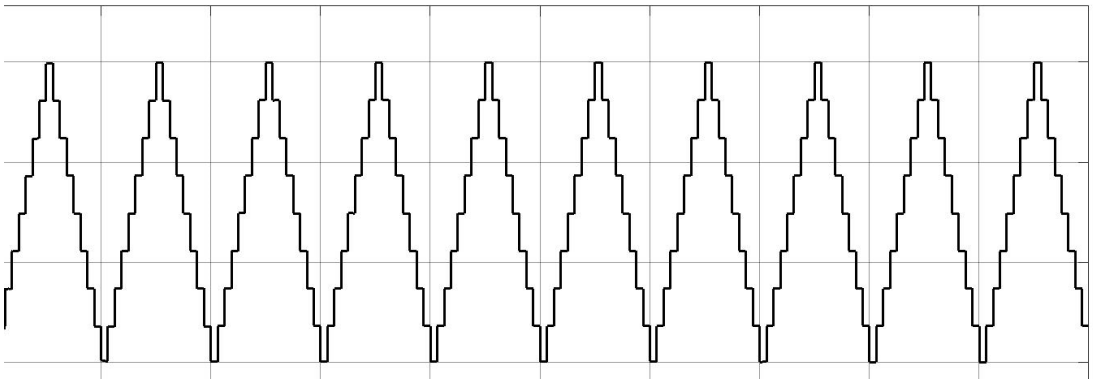

Figure 44: 9 Level Inverter Voltage Graphs of in SWM

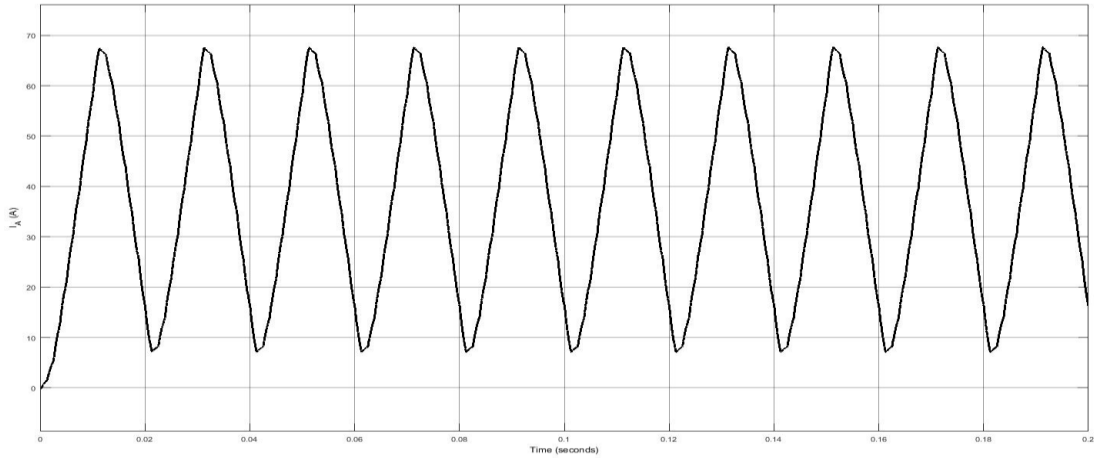

Figure 45: 9 Level Inverter Current Graphs of in SWM

5.3 Comparison of Total Harmonic Distortion of Pulse Width Modulation and Square Wave Modulation

Table 1 shows the Total Harmonic Distortion of Pulse Width Modulation and Square Wave Modulation of voltage and current in 3, 5, 7, and 9 levels of operation.

Table 1: THD of PWM and SWM

THD%	Levels	PWM	Square Wave	PWM	Square Wave	PWM	Square Wave
		FC		NPC		CHB	
Voltage	3	32.24	48.13	32.3	48.14	32.26	48.14
	5	16.85	28.86	16.92	29.01	16.88	28.96
	7	14.19	21.66	14.21	21.74	14.19	21.72
	9	10.74	17.87	10.74	18.18	10.73	17.47
Current	3	4.72	23.37	4.71	23.37	4.71	23.37
	5	2.29	10.98	2.29	11.09	2.27	11.06
	7	1.72	8.78	1.72	8.83	1.70	8.82
	9	1.59	7.79	1.59	7.97	1.58	7.53

5.4 Analysis of Output Waveforms of Pulse Width Modulation with Different Modulation Depths

Voltage and current graphs of Generalized 3 Level Inverter operated in 25% modulation depth is shown in Figure 46 and 47 respectively.

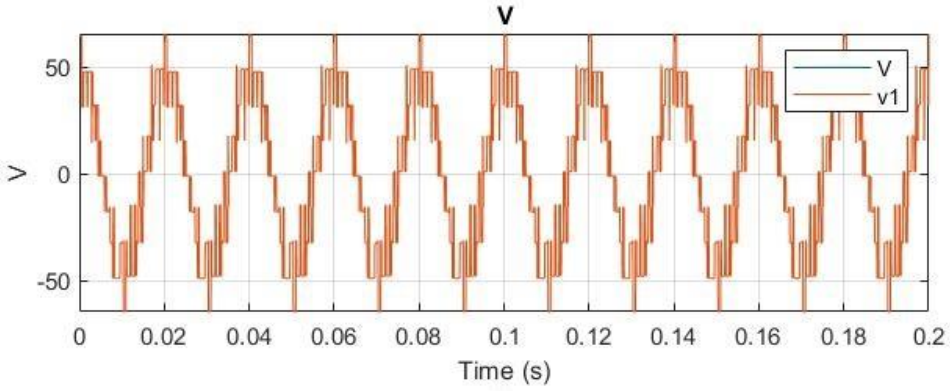

Figure 46: 3 Level Inverter Voltage Graph at 25% Modulation Depth in PWM

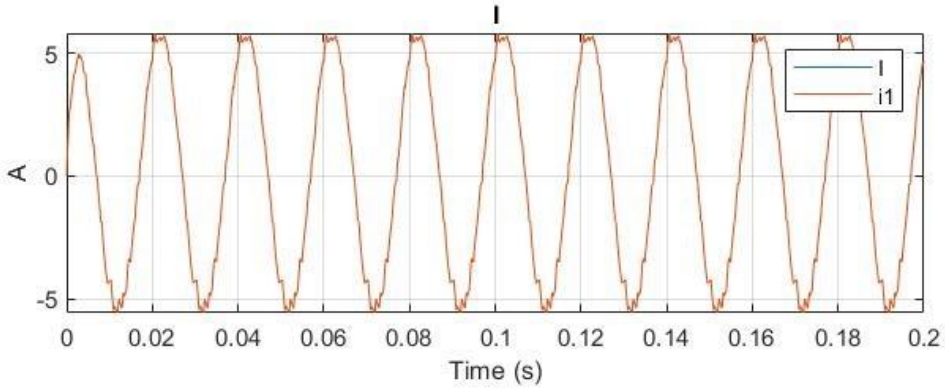

Figure 47: 3 Level Inverter Current Graph at 25% Modulation Depth in PWM

Voltage and current graphs of Generalized 3 level converter operated in 50% modulation depth is shown in Figure 48 and 49 respectively.

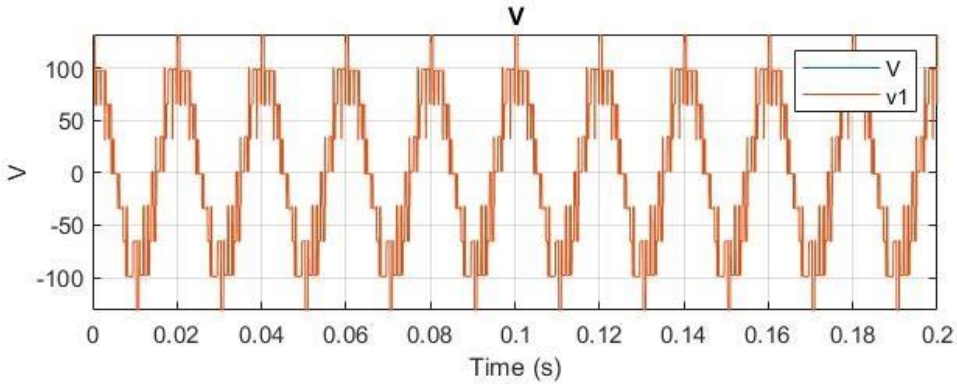

Figure 48: 3 Level Inverter Voltage Graph at 50% Modulation Depth in PWM

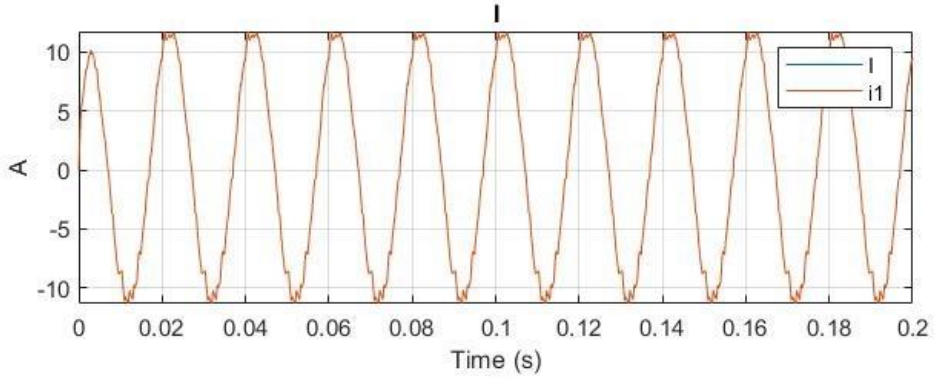

Figure 49: 3 Level Inverter Current Graph at 50% Modulation Depth in PWM

Voltage and current graphs of Generalized 3 level converter operated in 75% modulation depth is shown in Figure 50 and 51 respectively.

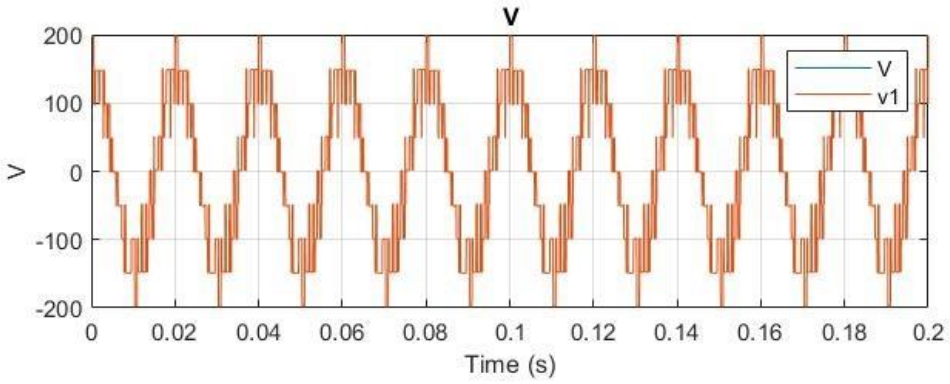

Figure 50: 3 Level Inverter Voltage Graph at 75% Modulation Depth in PWM

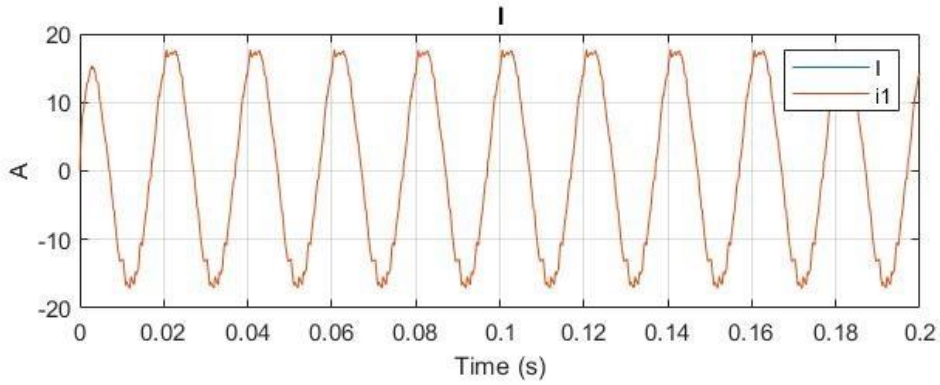

Figure 51: 3 Level Inverter Current Graph at 75% Modulation Depth in PWM

Voltage and current graphs of Generalized 3 level converter operated in 100% modulation depth is shown in Figure 52 and 53 respectively.

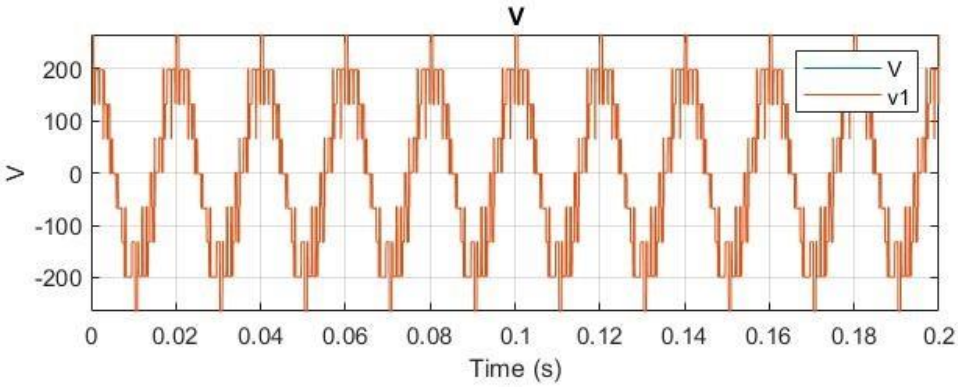

Figure 52: 3 Level Inverter Voltage Graph at 100% Modulation Depth in PWM

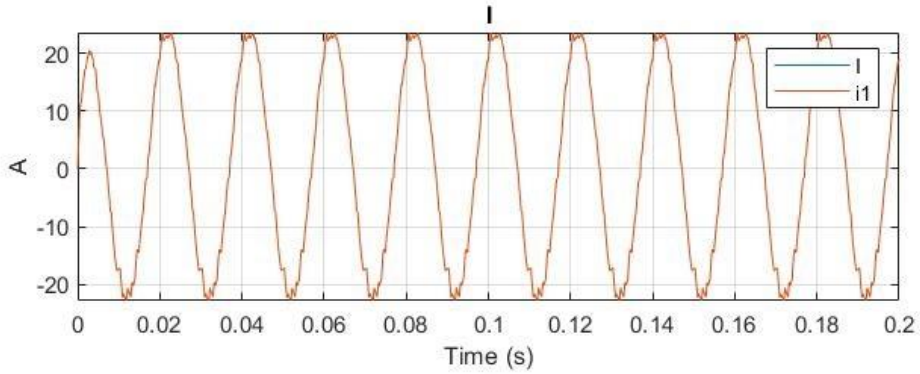

Figure 53: 3 Level Inverter Current Graph at 100% Modulation Depth in PWM

Voltage and current graphs of Generalized 5 level converter operated in 25% modulation depth is shown in Figure 54 and 55 respectively.

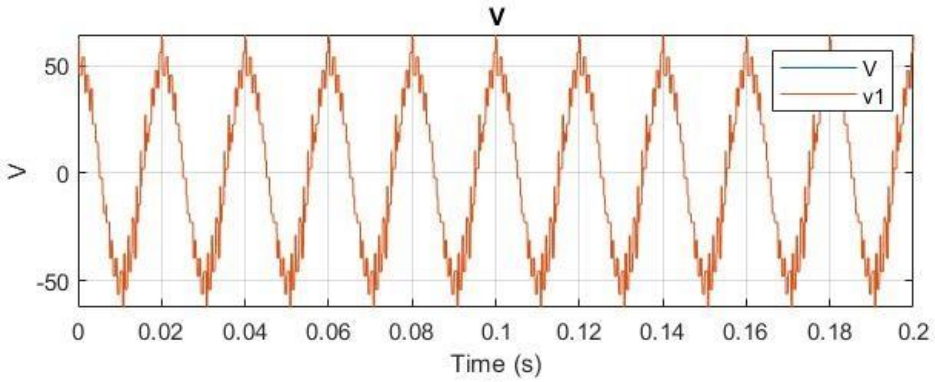

Figure 54: 5 Level Inverter Voltage Graph at 25% Modulation Depth in PWM

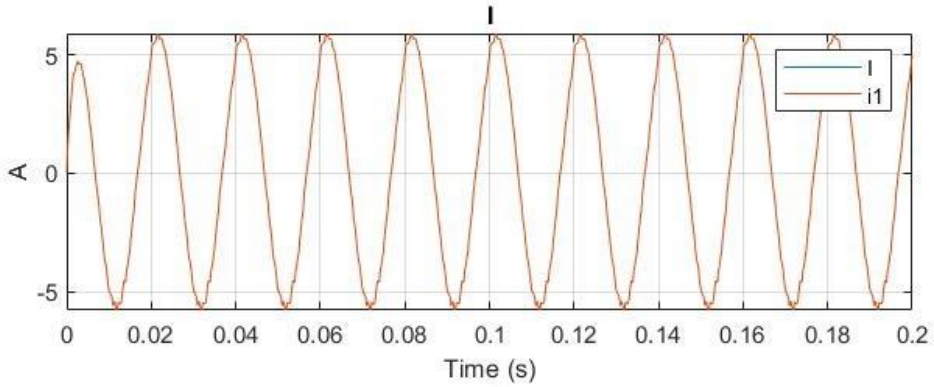

Figure 55: 5 Level Inverter Current Graph at 25% Modulation Depth in PWM

Voltage and current graphs of Generalized 5 level converter operated in 50% modulation depth is shown in Figure 56 and 57 respectively.

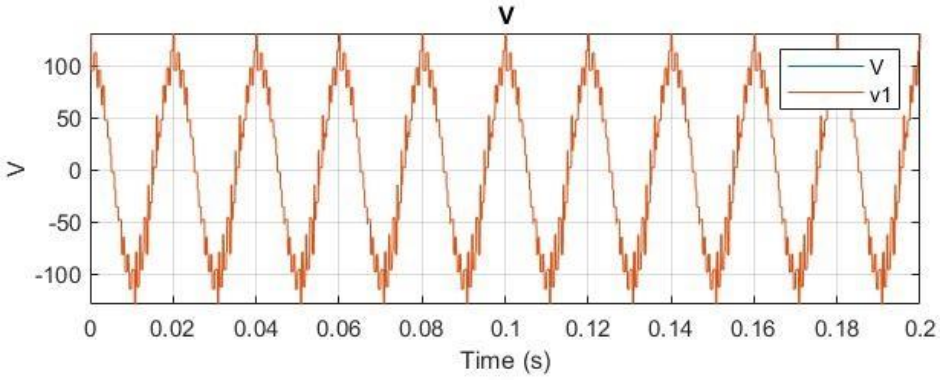

Figure 56: 5 Level Inverter Voltage Graph at 50% Modulation Depth in PWM

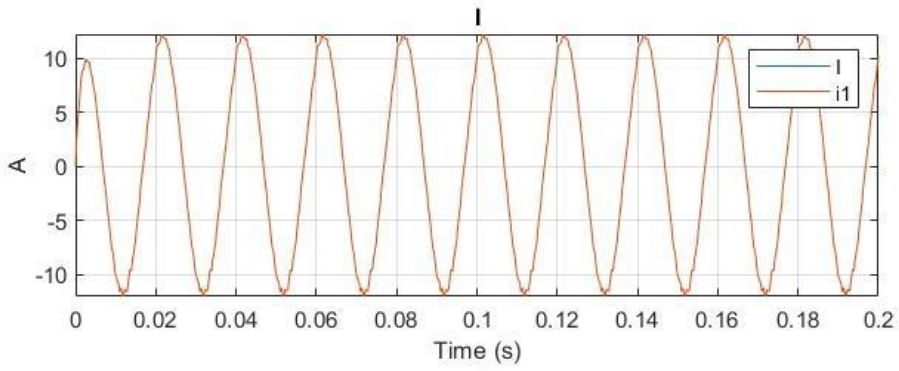

Figure 57: 5 Level Inverter Current Graph at 50% Modulation Depth in PWM

Voltage and current graphs of Generalized 5 level converter operated in 75% modulation depth is shown in Figure 58 and 59 respectively.

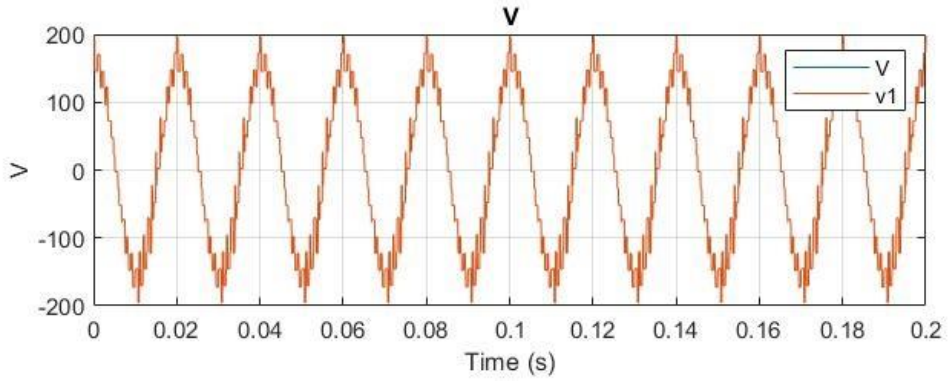

Figure 58: 5 Level Inverter Voltage Graph at 75% Modulation Depth in PWM

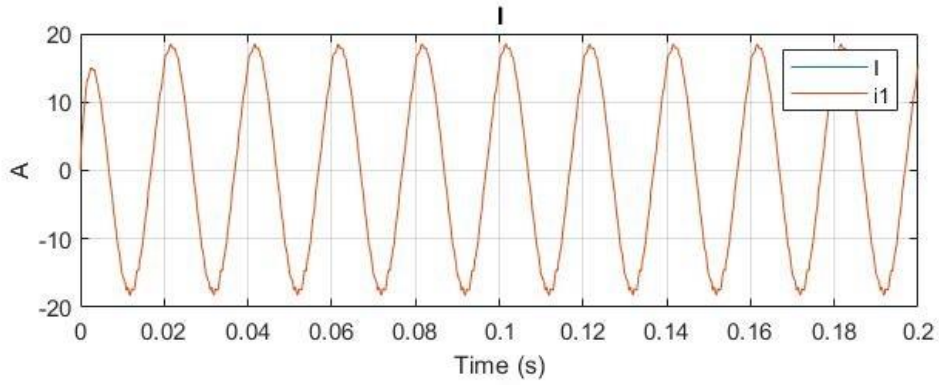

Figure 59: 5 Level Inverter Current Graph at 75% Modulation Depth in PWM

Voltage and current graphs of Generalized 5 level converter operated in 100% modulation depth is shown in Figure 60 and 61 respectively.

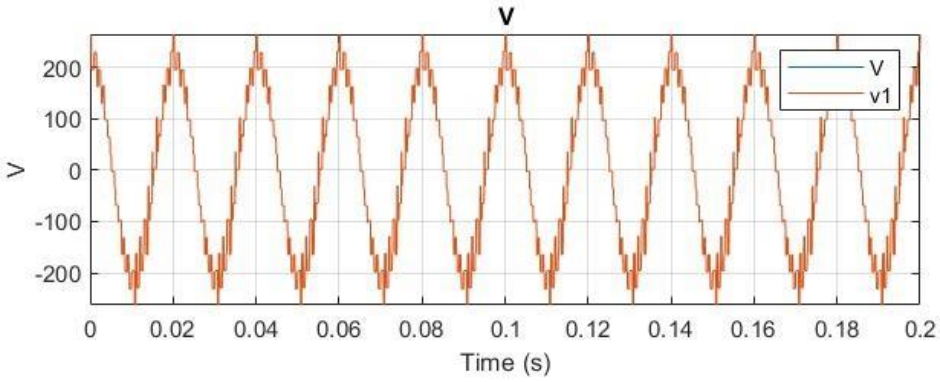

Figure 60: 5 Level Inverter Voltage Graph at 100% Modulation Depth in PWM

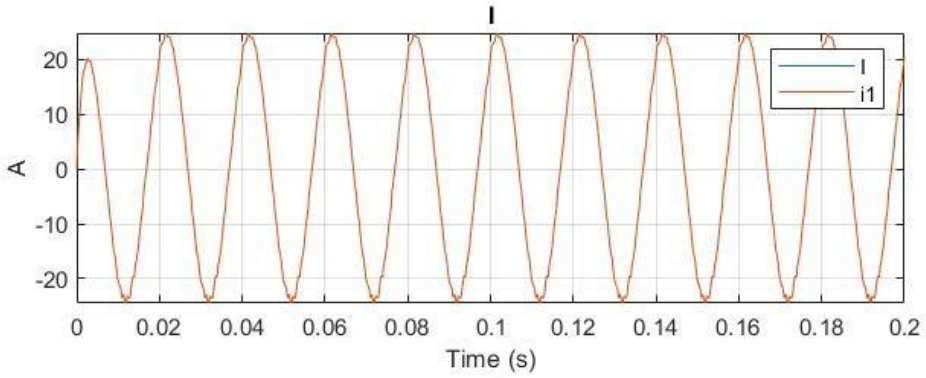

Figure 61: 5 Level Inverter Current Graph at 100% Modulation Depth in PWM

Voltage and current graphs of Generalized 7 level converter operated in 25% modulation depth is shown in Figure 62 and 63 respectively.

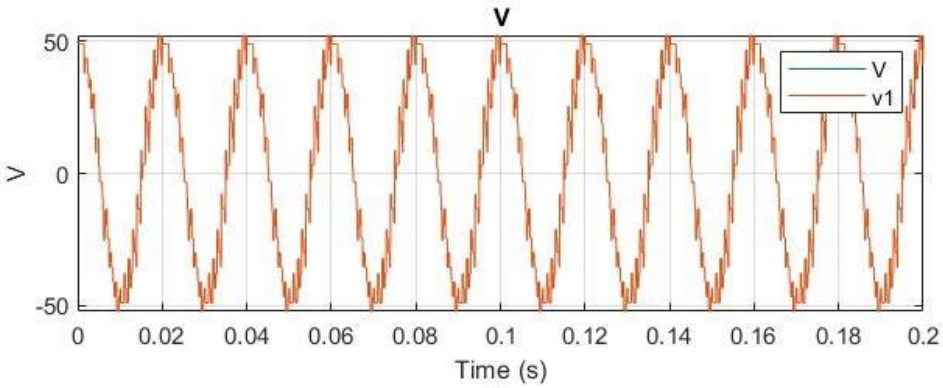

Figure 62: 7 Level Inverter Voltage Graph at 25% Modulation Depth in PWM

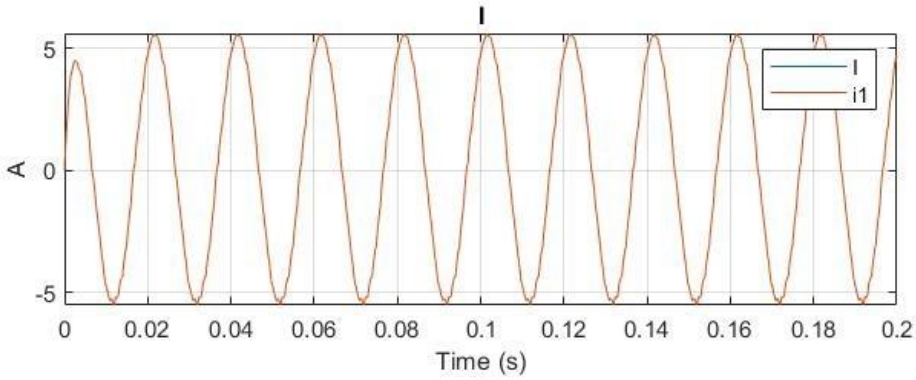

Figure 63: 7 Level Inverter Current Graph at 25% Modulation Depth in PWM

Voltage and current graphs of Generalized 7 level converter operated in 50% modulation depth is shown in Figure 64 and 65 respectively.

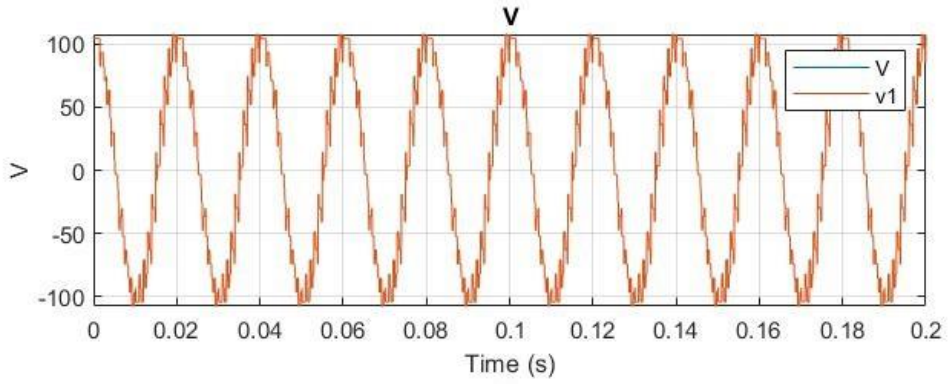

Figure 64: 7 Level Inverter Voltage Graph at 50% Modulation Depth in PWM

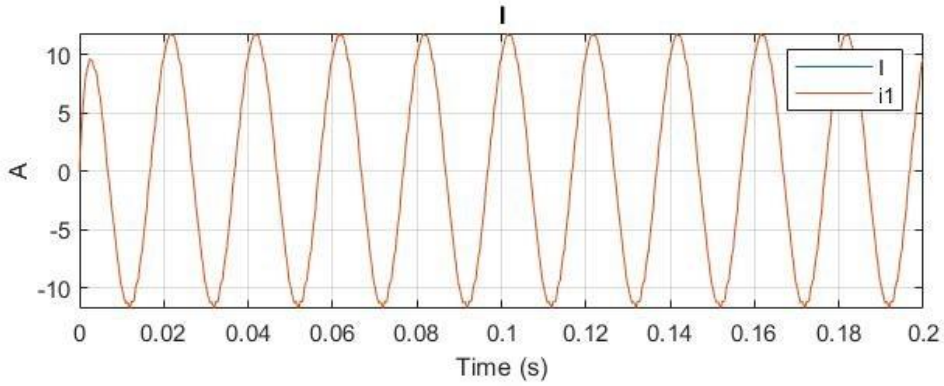

Figure 65: 7 Level Inverter Current Graph at 50% Modulation Depth in PWM

Voltage and current graphs of Generalized 7 level converter operated in 75% modulation depth is shown in Figure 66 and 67 respectively.

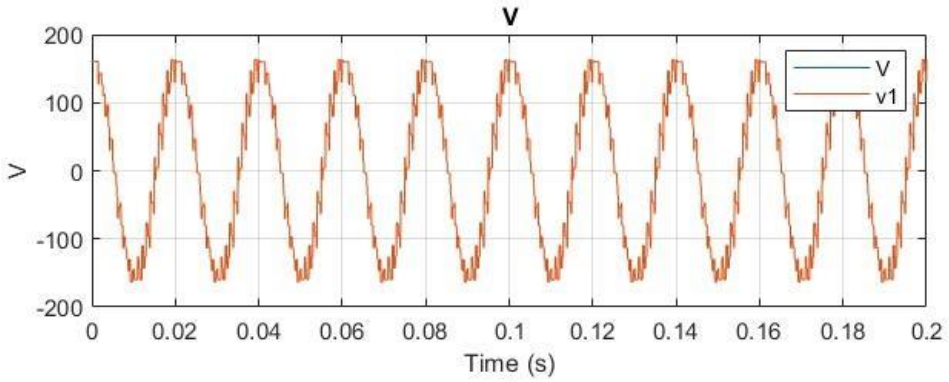

Figure 66: 7 Level Inverter Voltage Graph at 75% Modulation Depth in PWM

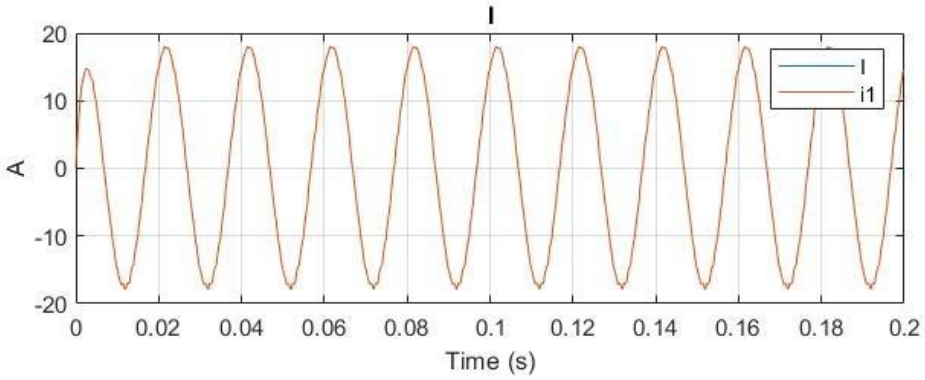

Figure 67: 7 Level Inverter Current Graph at 75% Modulation Depth in PWM

Voltage and current graphs of Generalized 7 level converter operated in 100% modulation depth is shown in Figure 68 and 69 respectively.

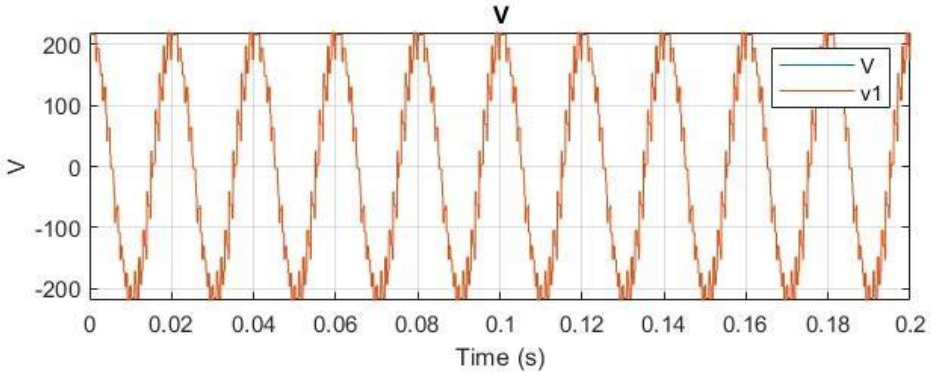

Figure 68: 7 Level Inverter Voltage Graph at 100% Modulation Depth in PWM

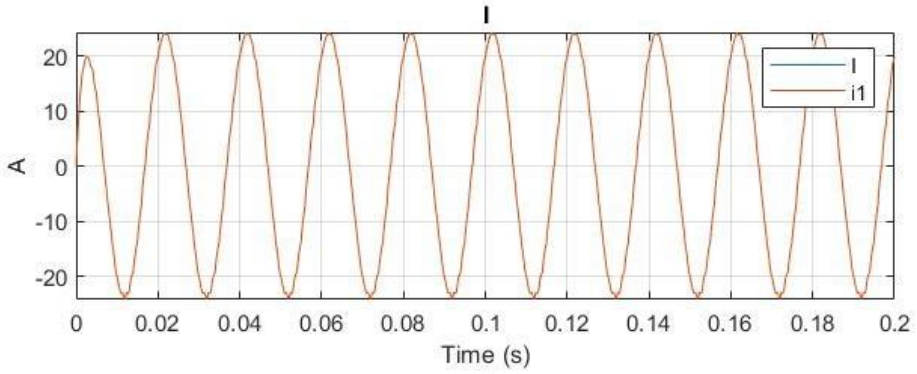

Figure 69: 7 Level Inverter Current Graph at 100% Modulation Depth in PWM

Voltage and current graphs of Generalized 9 level converter operated in 25% modulation depth is shown in Figure 70 and 71 respectively.

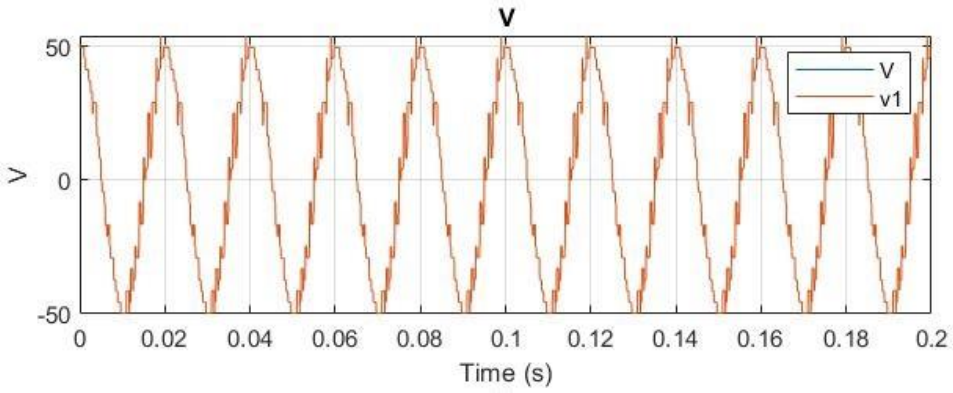

Figure 70: 9 Level Inverter Voltage Graph at 25% Modulation Depth in PWM

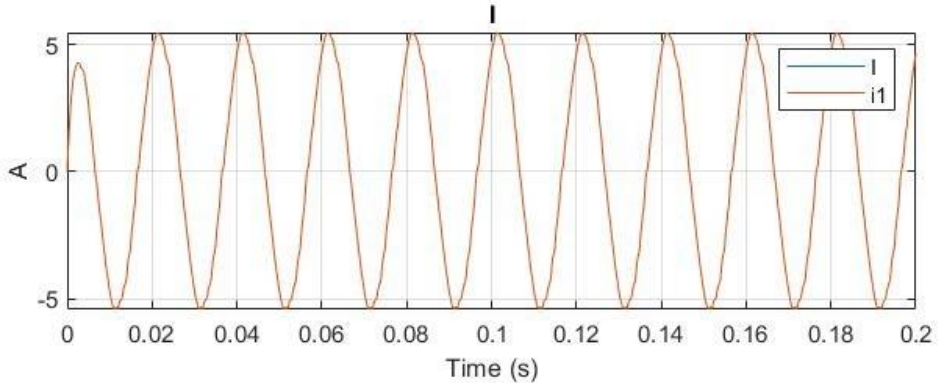

Figure 71: 9 Level Inverter Current Graph at 25% Modulation Depth in PWM

Voltage and current graphs of Generalized 9 level converter operated in 50% modulation depth is shown in Figure 72 and 73 respectively.

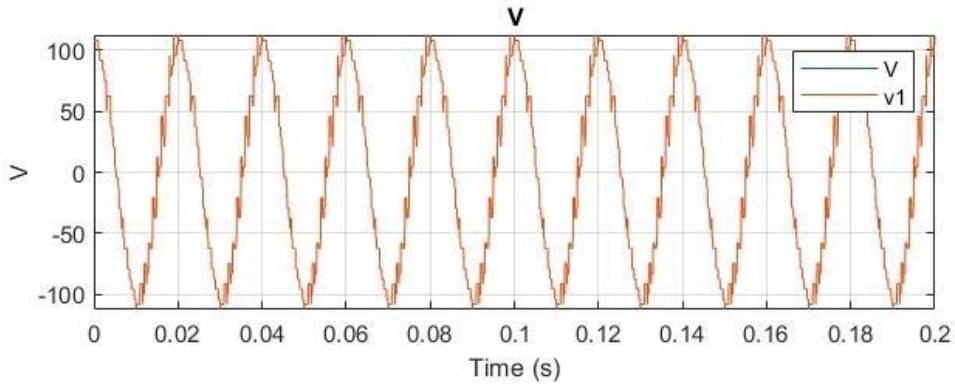

Figure 72: 9 Level Inverter Voltage Graph at 50% Modulation Depth in PWM

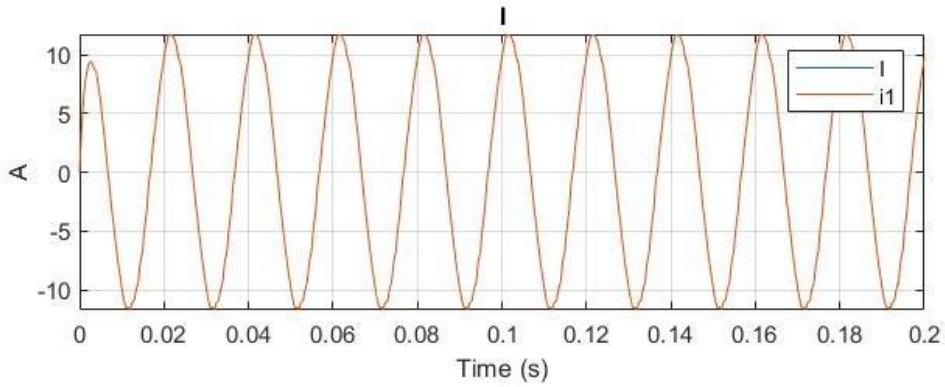

Figure 73: 9 Level Inverter Current Graph at 50% Modulation Depth in PWM

Voltage and current graphs of Generalized 9 level converter operated in 75% modulation depth is shown in Figure 74 and 75 respectively.

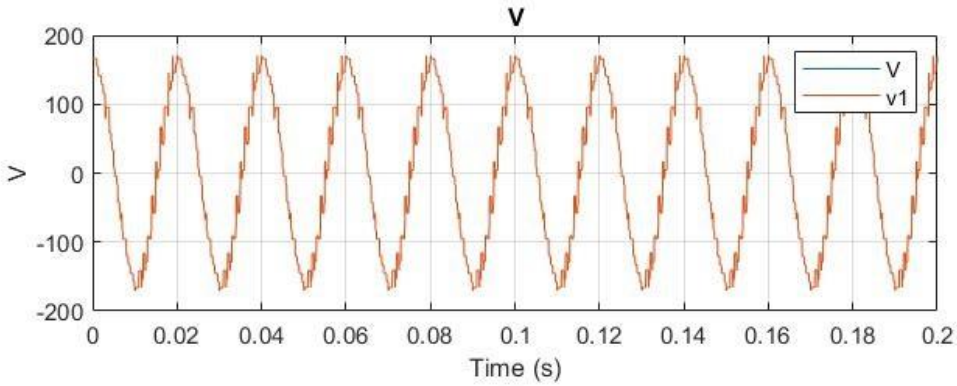

Figure 74: 9 Level Inverter Voltage Graph at 75% Modulation Depth in PWM

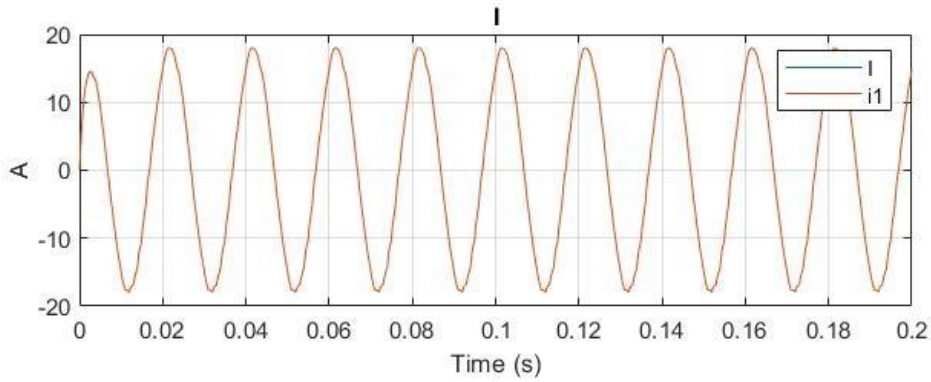

Figure 75: 9 Level Inverter Current Graph at 75% Modulation Depth in PWM

Voltage and current graphs of Generalized 9 level converter operated in 100% modulation depth is shown in Figure 76 and 77 respectively.

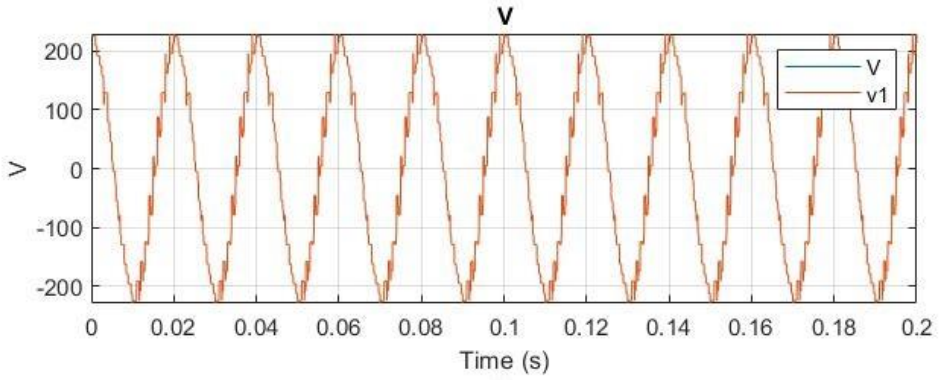

Figure 76: 9 Level Inverter Voltage Graph at 100% Modulation Depth in PWM

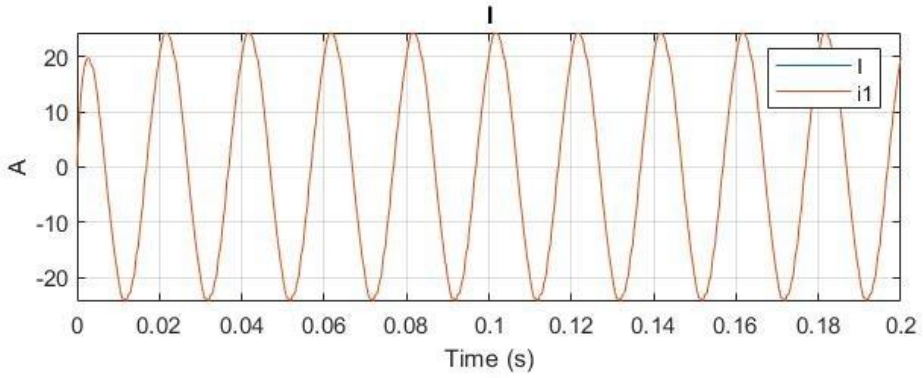

Figure 77: 9 Level Inverter Current Graph at 100% Modulation Depth in PWM

5.5 Analysis of Output Waveforms of Square Wave Modulation with Different Modulation Depths

Voltage and current graphs of Generalized 3 Level Inverter operated in 25% modulation depth is shown in Figure 78 and 79 respectively.

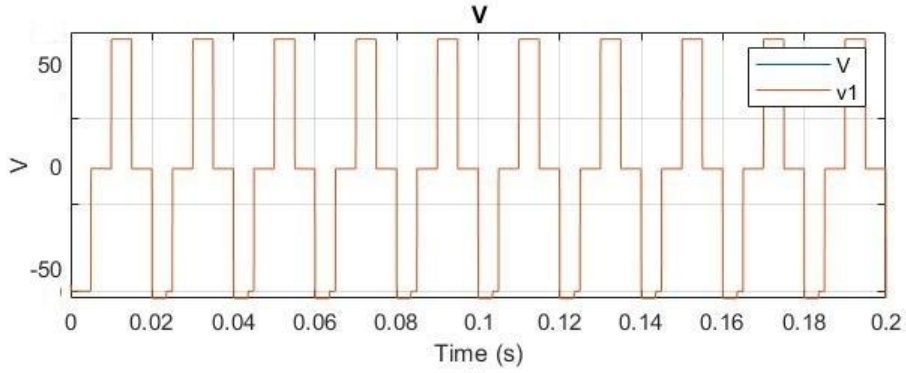

Figure 78: 3 Level Inverter Voltage Graph at 25% Modulation Depth in SWM

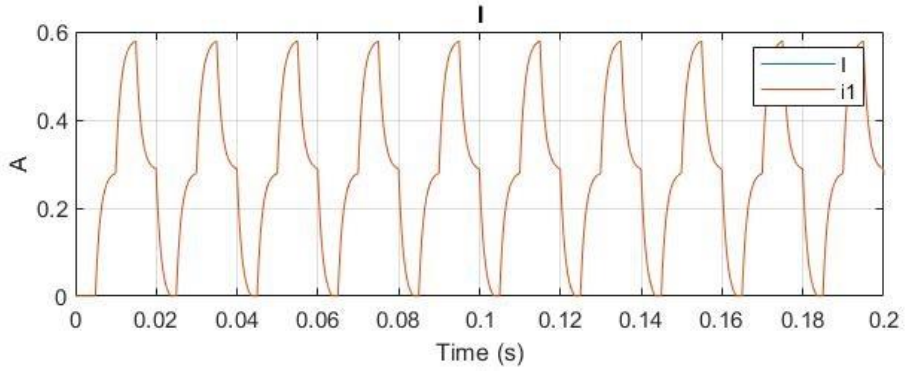

Figure 79: 3 Level Inverter Current Graph at 25% Modulation Depth in SWM

Voltage and current graphs of Generalized 3 level converter operated in 50% modulation depth is shown in Figure 80 and 81 respectively.

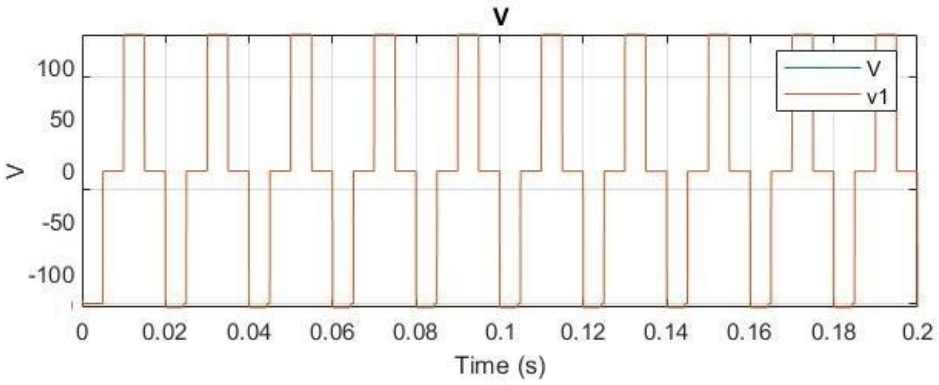

Figure 80: 3 Level Inverter Voltage Graph at 50% Modulation Depth in SWM

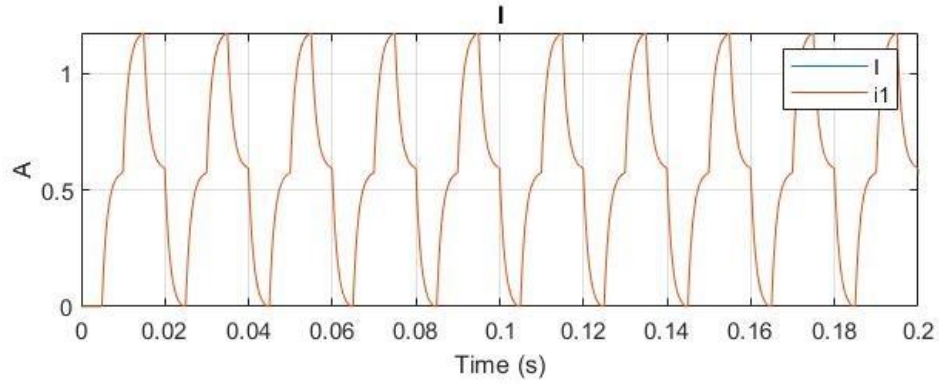

Figure 81: 3 Level Inverter Current Graph at 50% Modulation Depth in SWM

Voltage and current graphs of Generalized 3 level converter operated in 75% modulation depth is shown in Figure 74 and 75 respectively.

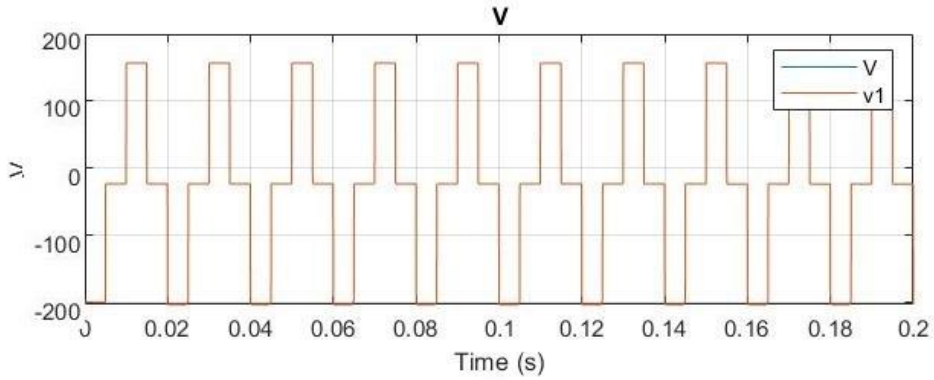

Figure 82: 3 Level Inverter Voltage Graph at 75% Modulation Depth in SWM

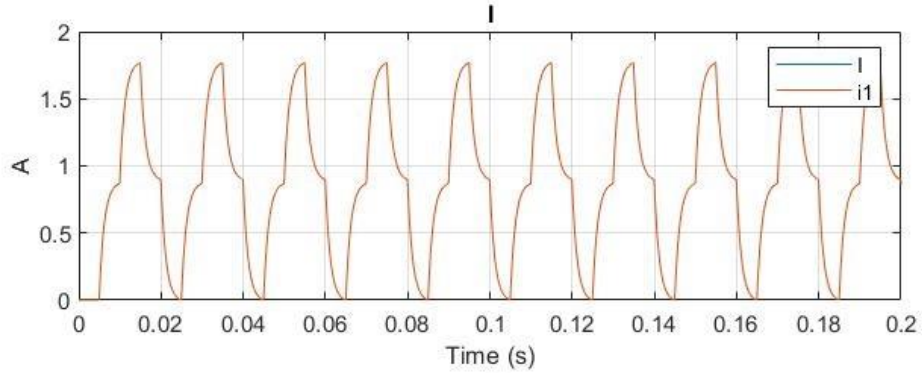

Figure 83: 3 Level Inverter Current Graph at 75% Modulation Depth in SWM

Voltage and current graphs of Generalized 3 level converter operated in 100% modulation depth is shown in Figure 84 and 85 respectively.

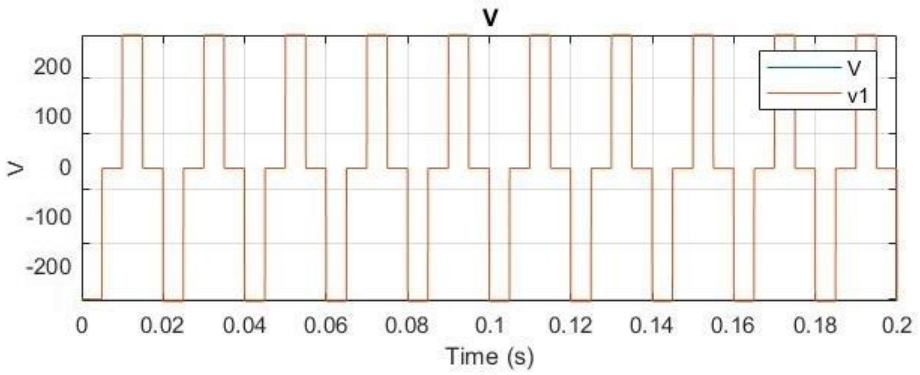

Figure 84: 3 Level Inverter Voltage Graph at 100% Modulation Depth in SWM

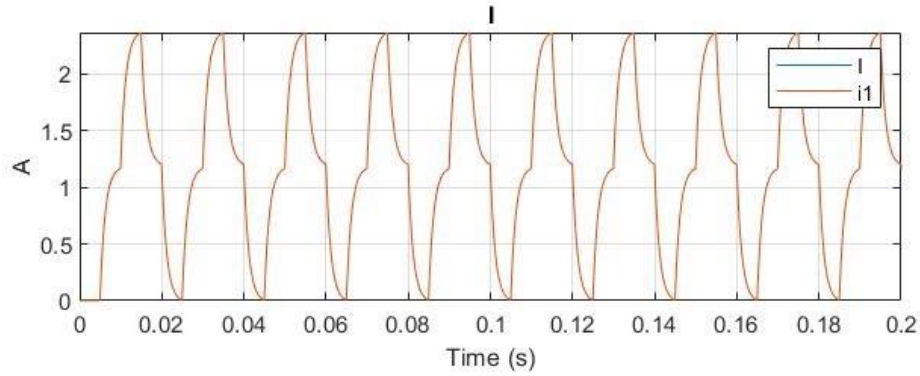

Figure 85: 3 Level Inverter Current Graph at 100% Modulation Depth in SWM

Voltage and current graphs of Generalized 5 level converter operated in 25% modulation depth is shown in Figure 86 and 87 respectively.

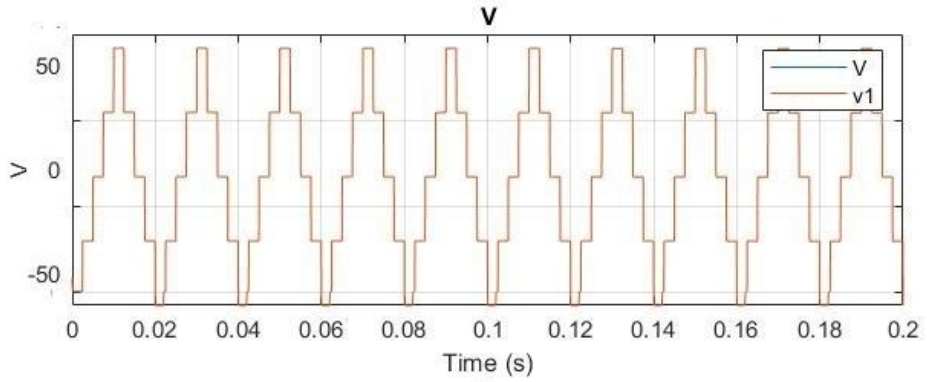

Figure 86: 5 Level Inverter Voltage Graph at 25% Modulation Depth in SWM

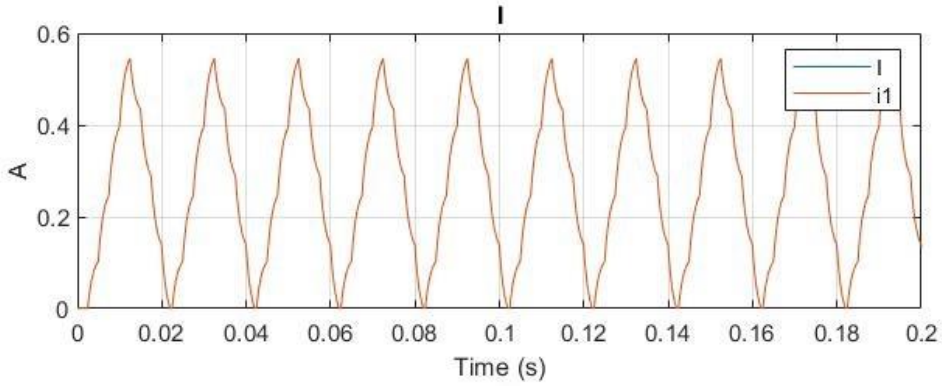

Figure 87: 5 Level Inverter Current Graph at 25% Modulation Depth in SWM

Voltage and current graphs of Generalized 5 level converter operated in 50% modulation depth is shown in Figure 88 and 89 respectively.

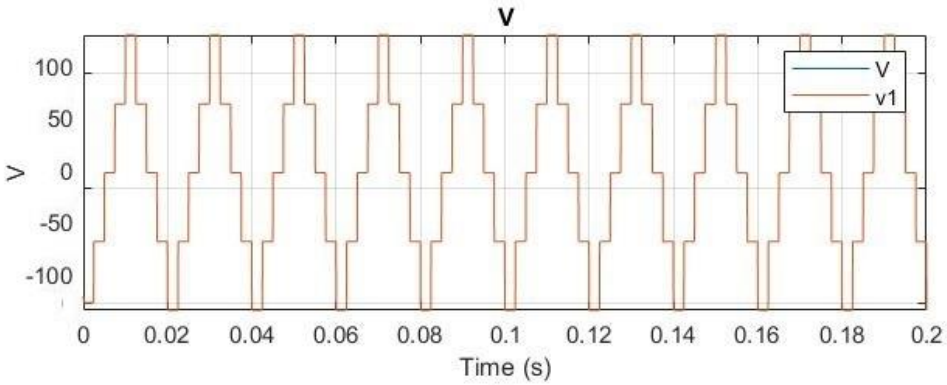

Figure 88: 5 Level Inverter Voltage Graph at 50% Modulation Depth in SWM

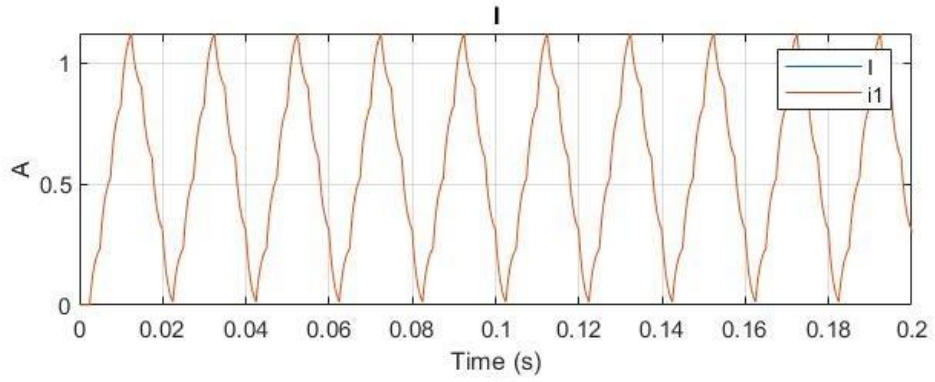

Figure 89: 5 Level Inverter Current Graph at 50% Modulation Depth in SWM

Voltage and current graphs of Generalized 5 level converter operated in 75% modulation depth is shown in Figure 90 and 91 respectively.

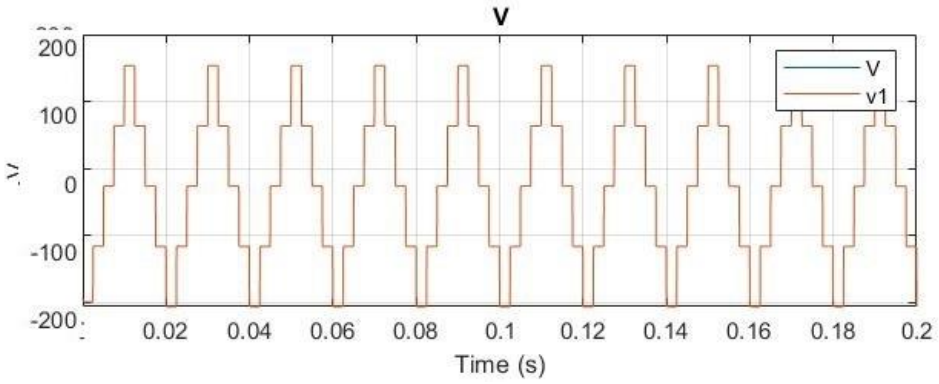

Figure 90: 5 Level Inverter Voltage Graph at 75% Modulation Depth in SWM

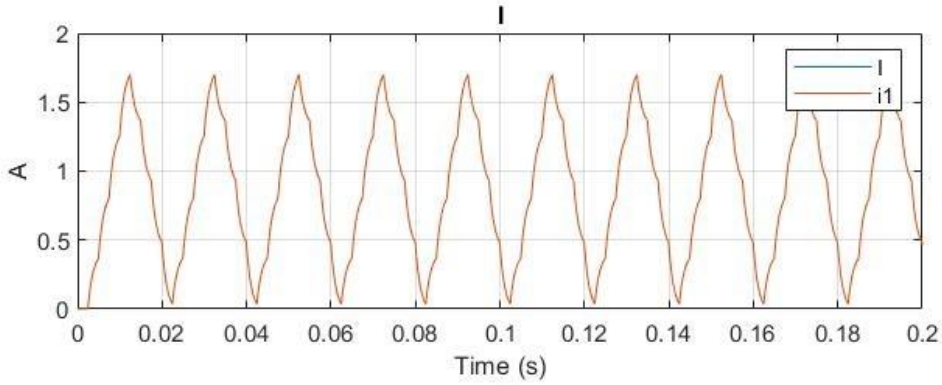

Figure 91: 5 Level Inverter Current Graph at 75% Modulation Depth in SWM

Voltage and current graphs of Generalized 5 level converter operated in 100% modulation depth is shown in Figure 92 and 93 respectively.

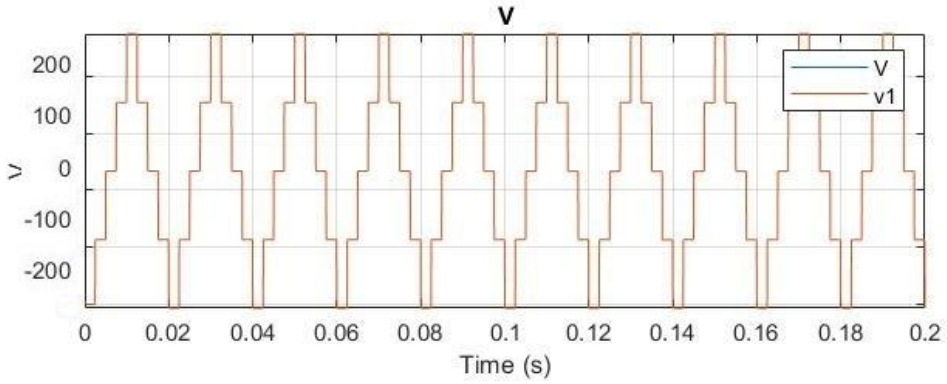

Figure 92: 5 Level Inverter Voltage Graph at 100% Modulation Depth in SWM

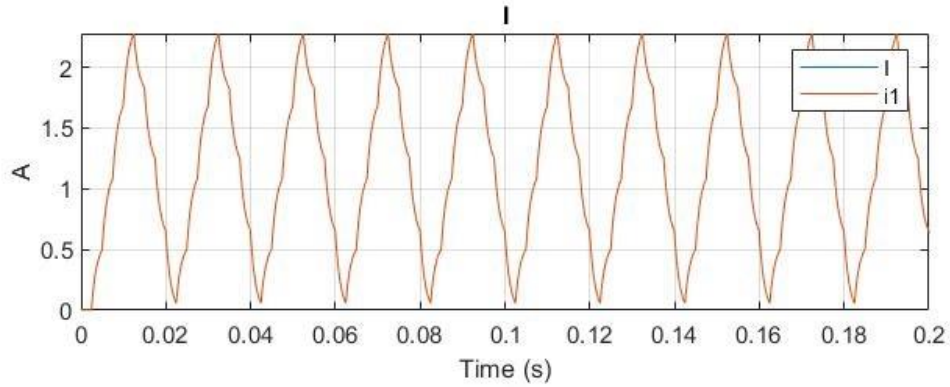

Figure 93: 5 Level Inverter Current Graph at 100% Modulation Depth in SWM

Voltage and current graphs of Generalized 7 level converter operated in 25% modulation depth is shown in Figure 94 and 95 respectively.

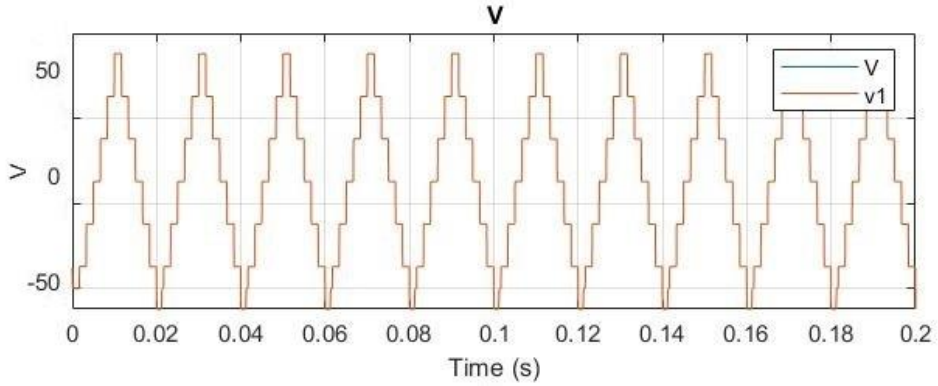

Figure 94: 7 Level Inverter Voltage Graph at 25% Modulation Depth in SWM

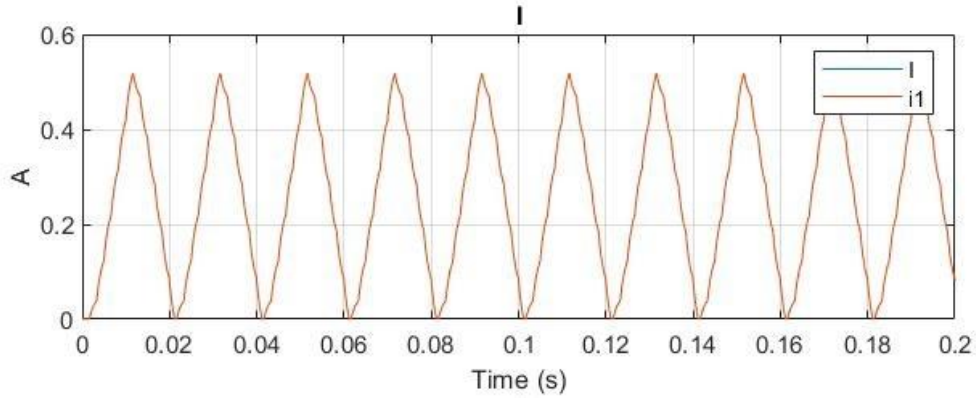

Figure 95: 7 Level Inverter Current Graph at 25% Modulation Depth in SWM

Voltage and current graphs of Generalized 7 level converter operated in 50% modulation depth is shown in Figure 96 and 97 respectively.

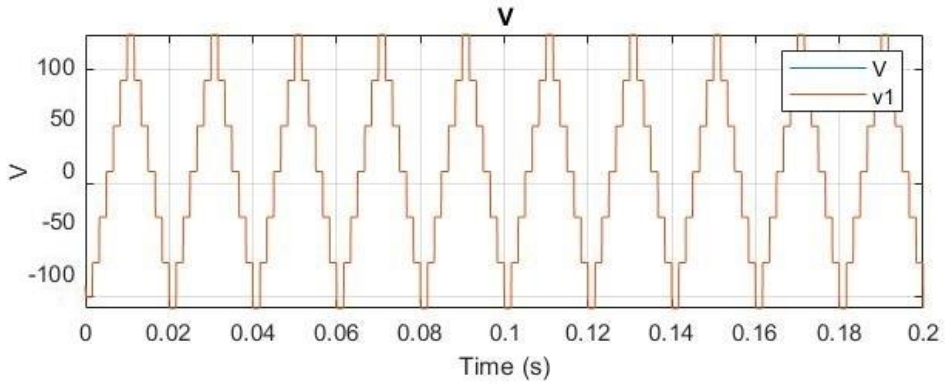

Figure 96: 7 Level Inverter Voltage Graph at 50% Modulation Depth in SWM

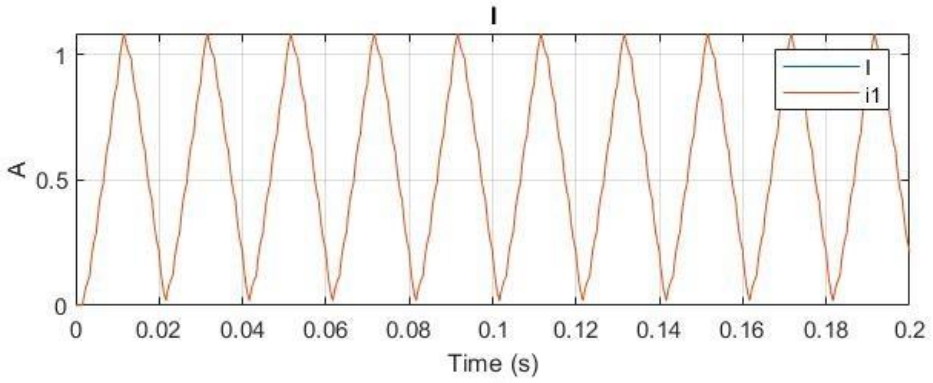

Figure 97: 7 Level Inverter Current Graph at 50% Modulation Depth in SWM

Voltage and current graphs of Generalized 7 level converter operated in 75% modulation depth is shown in Figure 98 and 99 respectively.

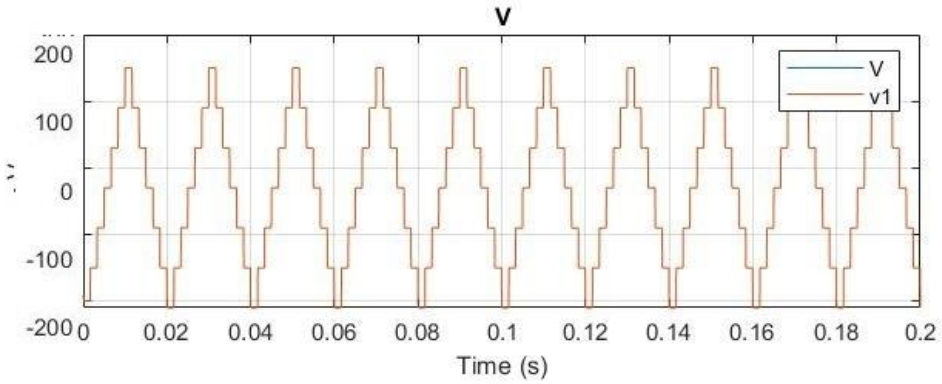

Figure 98: 7 Level Inverter Voltage Graph at 75% Modulation Depth in SWM

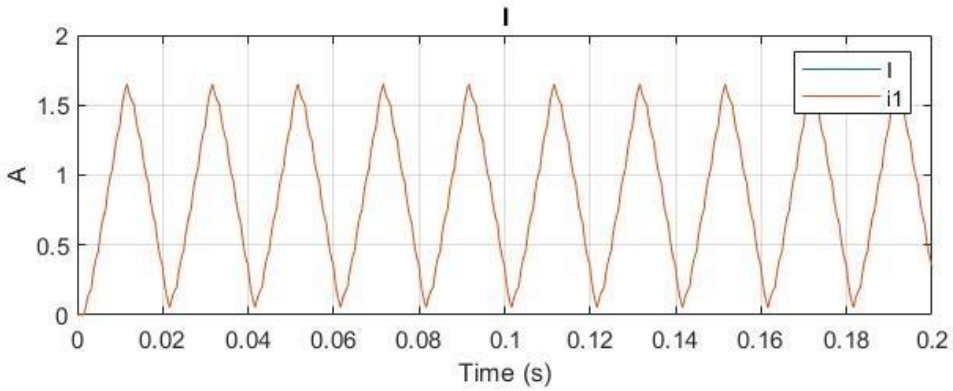

Figure 99: 7 Level Inverter Current Graph at 75% Modulation Depth in SWM

Voltage and current graphs of Generalized 7 level converter operated in 100% modulation depth is shown in Figure 100 and 101 respectively.

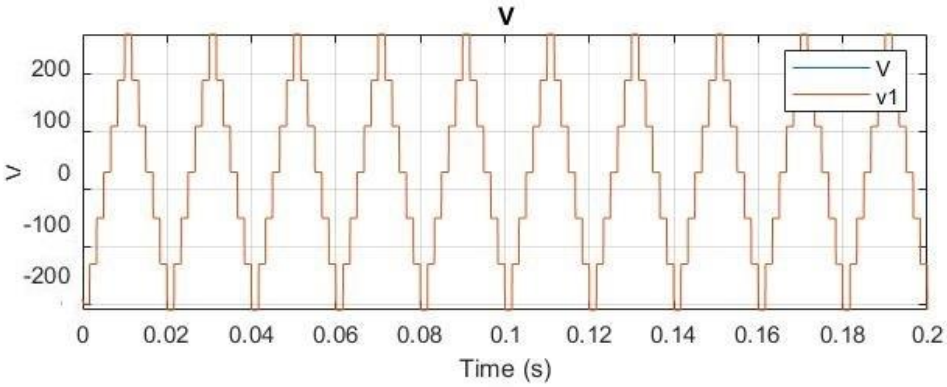

Figure 100: 7 Level Inverter Voltage Graph at 100% Modulation Depth in SWM

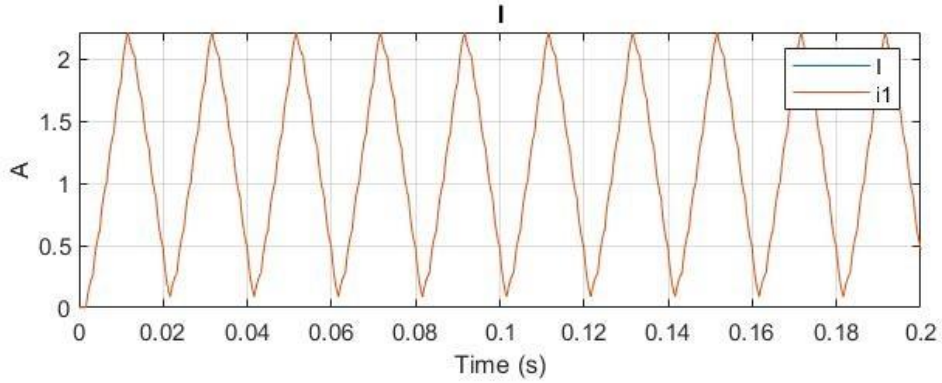

Figure 101 7 Level Inverter Current Graph at 100% Modulation Depth in SWM

Voltage and current graphs of Generalized 9 level converter operated in 25% modulation depth is shown in Figure 102 and 103 respectively.

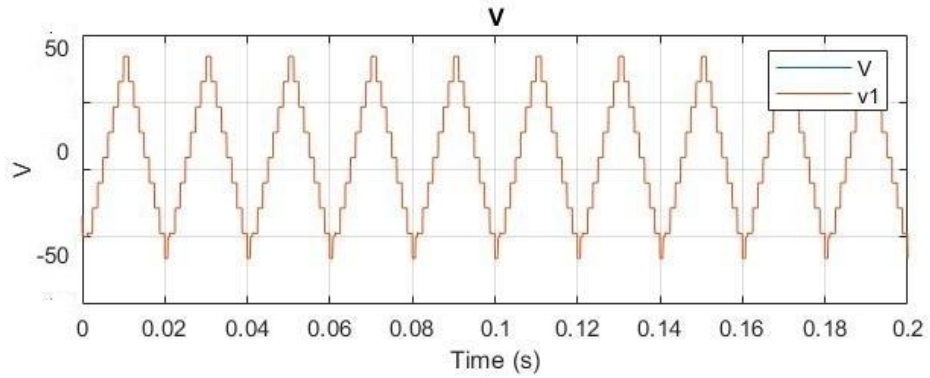

Figure 102: 9 Level Inverter Voltage Graph at 25% Modulation Depth in SWM

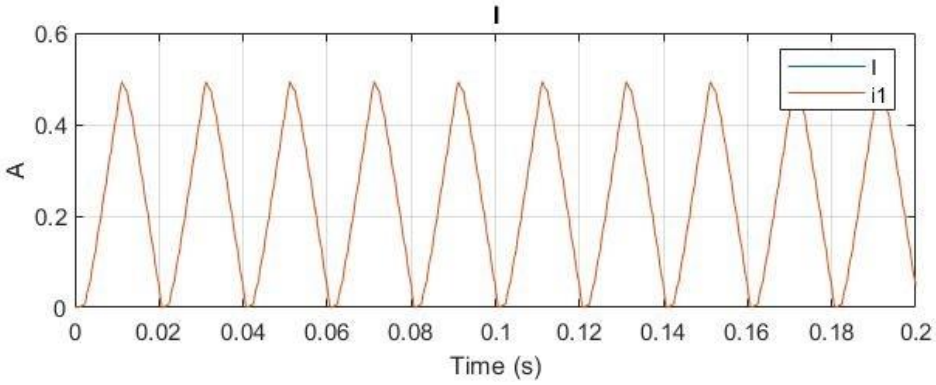

Figure 103: 9 Level Inverter Current Graph at 25% Modulation Depth in SWM

Voltage and current graphs of Generalized 9 level converter operated in 50% modulation depth is shown in Figure 104 and 105 respectively.

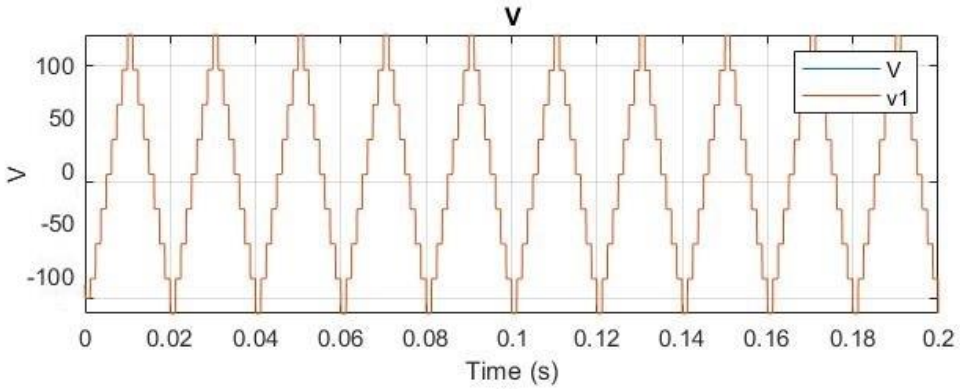

Figure 104: 9 Level Inverter Voltage Graph at 50% Modulation Depth in SWM

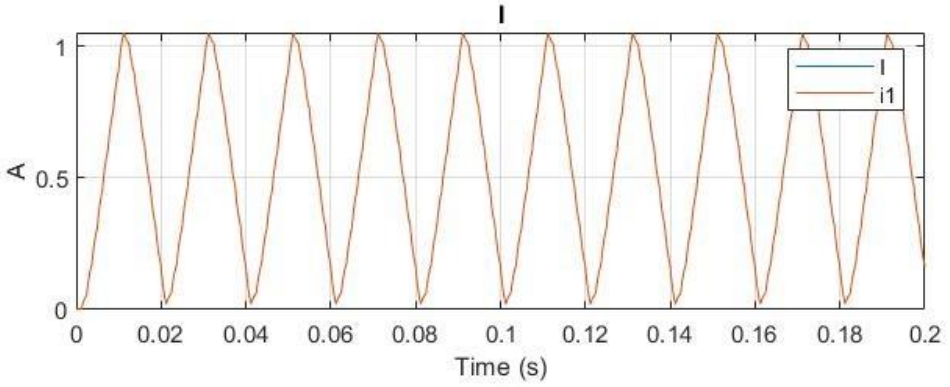

Figure 105: 9 Level Inverter Current Graph at 50% Modulation Depth in SWM

Voltage and current graphs of Generalized 9 level converter operated in 75% modulation depth is shown in Figure 106 and 107 respectively.

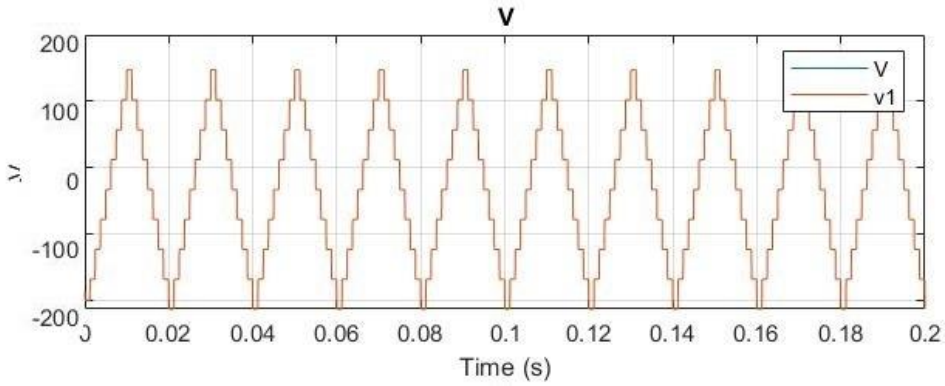

Figure 106: 9 Level Inverter Voltage Graph at 75% Modulation Depth in SWM

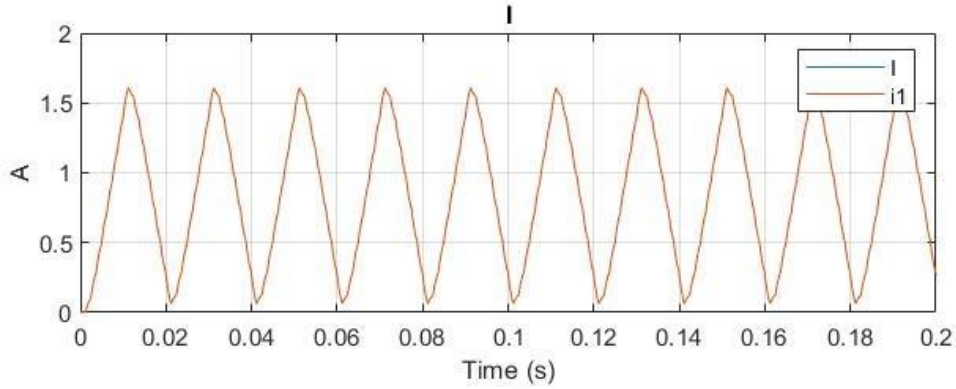

Figure 107: 9 Level Inverter Current Graph at 75% Modulation Depth in SWM

Voltage and current graphs of Generalized 9 level converter operated in 100% modulation depth is shown in Figure 108 and 109 respectively.

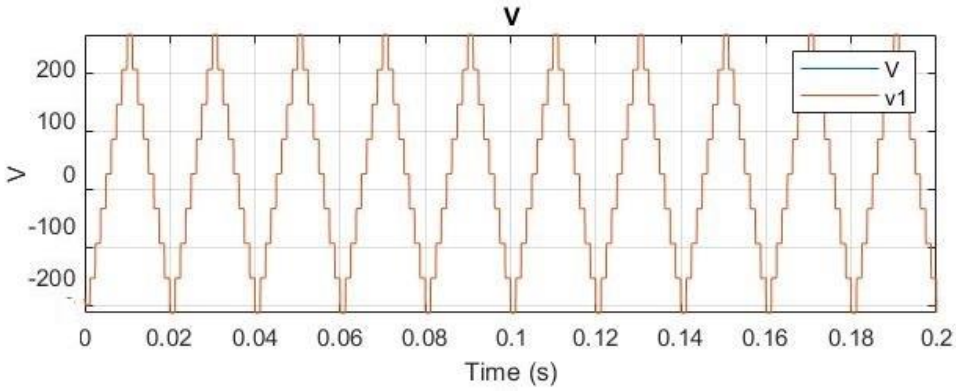

Figure 108: 9 Level Inverter Voltage Graph at 100% Modulation Depth in SWM

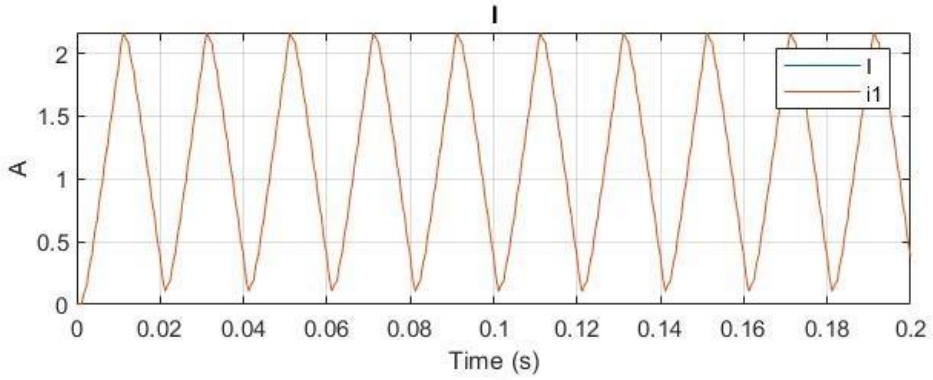

Figure 109: 9 Level Inverter Current Graph at 100% Modulation Depth in SWM

5.6 Total Harmonic Distortion and Efficiency of Pulse Width Modulation Operation

Table 2: THD and Efficiency of CHB, NPC and FC at 25% Mod. depth in PWM

Case 1: Depth of modulation 25% (Carrier frequency 1000 Hz)									
No. of Levels	CHB			NPC			FC		
	THD (%)		Efficiency (%)	THD (%)		Efficiency (%)	THD (%)		Efficiency (%)
	Voltage	Current		Voltage	Current		Voltage	Current	
3	33.2	4.75	94.9097	33.2	4.75	94.958	33.2	4.76	94.9479
5	18.49	2.72	91.4206	18.48	2.69	91.5539	18.47	2.69	91.5434
7	16.69	2.26	87.3119	16.64	2.24	87.5816	16.64	2.25	87.5711
9	13.83	2.63	83.329	13.76	2.57	83.757	13.77	2.57	83.7458

Table 3: THD and Efficiency of CHB, NPC and FC at 50% Mod. depth in PWM

Case 2: Depth of modulation 50% (Carrier frequency 1000 Hz)									
No. of Levels	CHB			NPC			FC		
	THD (%)		Efficiency (%)	THD (%)		Efficiency (%)	THD (%)		Efficiency (%)
	Voltage	Current		Voltage	Current		Voltage	Current	
3	32.69	4.72	97.0706	32.69	4.72	97.1051	32.69	4.72	97.095
5	17.62	2.45	95.5538	17.62	2.42	95.631	17.61	2.43	95.6208
7	15.24	1.78	93.4901	15.21	1.78	93.6416	15.21	1.78	93.6313
9	11.85	1.96	91.4435	11.8	1.9	91.685	11.8	1.9	91.6745

Table 4: THD and Efficiency of CHB, NPC and FC at 75% Mod. depth in PWM

Case 3: Depth of modulation 75% (Carrier frequency 1000 Hz)									
No. of Levels	CHB			NPC			FC		
	THD (%)		Efficiency (%)	THD (%)		Efficiency (%)	THD (%)		Efficiency (%)
	Voltage	Current		Voltage	Current		Voltage	Current	
3	32.54	4.71	97.7954	32.54	4.71	97.8252	32.53	4.71	97.8151
5	17.37	2.39	96.9459	17.36	2.35	97.0031	2.36	2.36	96.993
7	14.84	1.67	95.5811	14.82	1.66	95.6891	14.82	1.66	95.6789
9	11.34	1.81	94.2055	11.31	1.75	94.3758	11.32	1.75	94.3655

Table 5: THD and Efficiency of CHB, NPC and FC at 100% Mod. Depth in PWM

Case 4: Depth of modulation 100% (Carrier frequency 1000 Hz)									
No. of Levels	CHB			NPC			FC		
	THD (%)		Efficiency (%)	THD (%)		Efficiency (%)	THD (%)		Efficiency (%)
	Voltage	Current		Voltage	Current		Voltage	Current	
3	32.46	4.71	98.1588	32.46	4.71	98.1861	32.46	4.71	98.176
5	17.24	2.35	97.6447	17.24	2.33	97.6917	17.23	2.33	97.6816
7	14.67	1.62	96.6332	14.66	1.61	96.7187	14.66	1.61	96.7086
9	11.17	1.75	95.5977	11.12	1.69	95.7307	11.13	1.69	95.7206

5.7 Total Harmonic Distortion and Efficiency of square wave Operation

Table 6: THD and Efficiency of CHB, NPC and FC at 25% Mod. Depth in SWM

Case 1: Depth of modulation 25% (Carrier frequency 1000 Hz)									
No. of Levels	CHB			NPC			FC		
	THD (%)		Efficiency (%)	THD (%)		Efficiency (%)	THD (%)		Efficiency (%)
	Voltage	Current		Voltage	Current		Voltage	Current	
3	48.25	26.51	93.434	48.25	26.5	93.5085	48.25	26.51	93.437
5	28.74	12.35	91.1664	28.74	12.36	91.28	28.74	12.36	91.177
7	21.29	9.44	87.6379	21.29	9.45	87.7685	21.29	9.45	87.6594
9	18.5	9.1	83.9808	18.51	9.11	84.1252	18.51	9.11	84.0134

Table 7: THD and Efficiency of CHB, NPC and FC at 50% Mod. Depth in SWM

Case 2: Depth of modulation 50% (Carrier frequency 1000 Hz)									
No. of Levels	CHB			NPC			FC		
	THD (%)		Efficiency (%)	THD (%)		Efficiency (%)	THD (%)		Efficiency (%)
	Voltage	Current		Voltage	Current		Voltage	Current	
3	48.28	26.45	95.3234	48.28	26.45	95.3962	48.29	26.45	95.3257
5	28.98	12.44	95.0943	28.99	12.45	95.1992	28.99	12.44	95.1002
7	21.72	9.81	93.456	21.73	9.82	93.574	21.73	9.81	93.4678
9	18.36	8.91	91.5978	18.37	8.92	91.7261	18.37	8.92	91.616

Table 8: THD and Efficiency of CHB, NPC and FC at 75% Mod. Depth in SWM

Case 3: Depth of modulation 75% (Carrier frequency 1000 Hz)									
No. of Levels	CHB			NPC			FC		
	THD (%)		Efficiency (%)	THD (%)		Efficiency (%)	THD (%)		Efficiency (%)
	Voltage	Current		Voltage	Current		Voltage	Current	
3	48.32	26.42	95.9578	48.32	26.42	96.03	48.32	26.42	95.9598
5	28.98	12.44	96.425	28.99	12.45	96.5266	28.99	12.44	96.4292
7	21.72	9.81	95.446	21.73	9.82	95.5584	21.73	9.81	95.4542
9	18.26	8.81	94.2304	18.27	8.82	94.3509	18.27	8.82	94.243

Table 9: THD and Efficiency of CHB, NPC and FC at 100% Mod. Depth in SWM

Case 4: Depth of modulation 100% (Carrier frequency 1000 Hz)									
No. of Levels	CHB			NPC			FC		
	THD (%)		Efficiency (%)	THD (%)		Efficiency (%)	THD (%)		Efficiency (%)
	Voltage	Current		Voltage	Current		Voltage	Current	
3	48.34	26.4	97.2759	48.34	26.4	97.3479	48.34	26.4	97.2778
5	28.98	12.44	97.0947	28.99	12.45	97.1947	28.99	12.44	97.0981
7	21.72	9.81	96.4515	21.73	9.82	96.5607	21.73	9.81	96.4578
9	18.16	8.71	95.566	18.17	8.72	95.6824	18.17	8.72	95.5757

5.8 Tabulate Results

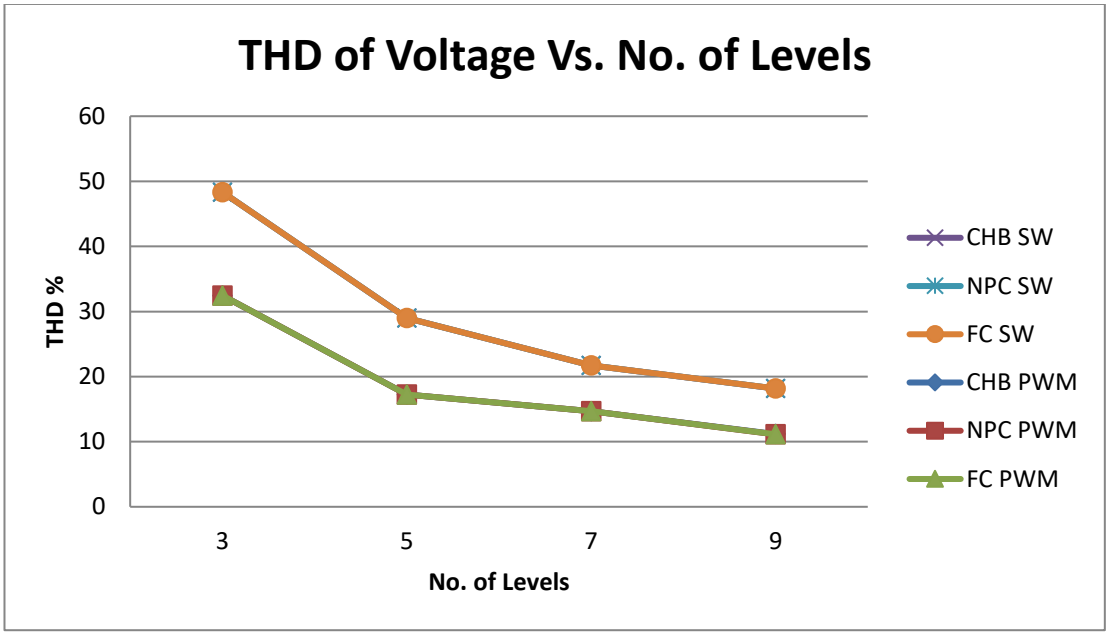

Figure 110: Graph of THD of Voltage vs. Number of Levels

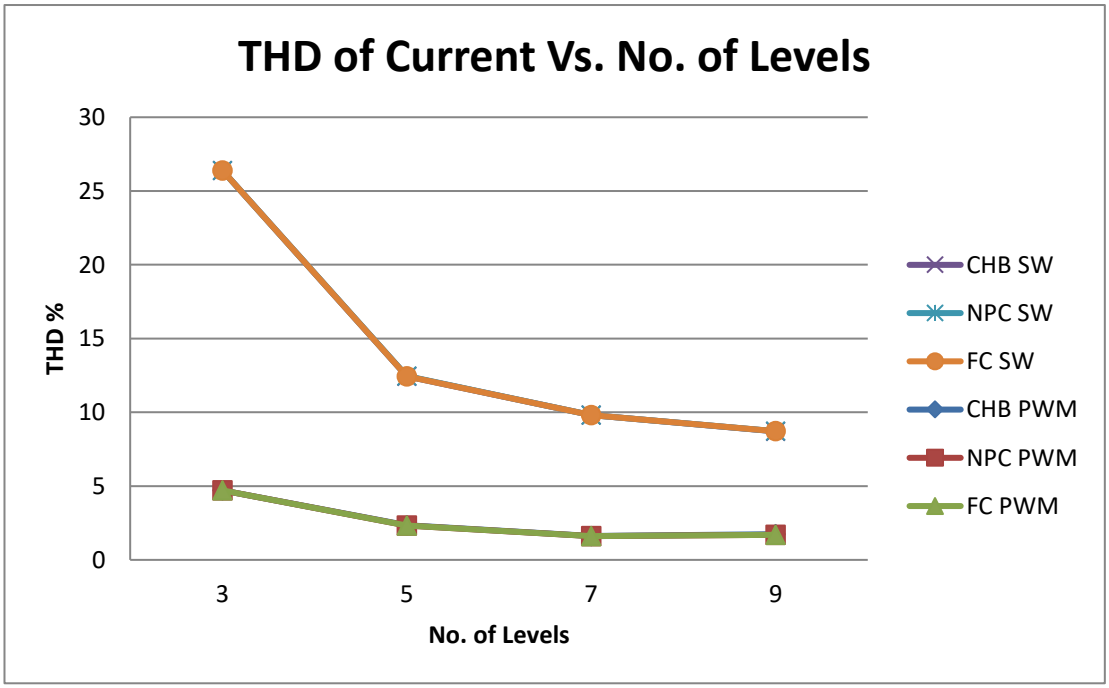

Figure 111: Graph of THD of Current vs. Number of Levels

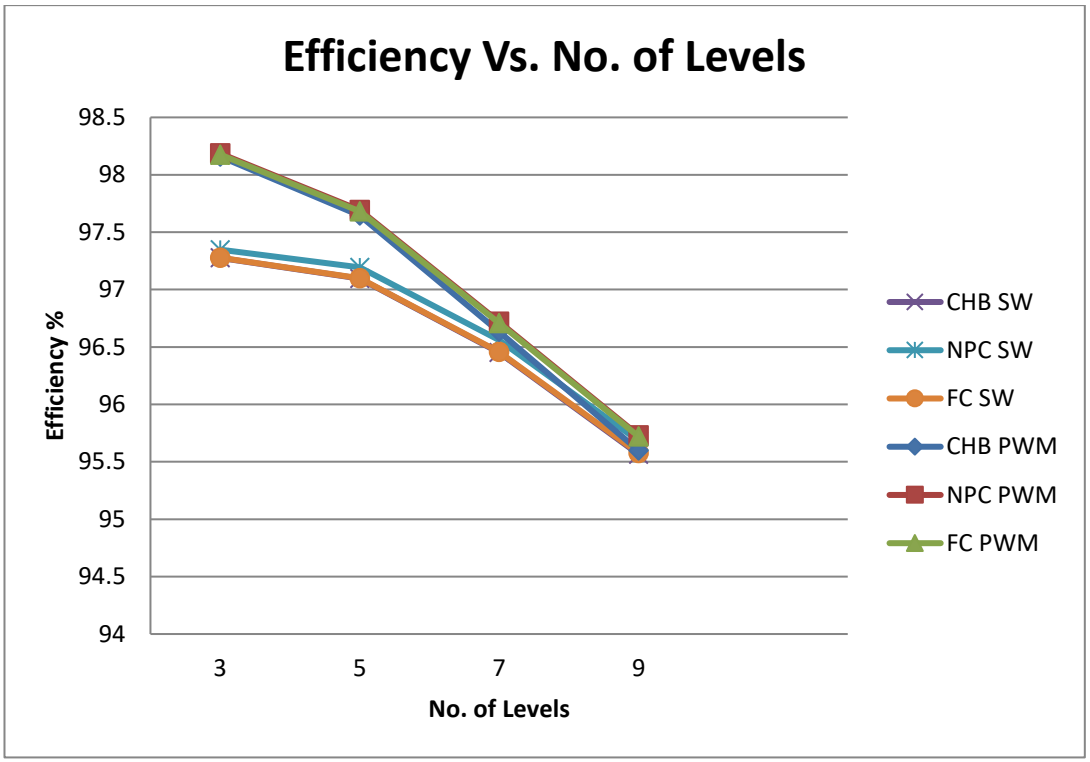

Figure 112: Graph of Efficiency vs. Number of Levels

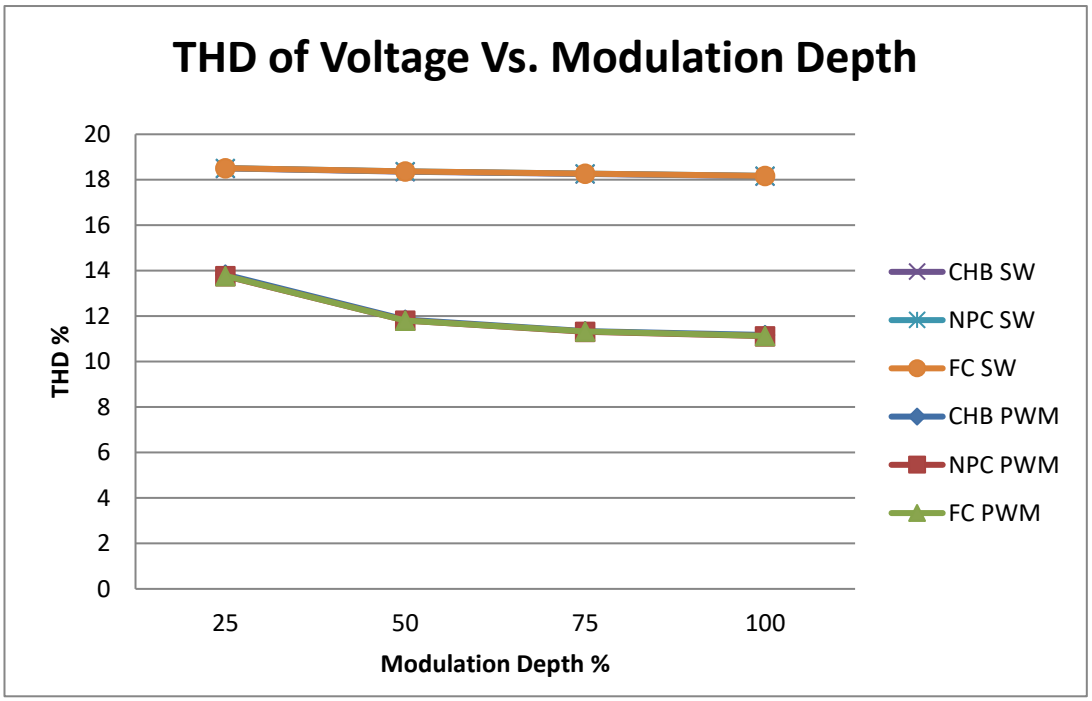

Figure 113: Graph of THD of Voltage vs. Modulation Depth

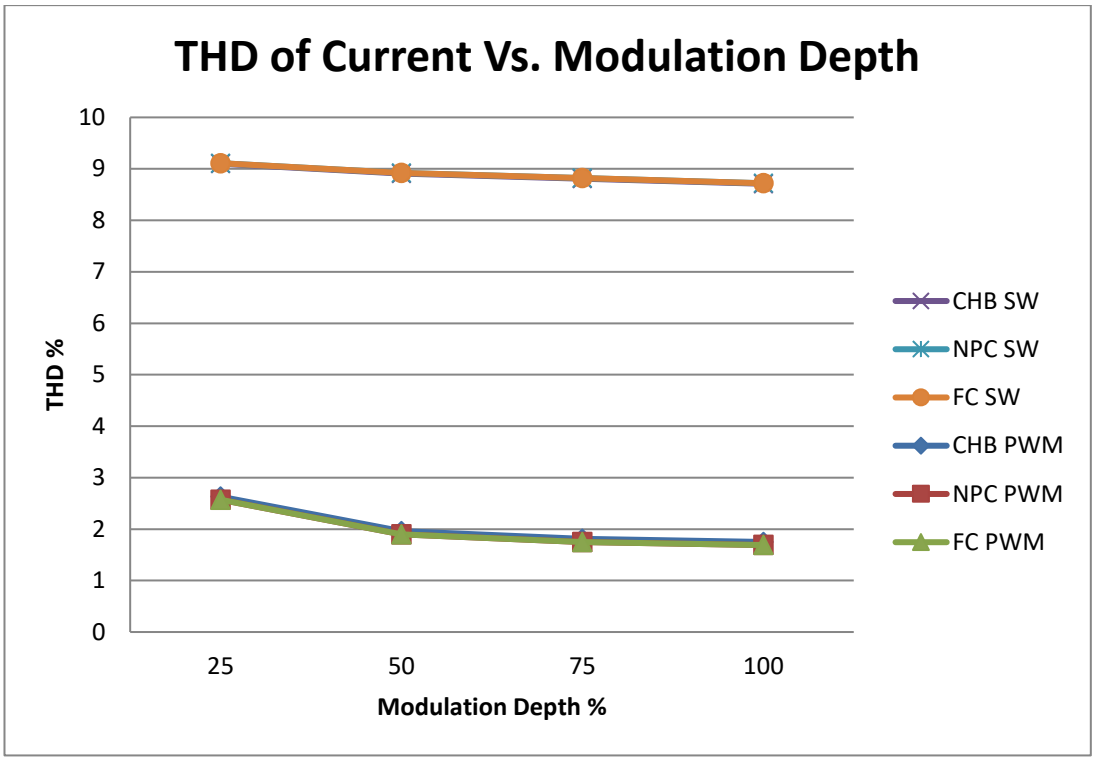

Figure 114: Graph of THD of Current vs. Modulation Depth

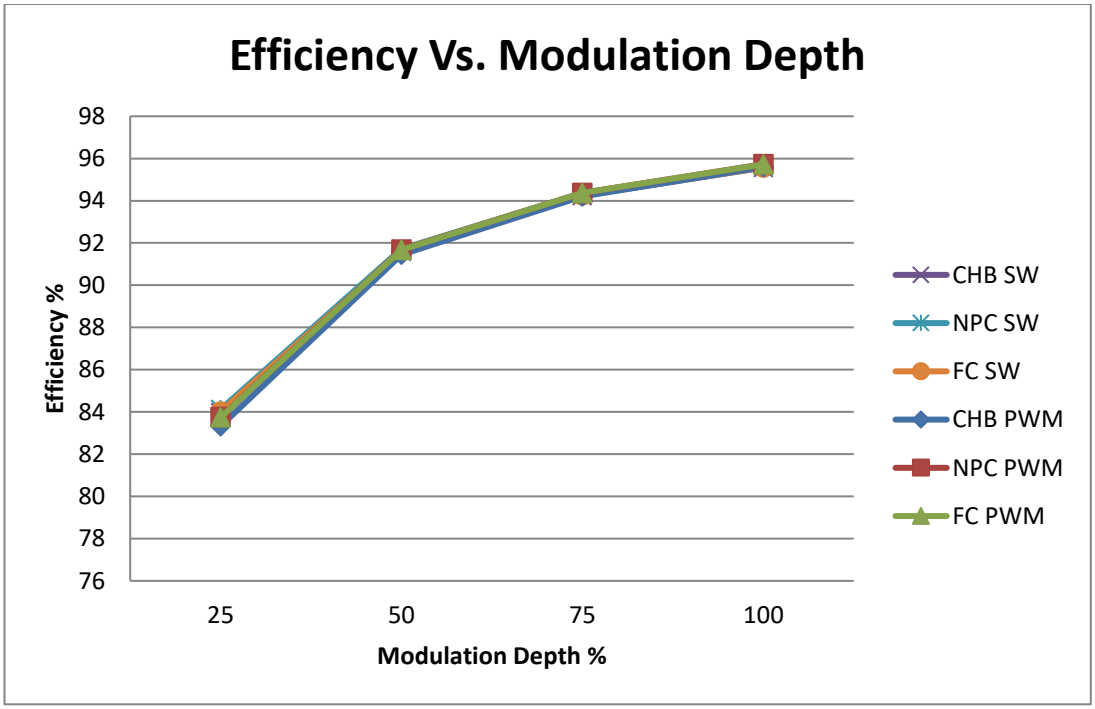

Figure 115: Graph of Efficiency vs. Modulation Depth

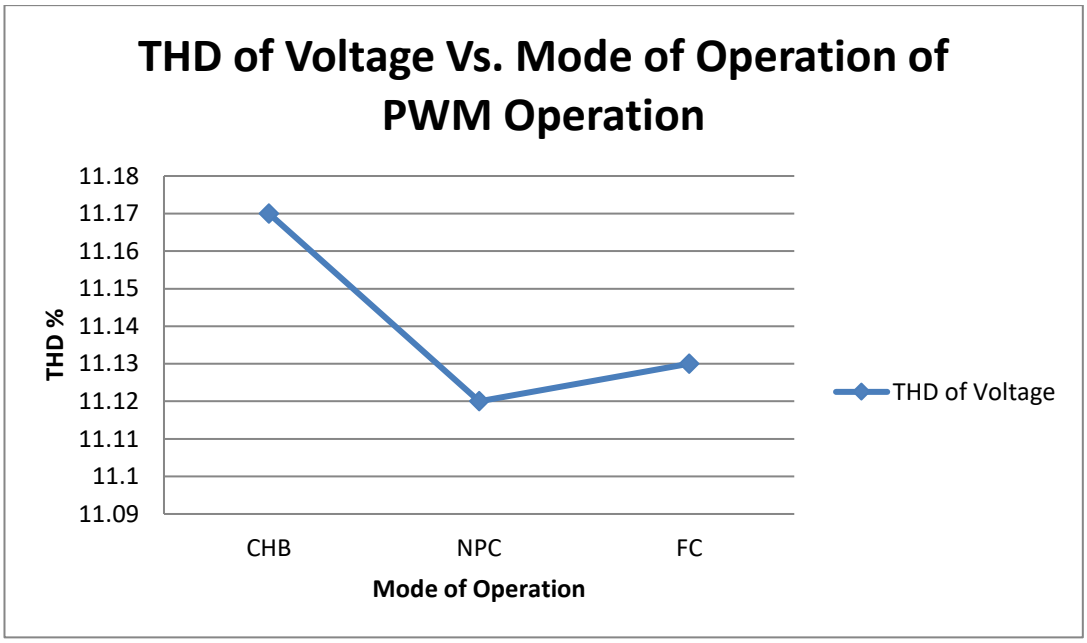

Figure 116: Graph of THD of Voltage vs. Mode of Operation in PWM

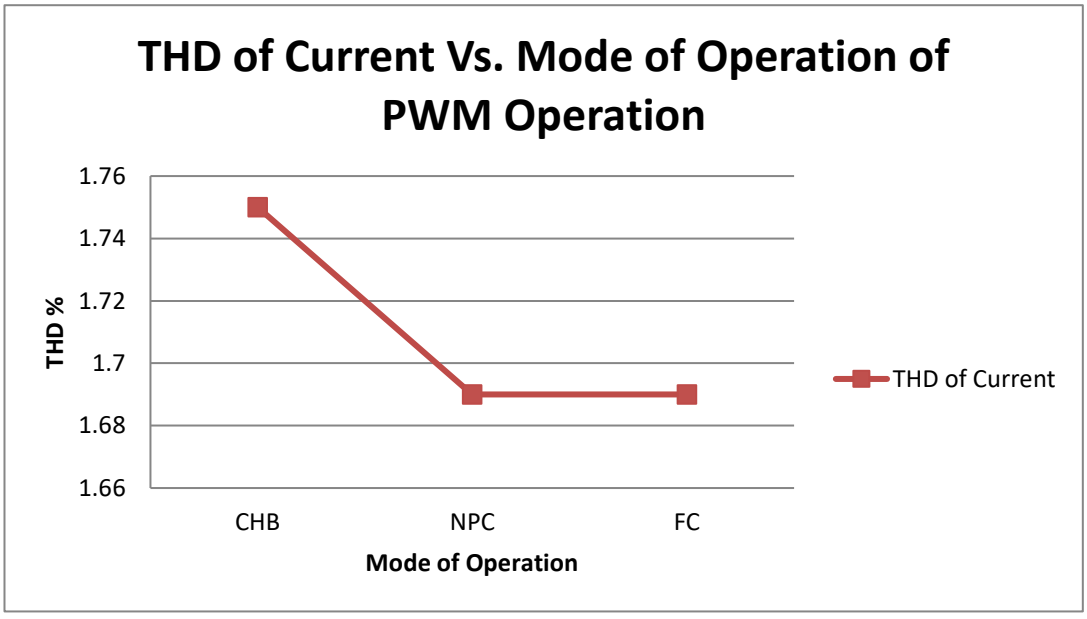

Figure 117: Graph of THD of Current vs. Mode of Operation in PWM

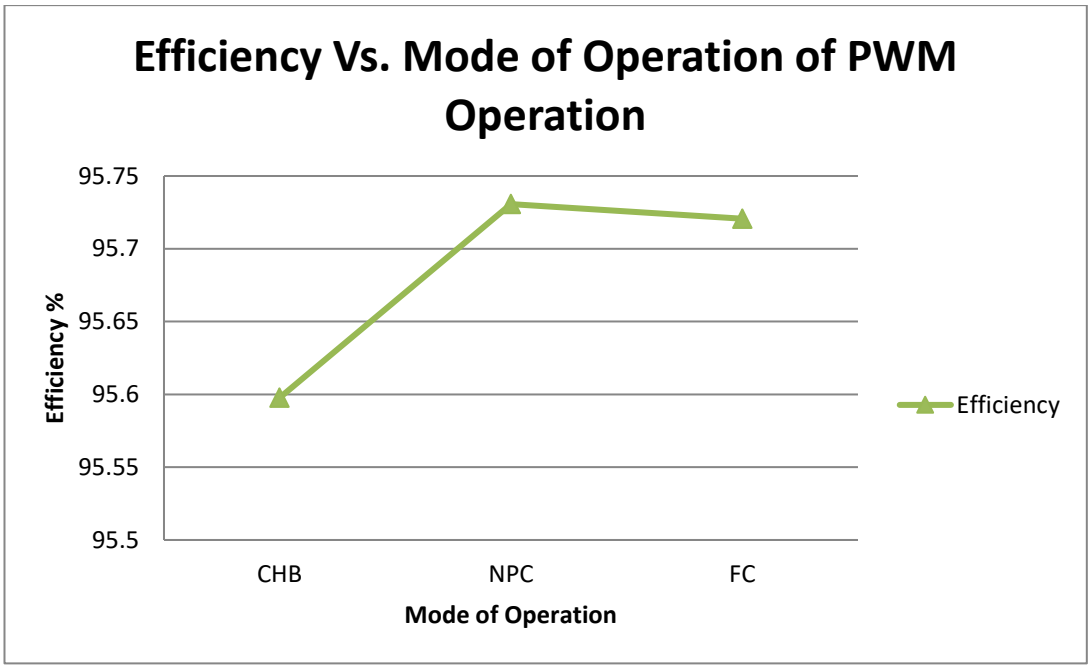

Figure 118:: Graph of Efficiency vs. Mode of Operation in PWM

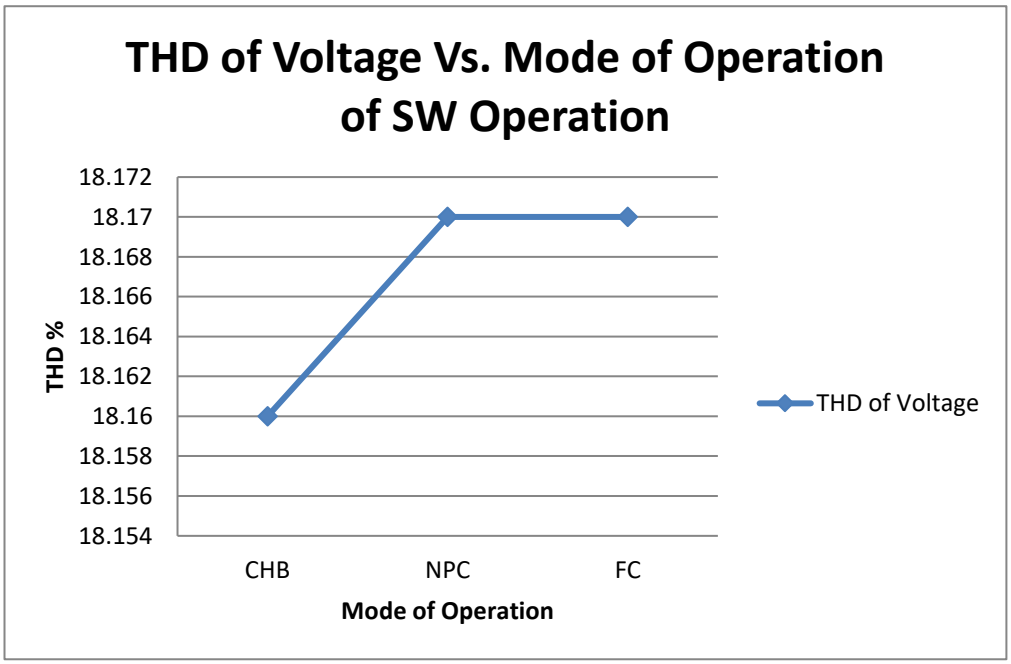

Figure 119: Graph of THD of Voltage vs. Mode of Operation in SWM

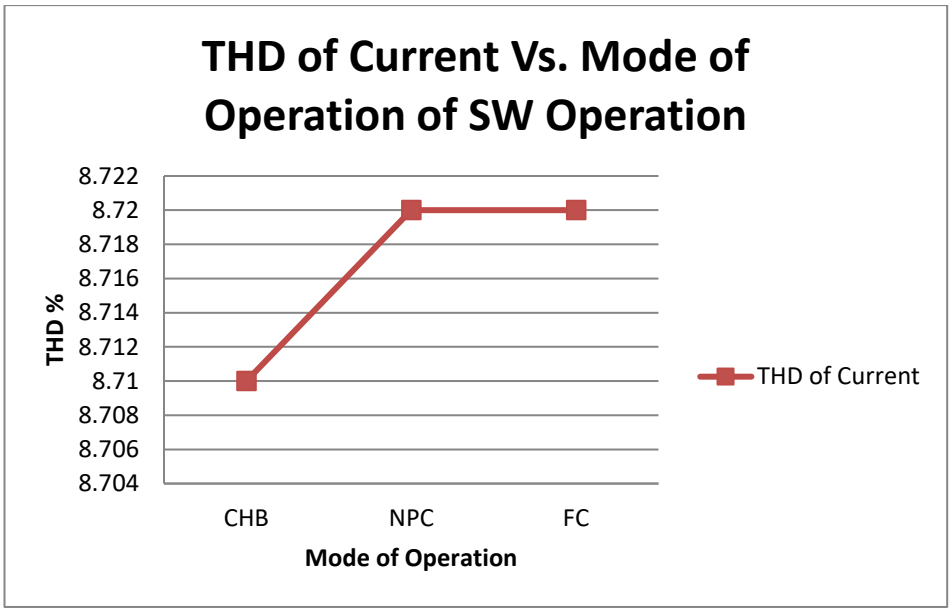

Figure 120: Graph of THD of Current vs. Mode of Operation in SWM

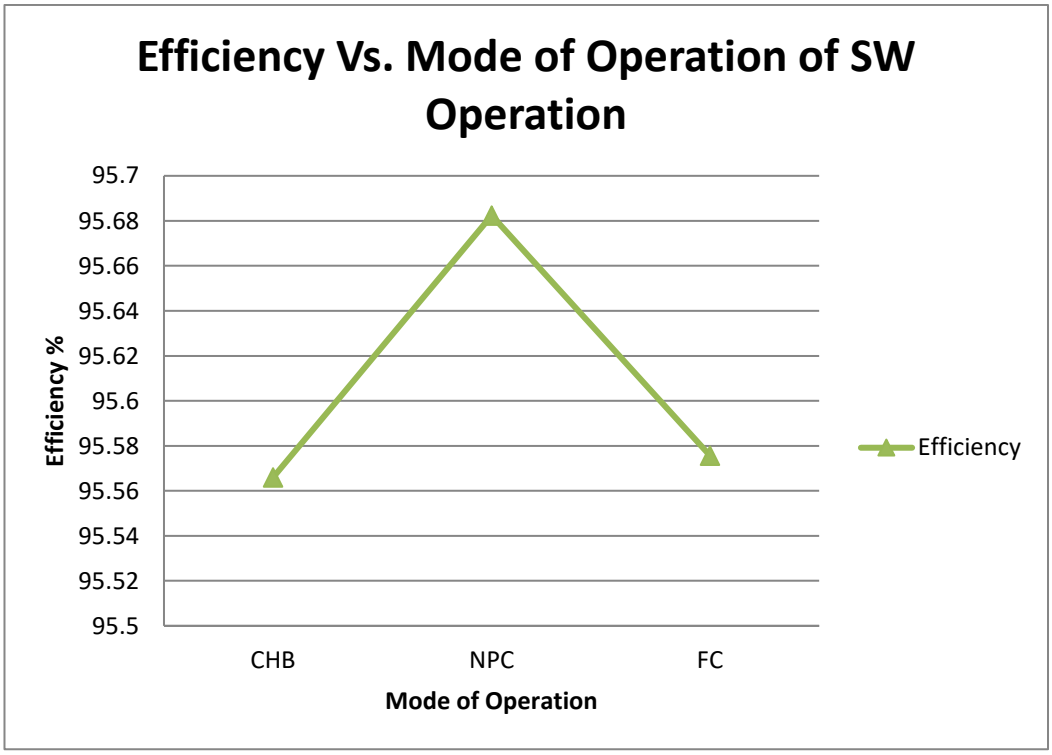

Figure 121: Graph of Efficiency vs. Mode of Operation in SWM

CHAPTER 6

6. CONCLUSION

6.1 Total Harmonic Distortion Convenience

The output wave forms of Pulse Width Modulation and Square Wave Modulation were compared and following were identified.

Compared to Square Wave Modulation, Pulse Width Modulation output has a lower THD. Further, when the inverter number of levels increases the THD reduces in both Pulse Width Modulation and Square Wave Modulation. There is no much difference in Total Harmonic Distortion of output waveform to the mode of operation of the inverter.

6.2 Over all Operational Convenience

When the number of levels increases the complexity of selecting the switching states increases.

PWM has redundant switching states which can be used efficiently to obtain symmetrical thermal loading among switches. Further, when the inverter is operated in Cascaded Half Bridge mode it has modularized construction capability which is easier to extend number of levels compared to Flying Capacitor mode and Neutral Point Clamped mode.

To have a low Total Harmonic Distortion inverter should have higher number of levels. When number of levels increases the number of capacitors also increase. This will result the size and weight of the inverter increases and become bulky. This will cause the complexity of operation increases and the price of the inverter increase. Therefore, depending on the application and the requirement we should select the number of levels and the mode of operation.

This is a tradeoff between weight, price, complexity and THD.

When the inverter number of levels increase, Generalized Multilevel Inverter become bulky because of the number of capacitors increase. This will cause the packaging difficult and packaging size increase.

The Cascaded Half Bridge Inverter should have separate DC sources. However, when the Cascaded Half Bridge Inverter is constructed using the Generalized Multilevel Inverter, requirement of separate DC sources can be eliminated.

6.3 Evaluation of Performance

When the inverter is operated in Pulse Width Modulation the THD of voltage and current waveforms is lower compared to Square Wave Modulation. Further, when the inverter is operated in Pulse Width Modulation the efficiency of this proposed inverter is higher compared to Square Wave Modulation.

The THD can be reduced in voltage and current waveforms by increasing number of levels of the converter. However, when the number of levels increases converter efficiency reduces.

Further, Total Harmonic Distortion of voltage and current wave forms can be reduced by increasing the Modulation Depth of the inverter. When increasing the Modulation Depth efficiency of the inverter also increases.

When the inverter is operated in Pulse Width Modulation the lowest Total Harmonic Distortion of output voltage and current is obtained when the inverter is operated in Neutral Point Clamped mode. The highest efficiency is also obtained when the inverter is operated in Neutral Point Clamped mode.

When the inverter is operated in Square Wave Modulation the lowest THD of output voltage and current is obtained when the converter is operated in Cascaded Half Bridge mode. The highest efficiency is obtained when the inverter is operated in Neutral Point Clamped mode.

6.4 Total Harmonic Distortion Convenience

The lowest THD of output waveform is obtained when the converter is operated in PWM.

Either the inverter is operated in Pulse Width Modulation or Square Wave Modulation the Total Harmonic Distortion can be reduced by increasing the number of levels.

Either the converter is operated in PWM or SWM the Total Harmonic Distortion of the inverter has no much difference whether it is operated in Flying Capacitor mode or Neutral Point Clamped mode or Cascaded Half Bridge mode.

6.5 Efficiency Convenience

When the number of levels increase either the converter is operated in Pulse Width Modulation or Square Wave Modulation efficiency of the converter reduce.

Either the inverter is operated in Pulse Width Modulation or Square Wave Modulation the efficiency of the inverter has no much difference whether it is operated in Flying Capacitor mode or Neutral Clamp mode or Cascaded Half Bridge mode.

6.6 Over all Operational Convenience

When number of levels the inverter is operated increases, the complexity of providing switching signals to the IGBTs also increases as the number of IGBTs increases.

When the inverter is operated in Pulse Width Modulation, it has redundant switching states. Out of these redundant switching states, the switching states which provide symmetrical thermal loading among switches were selected.

When the inverter is operated in Cascaded Half Bridge mode, it provides modularized construction capability. This helps to increase number of levels of the inverter easily compared to Flying Capacitor and Neutral Point Clamped mode.

When achieving low Total Harmonic Distortion and high efficiency the size, weight and complexity of the circuit and algorithm of the inverter increase. It is a tradeoff between price and achieving required level of Total Harmonic Distortion and efficiency. Therefore, we should select the level of Total Harmonic Distortion and efficiency based on the application requirements.

When the number of levels of the inverter is increased the Generalized Multilevel Inverter becomes bulky as the number of capacitors increase and also packaging of the inverter becomes difficult. Therefore, inverter package size and weight increases.

When the inverter is operated in Cascaded Half Bridge mode separate DC sources are required. However, when the Cascaded Half Bridge mode is implemented in Generalized Multi Level Inverter the requirement of separate DC sources is eliminated.

The Generalized Multilevel Inverter allow user to switch between inverter operation mode based on the application requirements. For instance, when taking off and landing an aircraft, interference to the aircraft control system should be low. Therefore, Total Harmonic Distortion of the aircraft power system inverter should be very low. During aircraft takeoff and landing the Generalized Multilevel Inverter should be operated in Neutral Point Clamped mode in Pulse Width Modulation operation where it has the lowest Total Harmonic Distortion. During aircraft flying the inverter should be operated in Neutral Point Clamped mode or Flying Capacitor mode where it has the highest efficiency. This will helpful to save aircraft fuel during long distance flying. Therefore, the capability to switch between mode of operation on the

go without interruption is a very useful advantage of Generalized Multilevel Inverter.

Benefits of Generalized Multilevel Inverter

- Increased power rating inverters can be constructed.
- Major multilevel inverter configurations such as FC, NPC & CHB can be configured.
- Low voltage stress on the power switches.
- Balance each voltage level regardless of load characteristics.
- Active or reactive power conversion.
- Low electromagnetic interferences.
- Improved output waveforms.
- Simulation study shows PWM for pulse generation, THD can be lowered.
- THD is decreased by increasing the number of levels.
- Reduced filter size.
- Higher number of capacitors allow converter to operate through short time period outages and deep voltage sags.
- In high power systems, can replace existing systems that use traditional multi-pulse converters without using transformers.
- Based on the application requirements Generalized Multilevel Inverter allow the user to switch between the mode of operation on the go without any interruption.

Application of Cascaded Half Bridge Inverter

- Suited for various renewable energy sources such as photovoltaic, fuel cell and biomass plants.
- Alternative Current power supply.
- Variable speed drive applications.
- Possibility to implement soft-switching.
- Flexible AC Transmission Systems (FACTS).
- Custom power devices.
- High power Adjustable Speed Drives.

- Electric and Hybrid vehicles.
- Photovoltaic power conversion.
- Uninterruptible Power Supplies.
- Magnetic Resonance Imaging.

Application of Neutral Point Clamped Inverter

- Adjustable speed motor drive applications.
- High voltage back to back inter connections.
- Custom power devices.
- Conveyors.
- Marine applications.
- Regenerative applications such as mining and renewable energy.

Application of Flying Capacitor Inverter

- Real and reactive power flow control.
- Adjustable Speed Drives.
- Medium Voltage traction drives.

6.7 Recommendation

Lower Total Harmonic Distortion can be obtained when Generalized Multi Level Inverter is operated in higher number of levels. However, as the number of levels increase bulky ness and the cost of the inverter increase while reducing the efficiency of the inverter. Therefore, considering the application & the purpose, we have to select the most suitable number of levels. Also, lower Total Harmonic Distortion can be obtained when the Generalized Multi Level Inverter is operated in Pulse Width Modulation mode.

Higher efficiency can be obtained when the Generalized Multi Level Inverter is operated in higher Modulation Depth.

Both higher efficiency and lower Total Harmonic Distortion can be obtained when the Generalized Multi Level Inverter is operated in Neutral Point Clamped mode.

Generalized Multilevel Inverter can be operated in FC, NPC, CHB modes and mode of operation can be interchanged on the go without any interruption based on the connected load requirements.

6.8 Conclusions

The goal of this research was to develop control and switching interfaces to operate a 9-level Generalized Inverter in CHB, NPC and FC modes for operation in 3, 5, 7 and 9 levels with square-wave and PWM control and to investigate relative performances, in terms of THD and efficiency.

In this study first identified switching paths within a generalized 9-level inverter for CHB, NPC and FC modes of different levels and designed switching algorithms corresponding to square-wave and PWM control of each mode of operation. Then, simulated each mode and level with different controls in MATLAB and investigated input output performances.

Investigation of influence on the operation of the inverter during switching of inverter mode from one type to another or changing number of levels of the inverter while operating the inverter is an interesting area for further investigation and research.

The study has verified that in PWM operation the lowest THD can be obtained when the inverter is operated in NPC mode with higher modulation depth and higher number of levels. In SW operation the lowest THD can be

obtained when the inverter is operated in CHB mode with higher modulation depth and higher number of levels. In PWM and SW operation NPC has highest efficiency with higher modulation depth and lower number of levels.

By considering the outcomes of this research study, as a conclusion it can be stated that the proposed model will be a convenient model to obtain characteristics of CHB, NPC and FC modes for operation in 3, 5, 7 and 9 levels with square-wave and PWM control.

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