IMPLEMENTATION OF A PEDOBAROGRAPHIC SYSTEM THROUGH EFFECTIVE CROSSTALK SUPPRESSION WITH AN ALL PROGRAMMABLE SYSTEM ON CHIP

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Declaration

I declare that this is my own work and this thesis/dissertation does not incorporate without acknowledgement any material previously submitted for a Degree or Diploma in any other University or institute of higher learning and to the best of my knowledge and belief it does not contain any material previously published or written by another person except where the acknowledgement is made in the text.

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Dedication

There are a number of people without whom this thesis might not have been written, and to whom I am greatly indebted.

To my beloved parents who have been the source of encouragement and inspiration to me throughout my life. And also for the myriad of ways in which, throughout my life, they actively supported me in my determination to find and realise my potential.

To my dear wife, who provided a invaluable practical and emotional support during the challenges of postgraduate studies without which, completion of this dissertation was not possible. You always inspire me and I am truly thankful for having you in my life.

A special feeling of gratitude to my loving sister who never left my side and are very special and my grandmother who raised me, loved me, and taught me to speak.

Finally, I am dedicating this work to all my teachers throughout my life, especially to my mentors at University of Moratuwa, under whose constant guidance, support and inspiration I was able to complete this dissertation. They not only enlightened me with academic knowledge but also gave me valuable advice and opened my my eyes for novel prospects that I never knew existed.

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Abstract

Diabetes Mellitus which is characterized by longstanding hyperglycemia, promote diabetic peripheral neuropathy (DPN) and peripheral artery diseases (PAD) which invoke ulcerations especially on the foot plantar ultimately leads to amputations related morbidity and mortality. Recent clinical studies have identified distinct associations between DPN and foot plantar pressure, and PAD and foot plantar temperature. Hence, development of technology to analyze foot plantar pressure (pedobarography) and foot plantar temperature (pedothermography) to infer DPN and PAD associated diseases at the onset have recently stirred a significant interest among the scientific community.

In the present study, we have primarily investigated the possibility of implementing a highly accurate large piezoresistive platform sensor array (a pedobrographic system) with an improved readout mechanism. We devised a readout circuit to mitigate inherent crosstalk interference with an improved scanning architecture implemented using a decoder-transistor based row driving electrodes and related electronics compatible with high frequency sensing. Then, the developed readout circuit was extensively validated and the proposed implementation was able to make measurements of significant accuracy with errors $< 1\%$ while not compromising the shape accuracy of the measured object. Initiatives were also taken to improve the data acquisition rate despite massive sensor data influx from 30,000 sensels. A Xilinx Zynq APSoC based data acquisition system was implemented to scan the entire array with 30,000 sensels and the analysis showed that the system demonstrated expected behavior. Overall, the proposed implementation entertained both static and dynamic pressure measurements of a foot plantar. A subsequent static calibration of the piezoresisitive sensor array was conducted using weight plates and the calibrated sensor array was validated against an existing commercial plantar pressure measurement system to determine its performance.

In addition, possibility of implementing a screening tool for pedothermographic assessment using near infrared (NIR) technology was investigated to provide an overall assessment of both foot planters in a single frame and record both regional and point temperatures of the foot plantar. The proposed thermal imaging system is anticipated to be used in routine clinical assessment of diabetic foot complications at diabetic clinics to provide improved diagnostics, thereby contributing to prevention of diabetic foot ulcerations, amputations and related morbidity.

List of Abbreviations

Abbreviation	Description
AA	Anti–Aliasing
ABI	Ankle-Brachial Index
ADC	Analog to Digital Converter
AGC	Automatic Gain Control
APSoC	All Programmable System on Chip
ASIC	Application Specific Integrated Circuit
AXI	Advanced eXtensible Interface
BRAM	Block Random Access Memory
CAN	Controller Area Network
CMOS	Complementary Metal-Oxide-Semiconductor
CPT	Current Perception Threshold
DAQ	Data Acquisition
DFU	Diabetic Foot Ulceration
DMA	Direct Memory Access
DPN	Diabetic Peripheral Neuropathy
DSP	Digital Signal Processing
EBT	Element Being Tested
EMG	Electromyography
ESR	Equivalent Series Resistance
FF	Flip-Flop
FPGA	Field Programmable Gate Array
Gbps	Giga-bits per second

GPIO	General Purpose Input Output
GRF	Ground Reaction Force
GUI	Graphical User Interface
HDL	Hardware Description Language
HDMI	High-Definition Multimedia Interface
IP	Intellectual Property
IWGDF	International Working Group on Diabetic Foot
LCT	Liquid Crystal Thermography
LDO	Linear Dropout Regulators
LOPS	Loss of Peripheral Sensation
LUT	Look Up Table
Mbps	Mega bits per second
Mux	Multiplexer
NCS	Nerve Conduction Studies
NCV	Nerve Conduction Velocity
NIR	Near Infrared
Op-amp	Operational Amplifier
PAD	Peripheral Artery Disease
PCB	Printed Circuit Board
PL	Programmable Logic
PS	Processing System
PSoC	Programmable System on Chip
QST	Quantitative sensory threshold
RTL	Register Transfer Level
RSA	Resistor Sensor Array
SBC	Single Board Computer
SDK	Software Development Kit
SMD	Surface Mount Devices
SMD	Surface-Mounted Device
SMPS	Switch Mode Power Supply

S-NSE-ZP	Setting Non-Scanned Electrode Zero Potential
S-NSDE-ZP	Setting Non-Scanned Driving Electrode Zero Potential
S-NSSE-ZP	Setting Non-Scanned Sampling Electrode Zero Potential
SPST	Single Pole Single Throw
SSH	Secure Shell
TBI	Toe-brachial Index
UART	Universal Asynchronous Receiver-Transmitter
USB	Universal Serial Bus
VFM	Voltage Feedback Method
VF-NSE	Voltage Feedback Non-Scanned Electrode
VF-NSDE	Voltage Feedback Non-Scanned Driving Electrode
VF-NSSE	Voltage Feedback Non-Scanned Sampling Electrode
VNC	Virtual Network Computing
WHO	World Health Organization
WHS	Worst Hold Slack
WNS	Worst Negative Slack
ZPM	Zero Potential Method

List of Appendices

CHAPTER 1

Introduction

1.1 Background

Diabetes Mellitus continues to grow at a pandemic proportion as a severe chronic and non-communicable disease with several long term complications leading to morbidity and mortality [1, 2]. It is a physiological debility caused by hyperglycemia either due to insulin resistance or insufficient insulin secretion by the pancreas which result in macro and microvascular disorders [3].

The International Working Group on Diabetic Foot (IWGDF) in their quadrennial report in 2019 [2] estimated that nearly 422 million people suffer from diabetes worldwide (8.5% of the world population). Incidentally, more than 80% of these reported cases are from developing countries (low-to-middle income countries) [4]. Apparently, these disconcerting figures are estimated to grow over 552 million (9.9% of the world population) by 2030 at the current rate.

Moreover, Diabetes is also associated with significantly high morbid-mortality rates and premature deaths in the world. World Health Organisation (WHO) reports that diabetes has been the primary cause of 1.5 million deaths worldwide in the year 2019 [5]. In addition, WHO dictates that there has been a total of 2.2 million deaths due to high blood glucose in the year 2012.

Figure 1.1: Diabetic foot ulcer (Deep Ulcer) in the foot plantar. Adapted from Cooney et al. [6]

Meanwhile, it had been previously estimated that diabetes is prevalent among 20% of the urban population of Sri Lanka [7, 8]. However, a recent study by Somasundaram et al. [9] indicates that this figure has exponentially risen to 27.6%. Alarmingly, one third of overt diabetes cases in Sri Lanka remain undiagnosed [1, 8]. The risk of not diagnosing and subsequently leaving these patients untreated for extended duration prompt several secondary complications of diabetes including cardiovascular diseases, retinopathy, glaucoma, nephropathic conditions and foot related complications such as ulcers [4, 10].

1.2 The Diabetic Foot

An infection, ulceration or tissue destruction in the lower limb extremity of diabetic patients as a result of Diabetic Peripheral Neuropathy (DPN) and/or Peripheral Artery Disease (PAD) can be identified as a Diabetic Foot [2, 3]. Diabetic foot inadvertently affect the peripheral nerves and peripheral blood vessels through complex metabolic pathways leading to Loss of Peripheral Sensation (LOPS) and decreased blood supply to lower foot extremities (ischemia) respectively. LOPS predisposes the foot to injuries and restriction of blood flow means that the resultant injuries are poorly healed. If left untreated for prolonged duration, most of these foot complications lead to formation of ulcers.As a matter of fact, DPN and PAD are the two major precursors which play a pivotal role in developing ulcers of diabetic patients [2].

Therefore, diabetic foot is a serious complication of diabetic mellitus as it is a source of considerable suffering for the patient while imparting a huge burden on the healthcare system. According to Armstrong et al. [11], $237 billion had been attributed as direct costs for treating diabetic foot complications in the USA during the year 2017 alone compared to the $80.2 billion as direct costs attributed to treatment of cancer in USA during the same year.

In fact, diabetes is the most prominent cause for non-traumatic lower limb amputation in the world with severe mortality rates even higher than “many varieties of cancer” [4]. Screpnek et al. [12] declares that, diabetic foot ulcers accounted for more Emergency Department admissions in USA than cancer, heart disease and chronic kidney diseases combined. Ulcers in the lower limbs often lead to amputations. Consequently, diabetic mellitus remains to be the primary cause of lower limb amputation in the world [2, 4]. Evidently, a diabetes mellitus related lower limb is amputated at every twenty seconds somewhere in the world [2]. Thus, the quality of life, livelihood as well as the social participation of diabetic patients decline over time while exerting a massive burden to the economy via increased healthcare costs.

Figure 1.2 is a simplified summary of how diabetes mellitus manifest dead to foot ulceration and subsequent amputations related morbidity through DPN and PAD complications. It also signifies the importance of diagnosing these complications at early stages that could lead to prevention or dampening the severe effect of DPN, PAD associated foot complications.

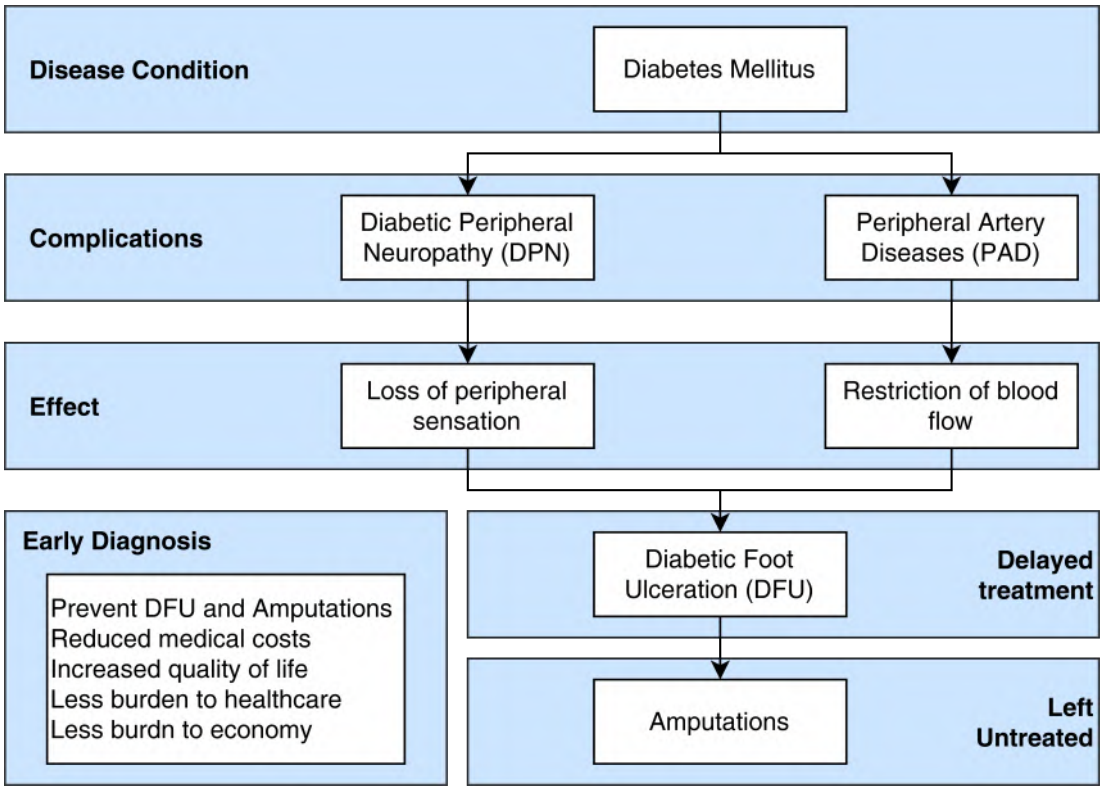

Figure 1.2: Simple diagrammatic illustration of how diabetes mellitus leads DPN and PAD that leads to ulcers and subsequent amputations.

1.3 Prevention of Diabetic Foot Ulcerations

A systematic review of literature suggests that proper control of glycemia, wearing appropriate footwear, patient education and regular assessment of the feet by a medical professional could curtail diabetic foot complications. The IWGDF has outlined a five-step process that should be followed to prevent diabetes related foot ulceration, thereby mitigating the morbidity and mortality associated with ulceration [2].

1. Examining the feet for LOPS and/or ischemia (risk factors of ulceration) in order to determine the level of risk
2. Regular inspection of the feet of patients with LOPS and/or ischemia for ulceration by a healthcare professional
3. Educating the patients about ulceration, signs and symptoms and methods of self-evaluation. In addition, increase awareness among the public.
4. Encouraging patients to wear appropriate footwear to protect their feet from secondary complications
5. Treatment for risk factors that lead to ulceration and subsequent amputations

The first step of the process follows the simple notion that the "Prevention is better than cure". Periodic assessment of the feet by a healthcare professional for Asymptomatic DPN, PAD and pre-ulcerative signs is performed to ensure that a person without ulceration symptoms is at a very low risk level (IWGDF risk 0 group) for ulceration.

If a patient who has already been diagnosed with DPN or PAD (IWGDF risk group 1, 2 or 3), should get their feet examined by a healthcare professional regularly to prevent or slowdown the progression of ulceration through effective modes of clinical care and/or intervention. The frequency of screening the feet is determined by the IWGDF risk group the patient is in.

The next step of the process is to create awareness about the severity of diabetic foot complications and prevention strategies among the general public while promoting techniques to self diagnose pre-ulceration with early symptoms and proper self-care methodologies among the patients. Apart from educating patients, their families and even the healthcare professionals working in the field are educated frequently.

Walking barefoot or using inappropriate footwear has been has been linked to foot trauma that ultimately leads to ulceration in patients with diabetes. Hence, special

therapeutic footwear prepared taking biomechanics, foot deformities, complications and amputations of the patient into consideration and are often promoted to be worn both indoors and outdoors for patients in IWGDF high risk groups.

The final step of the process is to provide continuous treatment for risk factors associated with ulceration through preventive mechanisms and/or surgical interventions.

1.4 Pedobarography and Thermography

As declared by the IWGDF (Section 1.3), Frequent medical examination of diabetic feet for DPN and PAD often help introducing medical interventions that prevent serious repercussions of diabetic foot ulceration. There are numerous strategies and techniques to effectively diagnose LOPS and ischemic complications of pre-ulcerative feet. These techniques are discussed in greater detail in Section 2.3.1 and Section 2.3.2. Out of the techniques, Pedobarograms and Thermograms have sparked a significant interest among the research community in the recent times, as two promising techniques to predict diabetic foot complications

The neurological complications posed by LOPS in the diabetic feet foster uneven pressure distribution over the foot plantar when the patient is standing upright. This abnormal pressure distribution can be mapped into a three-dimensional representation ($2 \times$ spacial dimensions in X and Y directions and $1 \times$'intensity of pressure' by depth dimension). Such a representation is called a "Pedobarogram". A sample pedobarogram is shown in Figure 1.3-A.

On the other hand, restriction of blood flow to the lower extremities of the diabetic foot plantar induce further complications such as inflammations which result in uneven temperature distribution across the foot plantar. A three-dimensional representation ($2 \times$ spacial dimensions, $1 \times$'intensity of temperature' by depth dimension) of such sort is termed a "Thermogram". A sample thermogram is shown in Figure 1.3-B.

Therefore, by incorporating pedobarographic and pedothermographic tools to regular patient feet screening processes, comprehensive foot examinations could be performed, susceptible areas in the foot plantar for complications could be distinguished and and patients could be directed for suitable treatments at preliminary stages, thereby, mitigating the serious repercussions associated with diabetic foot and related morbidity.

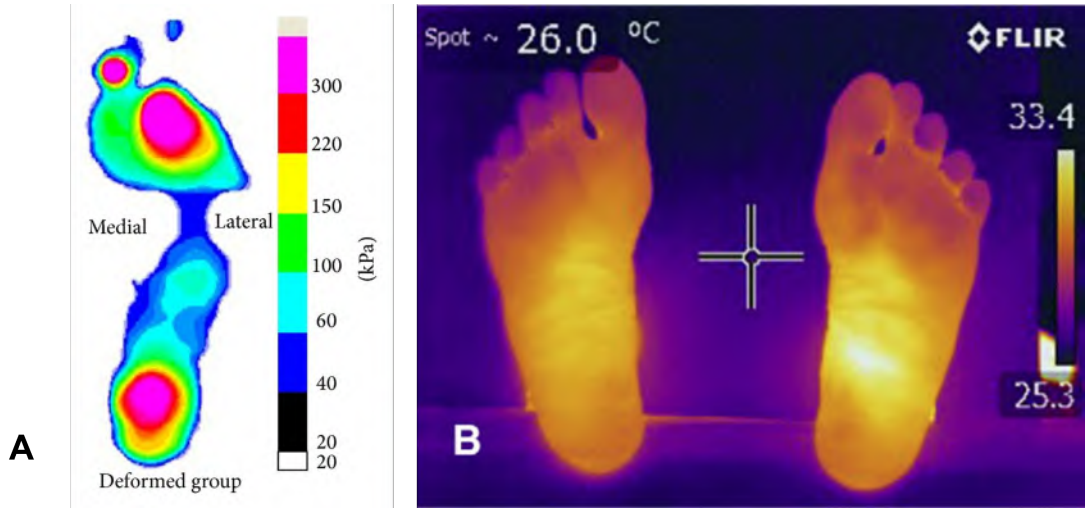

Figure 1.3: **A**: A pedobarogram of the right foot plantar with LOPS complications as recorded by Yu et al. [13]. **B**: A thermogram of the foot plantar of both feet as recorded by Silva et al. [14]

1.5 Aim of the Study

In the context of this study, we aimed at developing two separate, comprehensive devices that could facilitate the detection of LOPS and ischemic complications of the diabetic foot plantar by scanning the foot plantar for abnormal physiological parameters. The two devices maps the uneven pressure and temperature distributions of the foot plantar which reflect LOPS and ischemic complications. From hereon, the two realized devices will be referred to as the ‘Pedobarographic assessment tool’ and the ‘Pedothermographic assessment tool’ respectively.

1.6 Research Problem

Pedobarograms and pedothermograms of the foot plantar have recently been advocated to detect diabetic foot complications as they produce better clarity and efficacy than the traditional methods of diagnosing (discussed in Section 2.3.1 and Section 2.3.2).

In addition to taking static pressure measurements of the foot plantar, dynamic measurements tend to emphasize the areas of uneven pressure distribution during a gait cycle. These areas of uneven pressure distributions could be a result of LOPS, deformities of the foot or restricted mobility within the joints [2]. They generate comparatively extensive mechanical stresses in certain areas of the feet resulting in eccentric biomechanical loading which can be measured through a pedobarographic assessment tool.

In order to facilitate dynamic measurements, a spatially enhanced sensing platform (larger sensing area) with a sufficiently high operational frequency is desired. However, implementing a larger sensing platform for pedobarographic assessment incorporates several technological limitations that needs extensive research. Even existing commercial platform systems that could be adopted for plantar pressure measurements suffer from several limitations (discussed in Section 3.6), hence not the ideal solution.

Therefore, the main research problem of the present study dedicated to address is the extensive analysis required to implement such a pedobarographic assessment tool with increased sensing, spatial resolution, scanning frequency while mitigating crosstalk among sensors in close proximity.

1.7 Objectives

The main limitation of increased sensing area in pedobarographic assessment is the increased requirement of the number of sensing elements (sensels) which result in crosstalk among sensors 3.4. Therefore, the main objective of the present study was to mitigate the resulting crosstalk with a suitable suppression technique and evaluate its efficacy in terms of shape accuracy and measurement accuracy (Section 3.7). Followed by careful component selection to realize the proposed system with the identified crosstalk suppression mechanism. Upon implementation, the next objective was to conduct an analysis on the developed crosstalk suppression mechanism when used in scanning a large piezoresistive sensor array which is used for plantar pressure measurement.

In order to attain these high performance demands, FPGA based hardware acceleration was essential. Therefore, investigated the possibility pf implementing the pedobarographic assessment tool centered around an All Programmable System on Chip (APSoC) hardware platform which conprises of a dual core processor and FPGA on the same fabric. On that account, the main priority of the study was given for investigating the possibility of implementing a functional pedobarographic assessment tool by integrating a piezoresistive pressure sensor array to a custom-built data acquisition system, controlled with a AP-SoC platform, that will facilitate recording and interpretation of foot plantar pressure measurements and provide a detailed assessment of the foot plantar.

A secondary objective of the present study was to develop a suitable pedothermographic device to screen the diabetic feet to detect ischemic complications. A diagnostic tool that could perform an instantaneous screening of the foot plantar and provide pedothermographic data to perform an asymmetric analysis on the severity of the foot complications did not exist. Therefore, adhering to the strategies implemented in many areas of healthcare to facilitate diagnosis and prognosis of pathologies including early detection of cancer [15], the present research

investigated the possibility of developing a non-contact, instantaneous mechanism using near-infrared (NIR) thermography for screening of the diabetic foot plantar. Afterwards the accuracy of the thermal imaging sensor and related electronics to generate a thermogram with proper measurement accuracy and foot contour prediction ability were to be investigated. Hence, the objectives that the present study planned to accomplish are listed below.

1. To investigate a suitable FPGA centered pedobarographic architecture with provision for effective crosstalk suppression
2. To quantitatively analyze the implemented architecture in terms of,
    - Timing analysis of the circuit components
    - A data synchronization study.
    - Analysis on resulting time delays
    - Analysis of the effect of spatial resolution on the final readings
3. To validate the system and perform calibration
4. To conduct an observational study with live subjects from the subsequently developed devices.
5. Extract clinically significant features from the recorded data.

However, due to financial and resource constraints that arised during the research study due to Covid-19 pandemic situation forced to amend the above listed objectives as follows.

1. To investigate a suitable FPGA centered pedobarographic architecture with provision for effective crosstalk suppression
2. To quantitatively analyze the implemented architecture in terms of,
    - Timing analysis of the circuit components

- A data synchronization study.
- Analysis on resulting time delays

3. To validate the system and perform calibration

1.8 Overview of Proceeding Chapters

The proceeding three chapters (Chapter 2, 3 and 4) contain a detailed literature review about the background of the research. They discuss the DPN and PAD manifestations including existing methodologies to diagnose these complications in the present clinical setup. Moreover, the prospect of developing a fully fledged pedobarographic and thermographic assessment tools are discussed including limitations in the current methodologies and hardware.

They are followed by separate chapter on Pedobarographic assessment tool (Chapter 5. This chapter covers the four main aspects of developing the pedobarographic assessment tool, namely, readout circuit development, hardware implementation, data acquisition software development and the functioning of all separate entries as a single system. In addition to the methodology, this chapter presents all the results obtained from the assessment tool and a discussion of obtained results.

Similarly, a separate chapter on Thermographic assessment tool (Chapter 6) portrays the sensor selection process, device development process, the application development process, and the results obtained with the current implementation.

Finally, chapter on conclusion (Chapter 7) summarizes the implications of the present study, the improvements it requires to be used as a screening tool in a clinical setup.

CHAPTER 2

Diabetes and The Foot

2.1 Feet as an Indicator of Underlying Diseases

"Our feet often give clues that something is not quite right within our bodies."
-Tony Gavin- [16]

The foot plantar acts as the primary surface of interaction between the human body and the surrounding environment during locomotion. Most of the everyday activities we engage in are weight-bearing activities. Therefore, our foot plantar is constantly exposed to ground reaction forces which subject our feet to varying patterns of mechanical stress [17]. Clinical studies have shown that long term hyperglycemia results in impairment of the function of peripheral nerves and peripheral arteries [2, 10, 18]. As feet undergo constant mechanical stresses compared to any other organ/part of the body during day-to-day activities (standing, locomotion etc.), peripheral nerve impairment and peripheral artery impairment materialize in the foot plantar from very early stages giving rise to complications such as LOPS and ischaemia respectively [2, 10].

Podiatrists can often diagnose these complications by examining the feet for colour changes, swelling, nail discoloration, dryness, numbness (loss of sensation) and

temperature changes before it starts causing significant pain and discomfort to the patient. Figure 2.1 shows different stages of ulceration of a diabetic foot. Detection of ulceration symptoms at the early stages through effective risk assessment methodologies followed by subjecting patients with suitable treatments and glycemic control could prevent amputations and related morbidity by 85% [19].

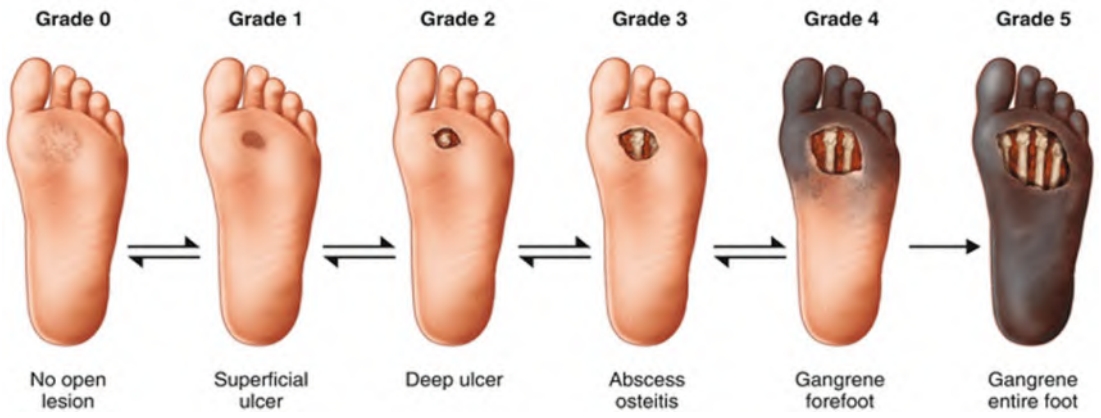

Figure 2.1: Different stages of Diabetic Foot Ulceration. In Grade 0 there exist no visual signs/symptoms which slowly progresses to a gangrene foot (Grade 6) where the foot tissue have has died due to restricted blood flow. Early detection and treatment could prevent progression of ulcer to the latter stages such as gangrene foot where amputation would be the only plausible solution. Image adapted from [20]

2.2 The Pathophysiology of Diabetic Foot Ulceration

Foot ulceration and resulting amputations prevail to be the driving causes for morbidity as well as emotional and physical burden for patients of diabetes mellitus. Although several factors govern the ulcer formation in lower limbs of diabetic patients, several clinical studies have successfully distinguished Diabetic Peripheral Neuropathy (DPN), Peripheral Artery Diseases (PAD) and structural deformities to be the three main pathways to Diabetic Foot Ulceration (DFU) [2, 4, 10]. Diabetic peripheral neuropathy and skeletal deformities alter the distribution of pressure in the foot plantar while PAD give rise to ischemic complications which manifest as

temperature variaitons in the foot plantar [2, 4]. These changes of pressure and temperature are good indicators of early diabetic foot complications that ultimately lead to ulceration. The pathway to diabetic foot ulceration through DPN, PAD and structural deformities are shown in Figure 2.2. Records suggest that more than 63% of DPN cases and more than 50% of ischemic cases lead to diabetic foot ulceration [4, 21]. Unfortunately, these percentages are gradually on the rise [22, 23]. Prompers et al. [23] has deduced that PAD are highly prevalent (incidence rate of over 70%) among patients who are 70 years or older.

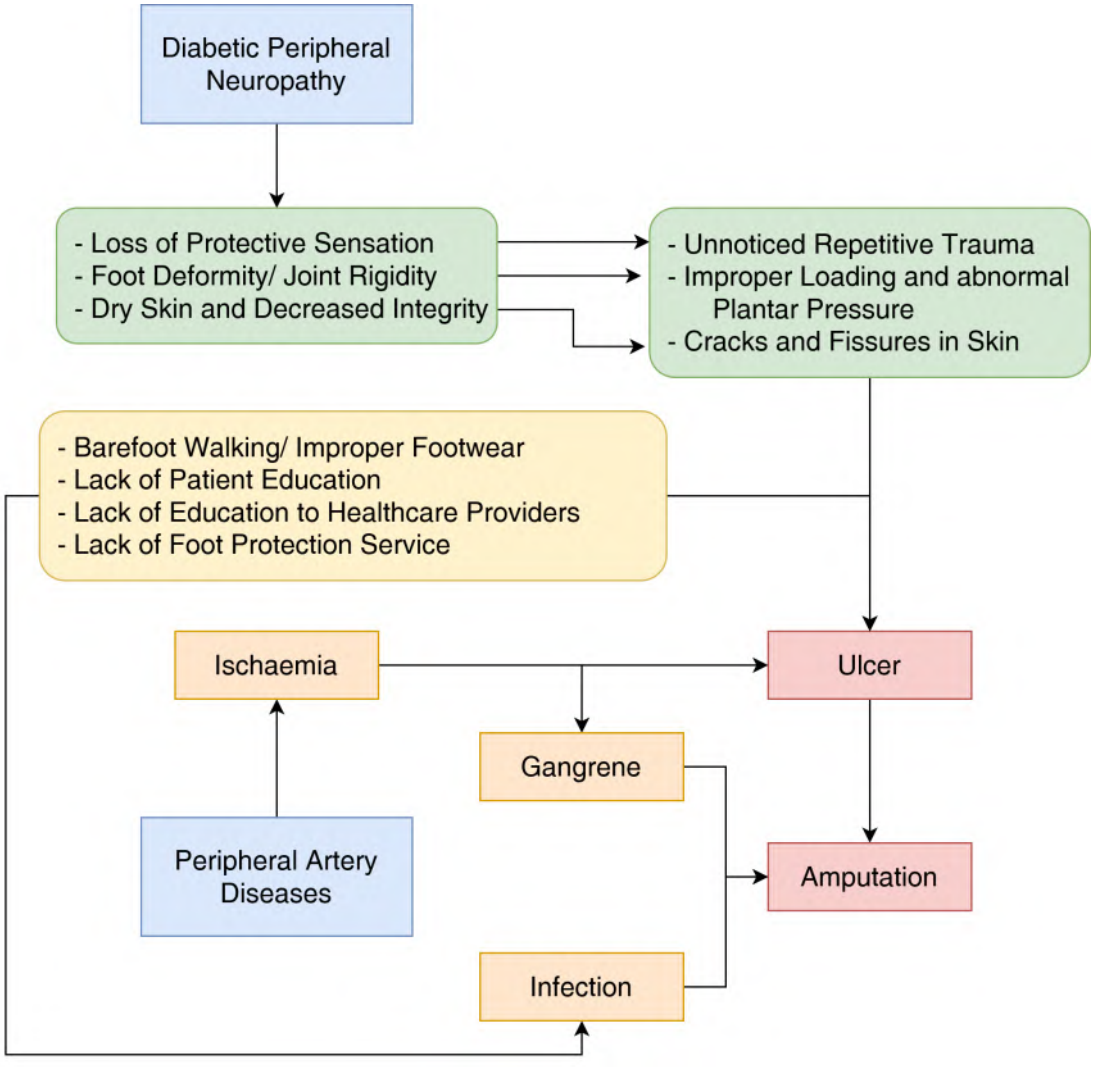

Figure 2.2: Etiology of Diabetic Foot Ulceration. Image adapted from Mishra et al. [10]

As it is evident from the Figure 2.2, DPN and structural deformities are closely related and both together provoke abnormal pressure distributions in the foot plantar. In fact, neuropathy is a main cause for structural deformities associated with the diabetic foot syndrome. Therefore, the scope of the present study is limited to the complications that arise due to DPN and PAD.

2.2.1 Diabetic Peripheral Neuropathy (DPN)

Diabetic Peripheral Neuropathy can be identified as a pathology that arises when the peripheral nerves (of the lower foot extremities) are disrupted or ceased as a result of longstanding hyperglycemia [24–26]. Thus, DPN manifests a Loss Of Protective Sensation (LOPS), dysfunction of the muscles and in addition anhidrosis in the lower extremities of a diabetic foot [25, 26]. Figure 2.3 demonstrates the difference between a damaged peripheral neuron and a healthy peripheral neuron, and how damage to such a nerve leads to DPN and related complications.

Longstanding hyperglycemia promote impaired regulation of various metabolic pathways, excessive release of byproducts such as cytokines and Kinase C proteins together with exaggerated oxidation stress which ultimately result in hypoxic nerve damage to sensory, motor as well as autonomic nerves of the foot plantar which is the primary surface of interaction with the surrounding environment during locomotion [17, 26]. These neurological complications pave way to callus formation, alteration of gait and posture of the diabetic patient leading to uneven distribution of pressure on the foot plantar [17, 24–26, 28].

DPN manifest in diabetic feet in one of three ways; sensory neuropathy, motor neuropathy and autonomic neuropathy [4, 29]. Sensory neuropathy is the first stage of DPN where sensory neurons in the foot get damaged and preliminary symptoms of LOPS starts to appear in the diabetic feet. If proper intervention and glycemic control is not undertaken, it can progress into motor neuropathy which weaken the motor neurons of the foot causing foot deformities. Motor neuropathy can develop into

autonomic neuropathy where autonomic neurons which control involuntary bodily functions (heart beat, blood pressure regulation, digestion, respiration etc.) are damaged promoting irregular cutaneous blood flow, sweating and skin alterations such as the formation of callous [4, 10, 26].

2.2.2 Peripheral Artery Diseases (PAD)

Peripheral Artery Diseases, also known as "Atherosclerotic Occlusive Disease" is a disorder fostering partial or complete occlusion of peripheral arteries (especially of the lower foot extremities) due to fatty and plaque deposits along the inner linings of the walls of arteries, making them narrower, thus, hindering the flow of blood or even terminating circulation to the lower limbs completely [22, 30, 31]. This phenomenon is illustrated in detail in Figure 2.4.

This long term hyperglycemia induced PAD invoke tissue damage. Minor tissue

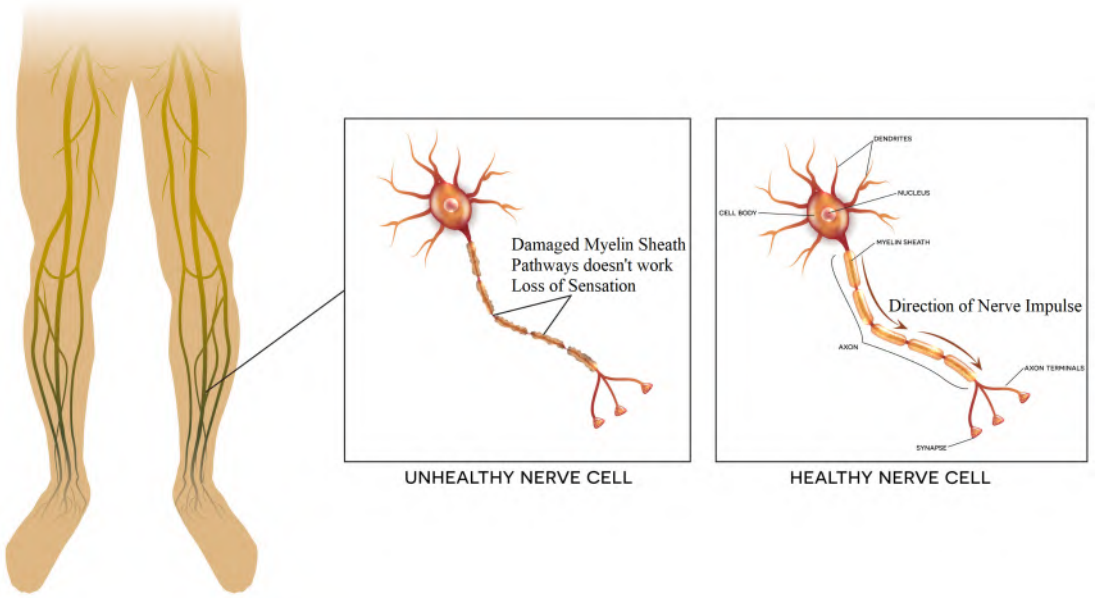

Figure 2.3: Sensory nerve fibers enclosed in myelin sheath transmit nerve impulses of different sensation (temperature, vibration, touch etc.) throughout the body. Long term hyperglycemia damage the myelin sheath thus transmission of sensory information is inhibited resulting in Diabetic Peripheral Neuropathy. Image Source: Duplantis [27]

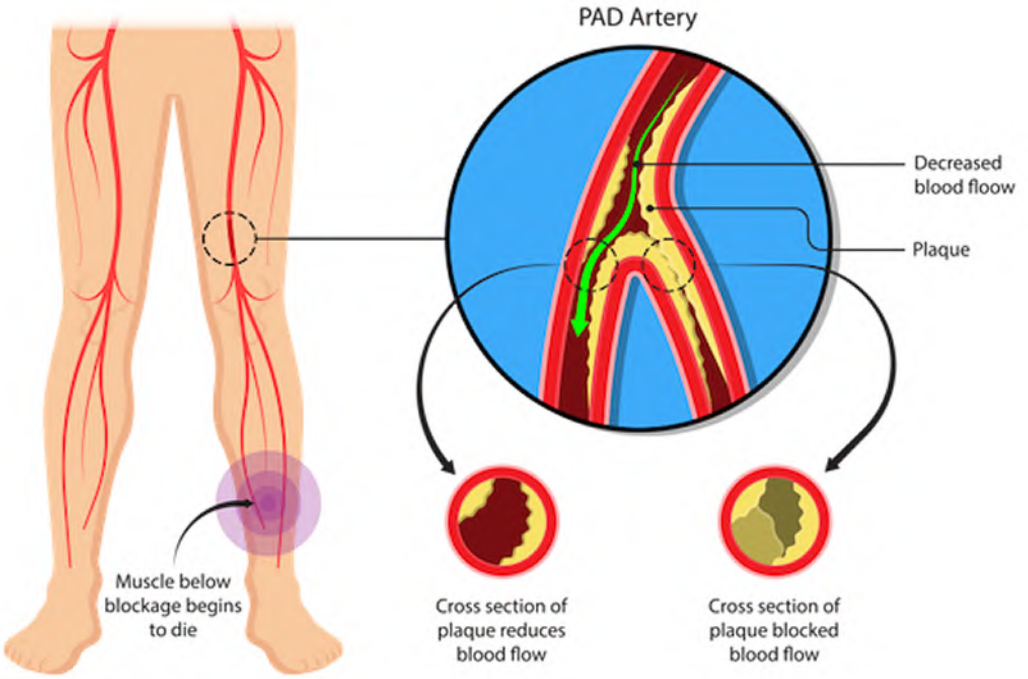

Figure 2.4: Fatty and plaque deposition result in Peripheral Artery Disease which narrows blood vessels causing reduced or termination of blood flow to the lower foot extremities. Image adapted from Cardiothoracic and Vascular Surgeons [32]

injuries during everyday locomotive activities are not healed properly due to the restriction of blood supply and disrupted tissue perfusion in the lower extremities [33]. This results in infections which subsequently results in inflammation in tissue structures [30, 31, 33, 34]. Inflammation of tissue structures in the foot plantar elevates temperature in those regions. [35, 36]. In addition, damage to the peripheral arteries as a result of PAD leads to the reduction in vasomotor functions reducing the temperature of localised regions the lower extremities [37–39].

2.3 Risk Assessment of Diabetic Feet

As highlighted in Section 1.3, regular feet examination is still the most easiest, cheapest and the most straightforward prevention strategy to combat diabetic foot complications and resulting amputations. Generally, risk assessment for DPN and PAD are conducted

separately through a distinct series of studies.

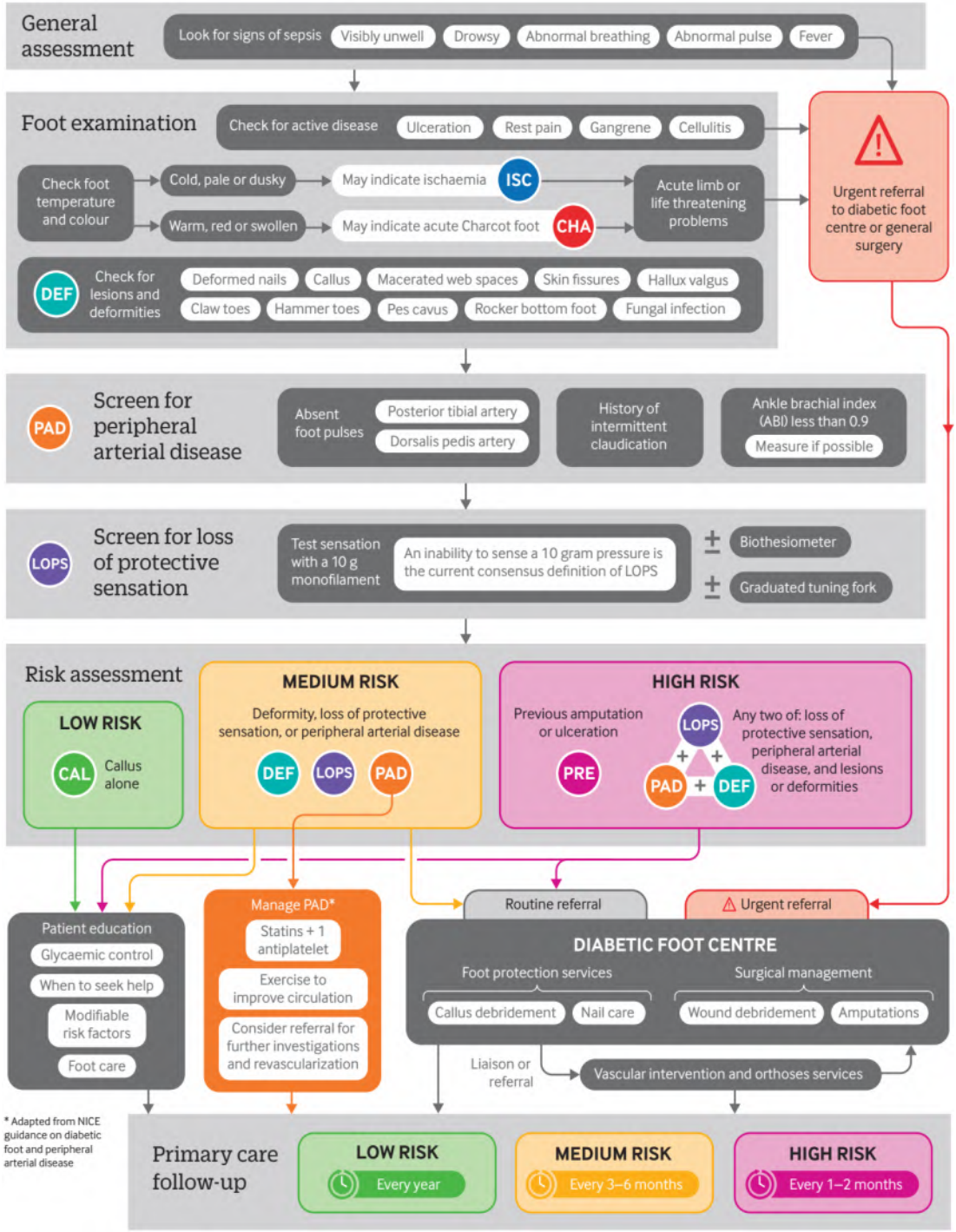

Figure 2.5: Complete Risk Assessment Process for Diabetic Foot Complications. Image adapted from Mishra et al. [10]

A detailed overview on the risk assessment process for diabetic foot complications is

shown in Figure 2.5. First a general assessment of the patient is conducted to diagnose whether he/she is exhibiting any response to infection. Then the patient is subjected to the initial foot assessment where visible signs of foot diseases and/or ulceration are identified inclusing lesions and deformities. Afterwards, the patient is subjected to a screening for DPN followed by a screening for PAD using techniques discussed in Sections 2.3.1 and 2.3.2 respectively. Upon concluding the screening process, the patient is assigned a risk category based on the susceptibility to foot complications. All at-risk patients, irrespective of their risk category, are educated about the disease and its complications while recommending them of proper management techniques, and frequency of routine clinical assessments.

2.3.1 Risk Assessment for Diabetic Peripheral Neuropathy

Accurate diagnosis of DPN involves investigating for symptoms through a detailed neurological patient history followed by physical examination and finally, electrophysiological testing for diagnosis and evaluating the severity [28, 40]. Patient history is recorded using a set of standard questionnaires. Physical examinations involve evaluating patient response for different sensations and quantify the sensitivity and specificity of neuropathy based on clinical scoring systems such as Neuropathy Impairment Score in the Lower Limbs (NIS-LL), Diabetic Neuropathy Examination (DNE) score, Toronto Clinical Scoring System (CSS) score, Leeds Assessment of Neuropathic Symptoms and Signs (LANSS), Douleur Neuropathique en 4 (DN4), Neuropa- thy Deficit Score (NDS) and Michigan Neuropathy Screening Instrument (MNSI) to name a few [28, 40].

There exist an abundance of clinical diagnosis techniques for DPN. Based on the nature of neurological assessment undertaken, they can be categorized as Nerve Conduction Studies (NCS), Quantitative Sensory Threshold tests (QST), morphological testing, autonomous nervous system testing, monofilament testing and Corneal confocal microscopy (CCM) ophthalmic imaging techniques [28, 40, 41].

2.3.1.1 NCV Measurements

NCV measurements, also known as Electroneurography, is a measure of the capability of peripheral nerves to conduct electrical impulses [40]. In essence, it measures the velocity (in ms^{-1}) with which an electrical impulse conducts though a peripheral nerve of concern via surface electrodes and quantify the motor amplitude (in mV) and sensory amplitude (in μV) of them [28, 42]. Inability to meet the expected threshold measurements is a direct indication of pathology in axons, nodes of Ranvier or myelin on the peripheral nerve concerned [40]. Therefore, existence, degree of spread and extremity of PAD can be diagnosed. As a result, NCS serve as the gold standard for diagnosis of DPN [40, 43]. Process of conducting a NCS is depicted in Figure 2.6. Furthermore, there are assessment techniques such as muscle response testing which is a combination of electromyography (EMG) and NCS that provide improved diagnosis of PAD [44].

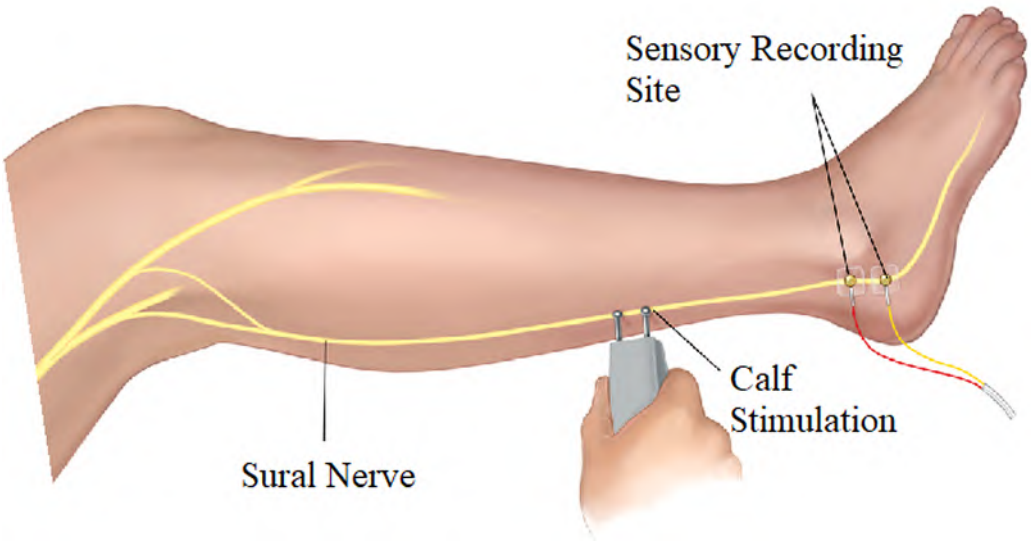

Figure 2.6: Process of conducting Nerve Conduction Velocity (NCV) testing of the Sural nerve of the leg. Stimulating electrodes are placed over the nerve and recording electrodes are placed over the muscle. A Low-level electrical signal is applied from the stimulating electrode and are received by the recording electrodes. A wave monitor is used to visualize the impulses. Image adaptation Hopkins [42]

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2.3.1.2 QST Tests

Meanwhile, QST tests provide a quantitative measurement of sensation about the sensory function of the peripheral arteries. Numerous QST tests are being carried out clinically that measure thermal, vibration and current perception thresholds (example: alternating current perception threshold test) [40, 44].

2.3.1.3 Alternating CPT Tests

Alternating CPT assess the severity of the condition by delivering a set of sinusoidal electrical impulses in a range of frequencies at varied current intensities to detect the presence or absence of stimuli [44, 45]. It takes approximately 45 minutes to 1 hour to complete the procedures and is extremely time consuming when evaluating the entire foot plantar of a diabetes patient.

2.3.1.4 Monofilament Tests

Monofilament testing, on the other hand, is an affordable and portable procedure that qualitatively assess LOPS through bulking stress of a calibrated single fibre nylon thread [41]. The major limitation in both QST testing and monofilament testing are that they are psychophysical exams. Hence, the accuracy of these tests are extensively dependent upon the patient feedback.

2.3.1.5 Morphological Assessments

Morphological assessments include nerve biopsy tests from suspected peripheral nerves. Due to the invasive nature, pain and susceptibility to infection, this technique suffers from diagnostic shortcomings [40]. Autonomic nervous system testing include orthostatic blood pressure measurement, orthostatic heart rate measurement and R–R variability measurement during deep inhalation and exhalation on a ECG exam [40].

2.3.1.6 CCM Imaging Technique

CCM which is an ophthalmic imaging technique of the cornea has gradually risen to fame as one of the most advanced diagnostic tools available for DPN diagnosis [28], upon the breakthrough studies by Rosenberg et al. [46] and Malik et al. [47] who discovered the deterioration of the sub-basal nerve fibers of the cornea among patients with DPN. However, the critical limitation in CCM is the acquisition of high resolution, high quality images reproducible images of the nerve fibers in cornea [48].

2.3.2 Risk Assessment for Peripheral Artery Diseases

With the gradual increase in prevalence of diabetes and related foot complications, multitude of different risk assessment methodologies for PAD have been adopted [22, 31]. However, the most formidable challenge in early diagnosis is that majority of patients are asymptomatic [31, 49]. Nonetheless, intermittent claudication (Section 2.2.2) is one of the most prominent symptoms of peripheral artery disease, among symptomatic patients. Therefore, tests conducted to identify the presence of claudication ranks as one of the primary diagnostic techniques for PAD [31, 35, 50]. In addition, checking for the absence of peripheral pulses is also a widely utilized diagnostic technique for PAD [35, 50].

The major drawback of the two methods is that they suffer from insensitivity, inter-observer reproducibility and the inability to quantify the measurements [22, 35]. Moreover, claudication inflicts a substantial pain on the patient feet during motion as discussed in Section 2.2.2. However, DPN is associated with impaired sensory feedback, therefore, the inflicted pain due to claudication could be suppressed in the presence of DPN [33–35].

2.3.2.1 ABI Tests

Ankle-brachial index (ABI) tests, which are both validated and reproducible are highly popular assessment technique [33–35]. ABI is calculated by measuring the systolic blood pressure of dorsalis pedis and posterior tibial arteries in ankles and brachial artery of the arm sequentially using a hand-held Doppler ultrasound machine together with a sphygmomanometer and calculating the ratio [2, 22, 35] as shown in Figure 2.7.

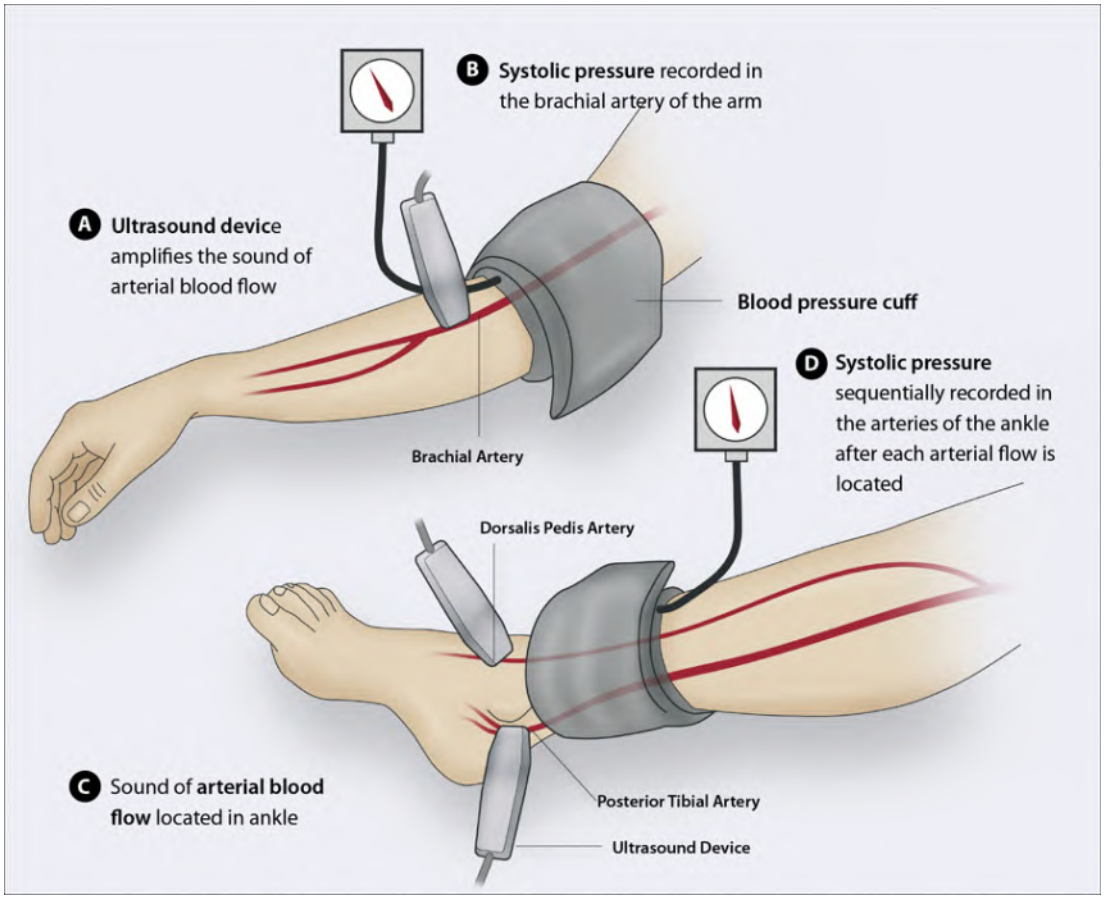


Figure 2.7: The sequential process of measuring the ankle systolic pressure and brachial systolic pressure using a sphygmomanometer and a Doppler ultrasound to calculate the ABI ratio to diagnose peripheral artery disease. Sphygmomanometer is used to measure blood pressure whereas the Doppler ultrasound is used to detect pulses [30]. Image adaptation from Best Practice Advocacy Centre New Zealand (bpac^{nz}) [51]

However, ABI tests also accompany several limitations. The diagnosing ability decline drastically when PAD complications are present distal to the ankle [30]. Besides, the measurement process is fairly time consuming and requires expensive equipment and expertise.

2.3.2.2 TBI Tests

Toe-brachial index (TBI) is also calculated together with ABI and diagnosis have proven to improve significantly [22, 30]. If TBI ratio is less than 0.75, it is highly suggestive of PAD [22, 52]. However, both ABI and TBI tests are dependant on the patient height, age, weight, gender and race [30, 35].

2.3.2.3 Other Miscellaneous Techniques

In addition to ABI and TBI tests several other clinical diagnostic techniques exit for diagnosing PADs complications such as transcutaneous oxygen pressure measurements, hyperspectral imaging and skin perfusion pressure measurement [22, 50]. These measurement generally determine the perfusion potential of the foot [22, 30]. Brownrigg et al. [22] states that computed tomography (CT), magnetic resonance imaging (MRI) and digital subtraction angiography tests are also being carried out to extract anatomical information with regard to distribution and severity of PAD. However, those imaging techniques can not be used for diagnosis of PAD.

Liquid Crystal Thermography (LCT) has also been experimented with, as a risk assessment technique for PAD [14, 44, 53]. Large hysteresis, low resolution and accuracy of measurement, risk of contamination and several other factors associated with LCT, has substantially hindered its further developments and progression [54].

2.3.3 Concluding Remarks of DPN and PAD Diagnostic Techniques

The conventional diagnostic tools for DPN are generally time-consuming, expensive, insensitive, not inter-observer reproducible and some does not provide a confirmatory diagnosis [22, 28, 40]. In addition, they are not suitable for routine examinations as a screening tool and their measurements are greatly influenced by the foot temperature [43]. In a routine diabetic clinic, screening a multitude of patients within a short interval of time with minimum number of accessories mounted on the patient is preferred. Besides, DPN and PAD complications manifest simultaneously on most patients, thus, hindering a proper assessment of the feet. Hence, a simple, easy-to-use screening tool for DPN and associated foot complications offers a significant clinical advantage [43].

All the conventional diagnostic tools for PAD are also time-consuming, expensive, insensitive, not inter-observer reproducible, may not provide a confirmatory diagnosis and requires sound technical competency [22, 28, 40].

As in the case with traditional DPN assessment techniques, these are not suitable for routine examinations, as screening a multitude of patients within a short interval of time with minimum number of accessories mounted on the patient is unattainable. ABI tests (sometimes ABI + TBI tests) which are considered to be the gold standard for PAD diagnosis generate false elevated values due to secondary complications of diabetes such as DPN, renal dysfunction etc. [55, 56]. Therefore, a simple, easy-to-use screening tool for PAD and associated foot complications could provide a significant clinical advantage [56].

CHAPTER 3

Plantar Pressure Measurement

3.1 Risk Assessment of the Diabetic Foot Plantar using Pressure Measurements

The relationship between foot plantar pressure and DPN has sparked significant scientific interest in recent years [43]. Frykberg et al. [57] demonstrated that DPN patients often have increased foot plantar pressure, meanwhile, Caselli et al. [58] demonstrated that DPN patients experience a shift in Center of Pressure (COP) of the foot as the resultant pressure is shifted more towards forefoot from rear foot. Likewise, Lee et al. [59] showed that patients with mild DPN exhibit asymmetric weight bearing and plantar pressure during both standing and walking. Further, Greenman et al. [60] discovered that small muscle atrophy (loss of muscle tissue) in lower limb muscles is prevalent among diabetes patients with DPN and it could be detected through plantar pressure variations even before the standard DPN diagnostic tools. Furthermore, several past studies have ascertained that foot pressures greater or equal than 6 kg/cm^2 are associated with patients who are at high risk of getting diabetes related foot complications that lead to ulceration [32, 61, 62]. It is worthy to note that the foot plantar pressure is conventionally expressed in kg/cm^2 rather than kPa for the convenience of the medical practitioners at their request [63, 64].

Accordingly, foot plantar pressure measurement is a formidable, easy to use,

inexpensive measurement process, that requires minimum technological proficiency and is indicative of DPN related diabetic foot complications. The traditional DPN measurement techniques discussed in Section 2.3.1 is cumbersome to be used as screening tools due to their long set up times, not providing an overall picture of the entire foot plantar, dependence of foot temperature etc. discussed in Section 2.3.3. Therefore, foot plantar pressure assessment tools has risen to fame as an alternative approach that is most suitable screening tool for routine clinical assessment for DPN related diabetic foot complications and subsequent ulcerations [43, 58–60].

3.1.1 Current Plantar Pressure Monitoring Techniques

In Section 2.1, it was distinguished that pressure component we are concerned with is from the resultant ground reaction force acting between the foot and the support surface. Ground reaction force can be decomposed into three perpendicular components acting on a foot during locomotion as shown in the Figure 3.1.

Measurement of foot plantar pressure can be done under two conditions, static conditions and dynamic conditions. Static conditions involves measurement of plantar pressure when a patient is standing freely in an upright position on the measurement surface without any motion. Although, static measurements provide insight into diabetic foot complications of the patient, dynamic measurements provide further insights into the pressure distribution of the feet during their main function of locomotion [65]. Despite the measurement condition, static or dynamic, the plantar pressure measurement mechanisms can measure only the vertical force component of the ground reaction force at a given moment [17].

3.1.2 Other Applications of Plantar Pressure Measurement

Apart from detecting diabetic foot complications, measurement of foot plantar pressure has multiple applications. Plantar pressure measurements are extensively

used in designing of footwear [66, 67]. Realistic loading of the foot plantar during locomotion, response of the insole materials to stress are identified through plantar pressure measurements. Designing of special custom footwear for diabetic patients is also a growing field that uses foot plantar pressure measurements.

Athletes, sportsman and sportswoman whose feet endure comparatively high stresses due to various high intensity loading conditions are frequently examined to identify most reliable techniques that enhance performance and also to prevent injuries [68]. For example, Kersting and Gurney [69] analysed effective golf swings that maximize the output while reducing the risk of injury.

Scaphoid and longitudinal arch pads which are widely used in rehabilitation of deformities in the foot and ankles are developed after a thorough analysis of the foot plantar pressure [70]. In addition, several studies are reported in literature that uses plantar pressure assessment for developing rehabilitation interventions for cerebral palsy [71].

Moreover, several balance control studies [72], posture control studies [73] and biometric studies [74, 75] have copiously relied upon plantar pressure as the underpinning measurement.

3.1.3 Types of Plantar Pressure Measurement Techniques

There are many varieties of instruments to conduct plantar pressure measurements and they may employ either discrete set of sensors or a two dimensional (2D) array of sensors [76]. Although many classifications exist, plantar pressure measurement systems are typically available as platform systems and as in-shoe systems [77, 78].

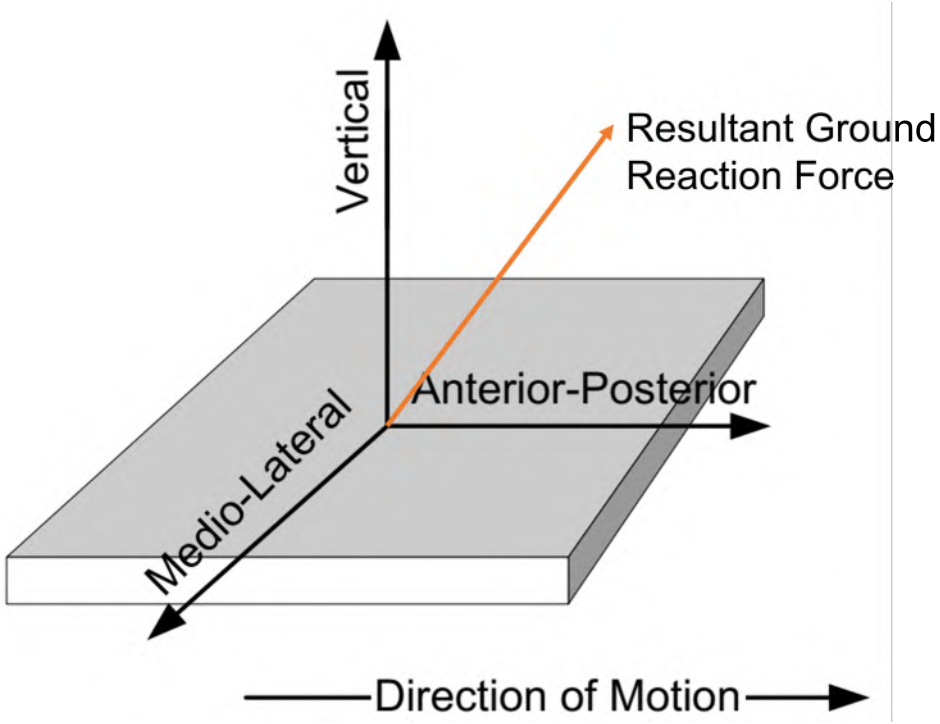


Figure 3.1: Three components of the resultant ground reaction forces acting on the foot by the support surface during locomotion. The vertical reaction force acts perpendicular to the support surface. Anterior-Posterior force component and Medio-Lateral force component are horizontal frictional forces. Image adapted from Billing [79]

3.1.3.1 Platform Systems

Platform systems are a collection of robust and rigid set of flat pressure sensors arranged in the form of a matrix (2D array) preferably embedded on the floor which facilitate natural gait allowing both static and dynamic measurements [77]. Generally, these systems have improved spatial resolution (number of sensors per unit area) compared to in-shoe systems enabling a complete measurement of pressure distribution in the foot plantar. Therefore, a more realistic estimation of the distribution of plantar pressure (a pedobarogram) of one or both feet is attainable, through a platform system making it a more appropriate screening tool over in-shoe systems.

A comprehensive review of literature suggests that there exist four main categories of platform based pedobarographic data acquisition systems based on measurement technologies as listed below [64].

1. Barefoot Measurements
2. Cumulative Techniques
3. Optical Pedobarogrpahy
4. Electromechanical Pedobarography

Barefoot Measurements

Barefoot measurements of plantar pressure involves obtaining a pressure profile of one foot plantar when a subject walks on top of a pressure plate during normal gait [64] as shown in Figure 3.2. The barefoot measurement technique is relatively an outdated approach that has hardly being reported in recent literature. Besides, it does not permit evaluation of pressure distribution of the entire feet, nor does it allow measurement of pressure under static conditions. In essence, it simply allow measurement of parameters such as center of pressure.

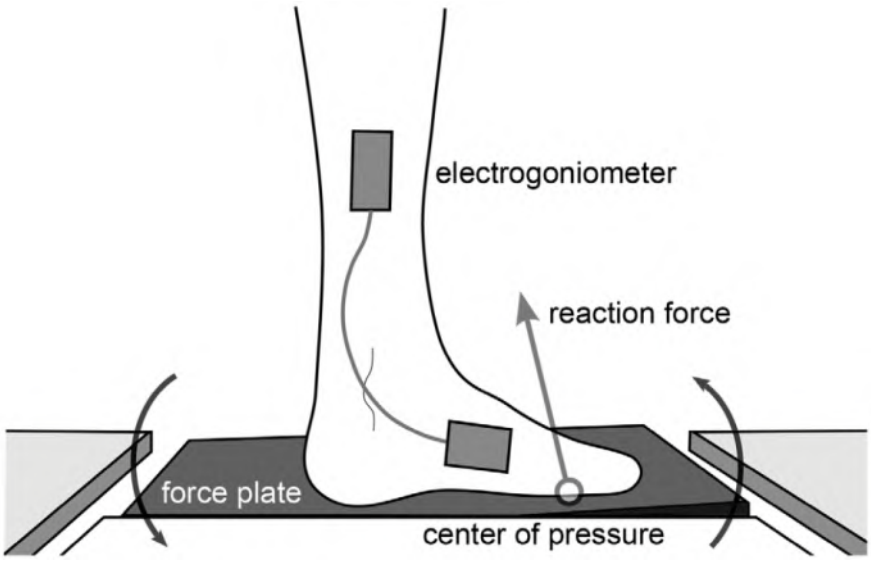


Figure 3.2: Working principle of barefoot plantar pressure measurement via a pressure plate.Source: Gregg et al. [80]

Cumulative Techniques

Cumulative techniques involve deducing peak plantar pressure experienced by specific anatomical location (such as heel, meta-tarsals) of the foot plantar by capturing the foot print using shape changing rubber mats, dry-filled microcapsules or permanently distorting aluminum foils [64]. Advent of in-shoe plantar pressure measurement techniques have prompted cumulative techniques out of use in plantar pressure measurement applications.

Optical Pedobarography

Optical Pedobarography techniques generally involves a glass plate which is illuminated on its edges by a light source (an LED strip), covered by a soft acrylic plate which gets pressed onto a glass plate underneath when a patient stands on it [81]. This slight distortion disturbs the light rays which are otherwise totally internal reflected by the glass plate making them scatter throughout [75]. These light beams are captured by a mirror and a Charge Coupled Device (CCD) camera set-up and transformed into a pedobarographic image as illustrated in Figure 3.3.

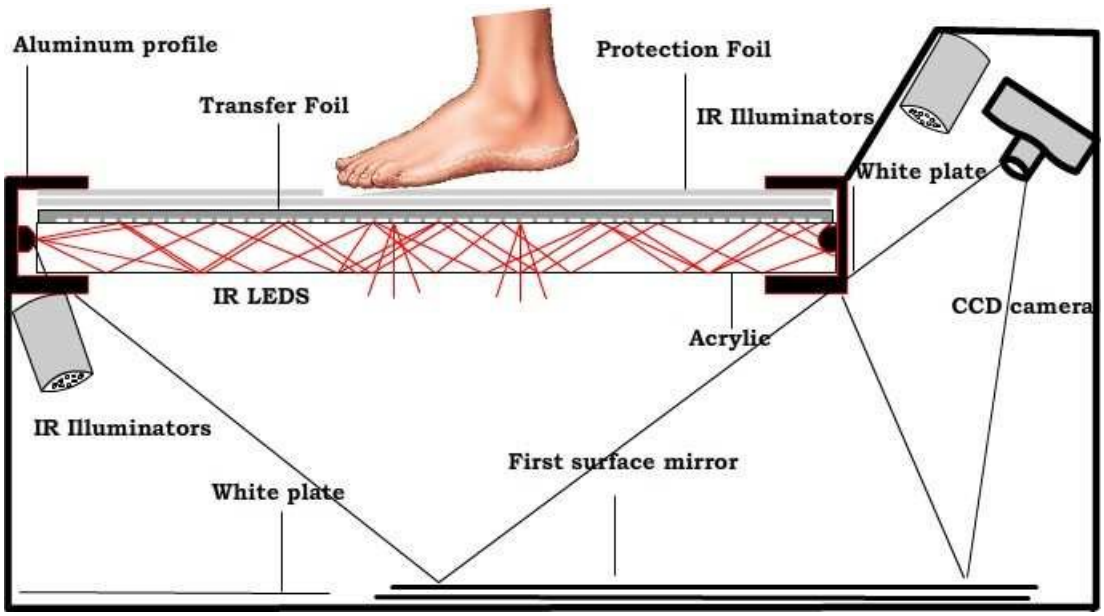


Figure 3.3: Main Components of an Optical Podoscope. Source: Crisan et al. [82]

The major limitations of optical pedobarography techniques are that the measurement accuracy depends significantly on the stability of the LED light intensity [75], they can measure only a limited number of walking steps (a full dynamic analysis is difficult) [75] and they are comparatively expensive and difficult to implement [75, 81] because of the camera requirement and the precise angles the cameras needs to be placed.

Electromechanical Pedobarography

Electromechanical systems on the other hand generate an electrical output in response to a mechanical input to its sensors. In the case of plantar pressure measurement systems this mechanical input is the pressure exerted by the soles of the feet on the supporting surface. Generally, pressure exerted induces a change in electrical properties of the sensor material, thus generating an electrical response which could be filtered, digitized and represented as a pedobarographic image. Some the electromechanical techniques used in pedobarographic measurements are segmented and matrix force plates, capacitance mats, piezoelectric and piezoresistive sensor plates and force sensitive resistor arrays [64, 81]. Moreover, these systems inherit several striking features such as fast response time, low hysteresis, high precision and reproducibility of measurements over other platform systems.

Figure 3.4: Electromechanical pedobarographic assessment tool for plantar pressure measurement developed by emed® [83]

3.1.3.2 In-shoe Systems

In-shoe systems are instrumented footwear which are equipped with flexible and robust sensors placed at specific target locations on the insoles [78, 84, 85] as shown in Figure 3.5 (a). They allow obtaining vital information regarding center of pressure, peak pressure, mean pressure of the heel, toes, hallux, medial of the foot and meta-tarsals (1^{st}, 3^{rd}, 5^{th} etc.) [86] which are highly susceptible to foot complications due to comparatively excessive loading.

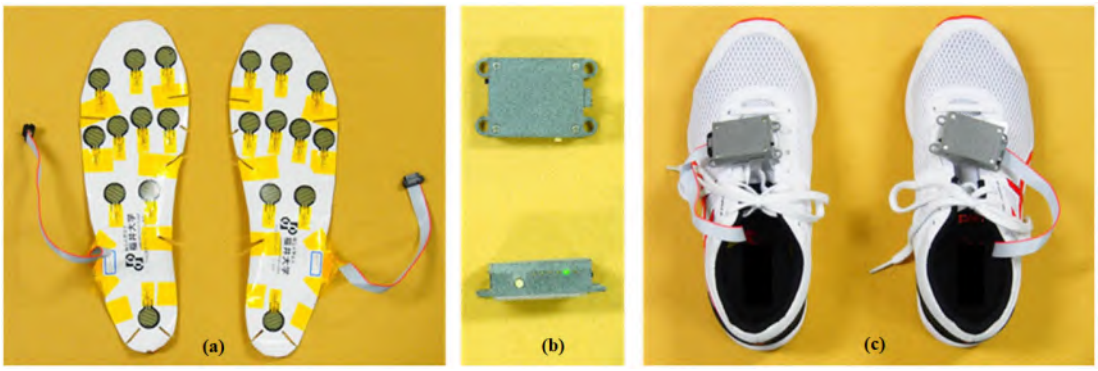


Figure 3.5: In-shoe plantar pressure measurement system developed by Yamamoto et al. [85]. **(a)** Arrangement of sensors at target locations in the shoe insole **(b)** The data acquisition device **(c)** The instrumented shoe the insoles are placed and worn by the subject

The main advantage of in-shoe plantar pressure measurement is the portability, which allows the subject to wear it for a prolonged duration and distribution of pressure over a course of a specific time period can be measured [87]. The recent developments of in-shoe systems adopt wireless data acquisition technologies and use of comparatively less power [85].

On account of lower implementation time, cost, complexity and the ability to record data over extended periods of time, several commercial in-shoe plantar pressure measurement systems such as F-Scan®, Pedar®, Moticon®, ParoTec®, Sensor Medica® etc. made of inertial sensors (accelerometers) and gyroscopes are being used in the industry [84] for balance analysis [88], spatiotemporal gait analysis [89],

evaluating structural deformities [90] and many other applications.

However, in in-shoe systems, the limited number of sensors used compared to platform systems generate low spatial resolution pedobarogram of the foot plantar pressure. According to Razak et al. [77], there are a substantial number of reported cases in literature about the tendency for sensor slippage causing errors in measurements.

3.1.4 Platform Systems Vs In-shoe Systems as a Screening Tool for Routine Clinical Assessments of DPN

The key differences between platform based plantar pressure measurement systems and in-shoe based plantar pressure measurement systems are summarized in Table 3.1.

Table 3.1: Comparision between Platform-based and In-shoe based plantar pressure measurement systems

Platform System	**In-shoe System**
Large array of sensors	Few sensors placed at specific locations
High spatial resolution	Low spatial resolution
Pressure distribution can be obtained	Pressure at specific locations can be measured
Can isolate localized foot complications	Can not isolate localized foot complications
Need not be patient specific	Custom designed to cater to patient feet dimensions
Screen large no. of patients in a small time period	Scan same patient over a long time period

Low spatial resolution owing to the limited number of sensors being present, is the major drawback of in-shoe systems compared to platform systems with regard to plantar pressure measurement as a routine clinical assessment tool in a diabetic clinic. As screening a large number of patients within a short duration of time to make a

distinguish vulnerable feet for diabetic foot complications is the primary objective of such an institute, in-shoe system which is precisely a patient centered measurement system diminish its value. Through an in-shoe system a complete overview of the feet will not be attained, but specific information on pre-selected locations on the foot plantar. Hence, it may be used to obtain a confirmation on a previously diagnosed foot complication, rather detecting new complications unless the sensor is placed below the exact spot of concern.

Improved sensor area in platform systems, on the other hand, ensure data acquisition with greater spatial resolution to isolate localized complications as well as obtain a detailed overview of both feet. Presence of durable sensors with restricted provisions for sensor slippage while facilitating natural gait under both static and dynamic conditions transcend platform systems as the most pertinent configuration for intended application.

Consequently, for these reasons, in-shoe measurement is ill-suited as a screening tool for routine clinical assessment of feet to detect DPN and PAD manifested foot complications as advocated by the IWGDF guidelines [2].

3.2 Sensors Used in Plantar Pressure Measurement Applications

A wide range of sensors have been reported in literature and available in commercial space where different material properties have been utilized to generate a quantifiable output voltage proportional to pressure exerted on them.

3.2.1 Capacitive Sensors

These comprise of a dielectric material such as rubber placed in between two flexible electrodes (elastomers). Upon comprehensive loading, capacitance of the sensor changes due to the reduction in the distance between two electrodes and due to the shape alternation of the dielectric material [90] (According to the equation for Capacitance $C = \varepsilon(A/d)$). However, Oballe-Peinado et al. [91] reports that sensor arrays fabricated with capacitive sensors are prone to RC crosstalk too.

3.2.2 Strain Gauge Sensors

Strain gauges consist of a thin conductive foil placed under an insulated substrate which undergoes deformation under mechanical loading. The deformation result in the change in resistance of the conductive foils [90].

3.2.3 Piezoresistive Sensors

Piezoresistivity is the ability of a material to alter its electrical resistance when subjected to mechanical stress. These sensors, also referred to as Force Sensing Resistor (FSR) sensors [93], are manufactured by placing a conductive film and a insulting spacer in between two substrate layers with a conductive print on it as shown in Figure 3.6. Under mechanical loading, the sensor undergo deformation, increasing the contact between the conductive film and the substrate layers inadvertently increasing conductivity between the substrate layers (reduction in resistivity) [92]. Upon removal of the load, the conductive film regains its former shape, decreasing the conductivity.

Based on the final cost of implantation, sensor characteristics, dimensions required for static and dynamic analysis, susceptibility to external interference and individual sensor power requirement, a piezoresistive sensor array based platform system

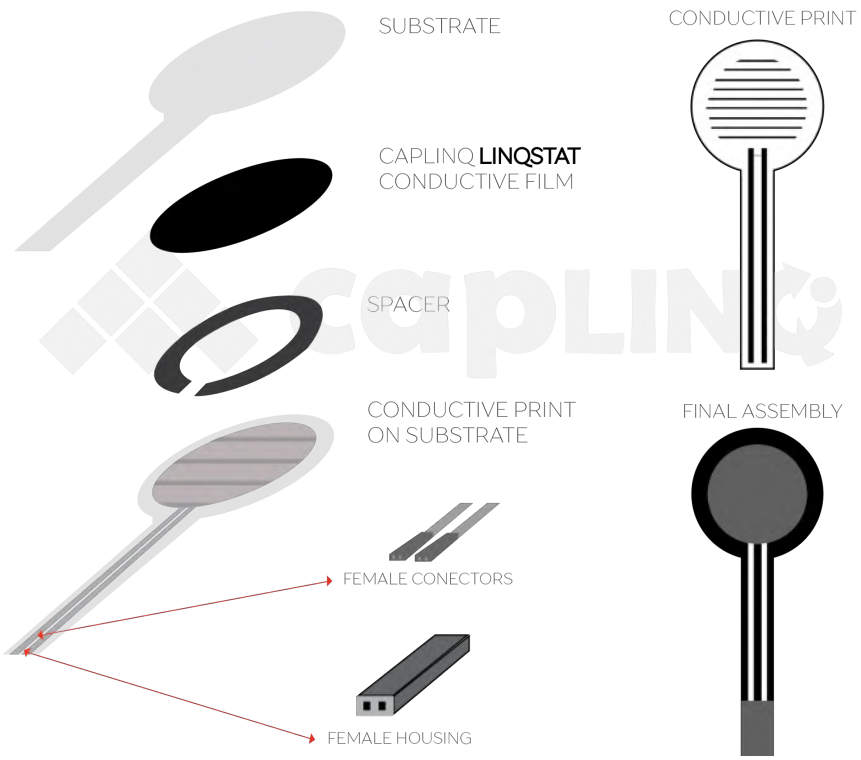


Figure 3.6: Composition of a Force Sensing Resistor type sensor. Image adapted from CAPLINQ [92]

appears to be the most formidable implementation [93–95] for the current application of routine clinical assessment of diabetic foot plantar.

3.3 Fabrication of the Sensor Array Used in Platform Systems

Platform systems are customarily a collection of individual sensors deployed at a certain geometry with a spatial resolution in millimeters (mm) [93] which are being used to procure an overall visualization of foot plantar as discussed in Section 3.1.3.1. Thus, individual sensors (either capacitive, strain gauge or FSR sensors) are interconnected together forming a network of two dimensional array as shown in Figure 3.7.

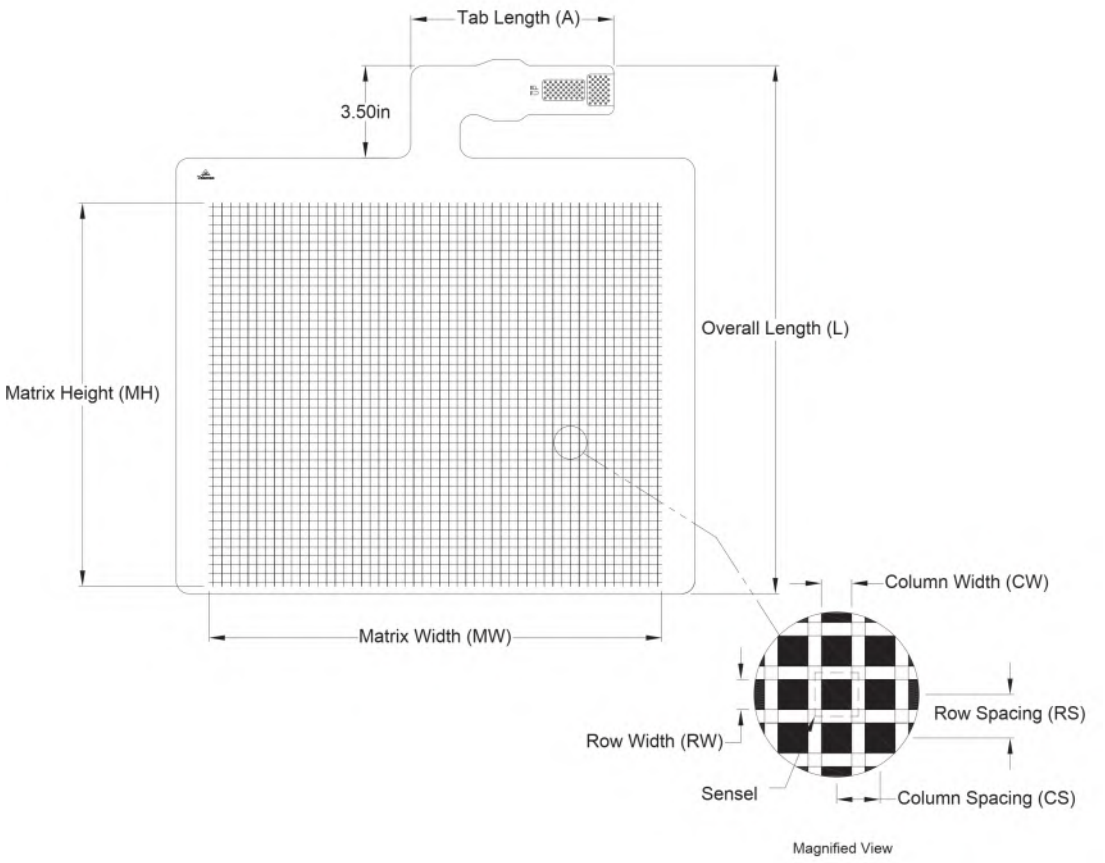


Figure 3.7: Platform based 2D sensor array formed by interconnecting 2288×2288 FSR (piezoresistive) sensor elements (sensels) Source: Tekscan® [96]

A piezoresistive sensor array can be fabricated by positioning a conductive polymer between two substrates with conductive film grids printed on the inner surface which are separated by a thin spacer as shown in Figure 3.8. When pressed, the conductive polymer short circuits the two conductive substrate layers which pass an electric current across it. The voltage drop across two conductive substrate layers are indirectly proportional to the resistivity across the polymer, which vary depending upon the intensity of the applied pressure (a property of piezoresistive materials) [93]. Castellanos-Ramos et al. [95] have verified that conductive polymer sheets fabricated with a conductive ink as the substrate are more efficient, reliable and accurate than other types of large sensor arrays.

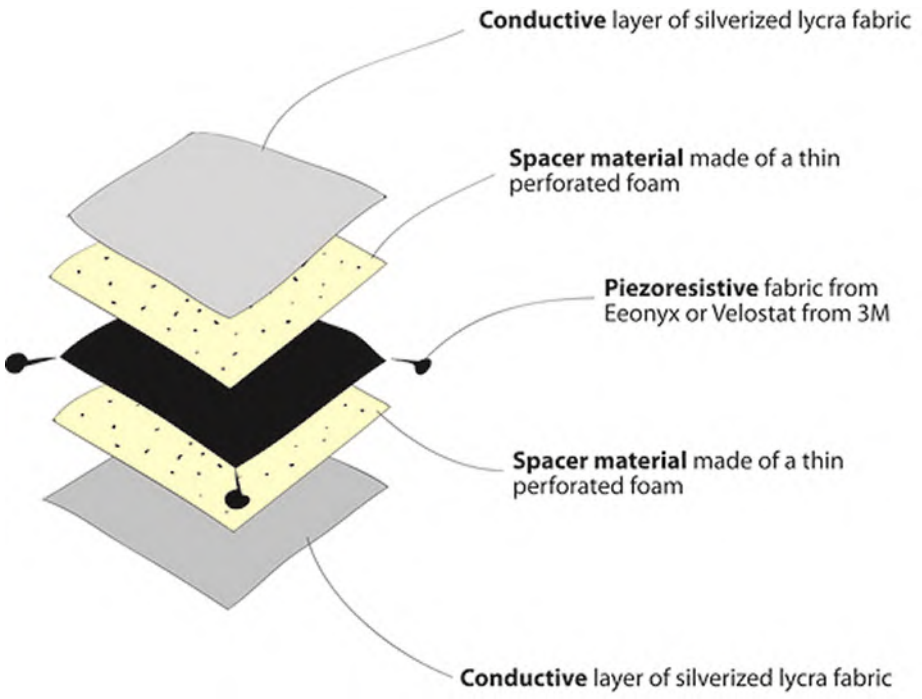


Figure 3.8: Composition of a piezoresistive conductive ploymer sheet. Image source Kobakant [97]

3.4 Crosstalk Interference

3.4.1 Interconnect Complexity

Incorporating a large number of sensors into a sensor array results in an increased number of interconnections within the array as each sensor has a minimum of two interconnects. A conventional method of measurement involves $M \times N + 1$ interconnections and wires to scan a sensor array of $M \times N$ sensels [98]. This results in a prolonged duration to completely scan the array and for an extensive wiring requirement [99]. This phenomenon is referred to as the "Interconnect Complexity" [100, 101]. As a solution, these sensors are often organized into arrays of shared row-column architecture, where each sensor is connected to a shared row and a shared column at either end as shown in Figure 3.9. The shared row-column architecture reduces the interconnections in a M×N sensor array drastically down to

M+N. By supplying a voltage to a given row and reading a specific column, all the sensel in the array could be individually accessed. Therefore, this reduces the interconnect complexity, while elevating the scanning rate significantly [99].

3.4.2 Effect of Crosstalk

In the shared row-column architecture, the reduction in interconnection complexity of sensor array networks is achieved at the expense of an undesirable phenomenon known as the "Crosstalk Interference". Crosstalk materializes due to the interconnect overloading where one node (interconnection) is often shared among many sensels due to the shared row-column architecture. Therefore, multiple sensels which are electrically connected to the same node may induce undesirable potentials (voltage drops) at that node. The reason for this is the momentary formation of parasitic parallel paths [102] (as shown in Figure 3.10), when attempting to read the voltage of a given sensel connected to that node. Momentary formation of parasitic parallel paths results in unintended current flow (bypass currents) through unintended paths contributing to overloading of the interconnect of concern (interconnect overloading) while promoting the "spread of information" [99]. Since we measure the resistance across a given sensel incidentally through the voltage drop across it, bypass currents alters the voltage drop across the measured sensel. Figure 3.10(a) demonstrate the parasitic parallel path formation during sensel readout through an operational amplifier. Note that electronics used in these array readout circuits are discussed extensively in Section 3.5.

Nonetheless, crosstalk has been one of the major drawbacks of incorporating piezoresistive sensor arrays in a diverse set of applications including plantar pressure measurement [93, 94, 103]. To date, there exist no ideal solution to combat crosstalk, yet studies have been carried out to determine various workarounds to mitigate the effect of crosstalk.

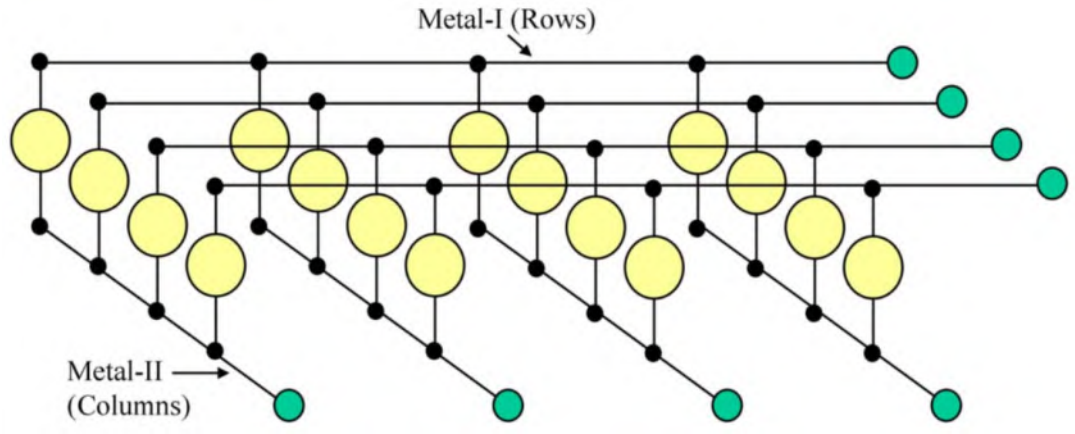


Figure 3.9: The row-column architecture employed in the development of platform based plantar pressure measurement systems to reduce interconnect complexity. Image adapted from Saxena et al. [99]

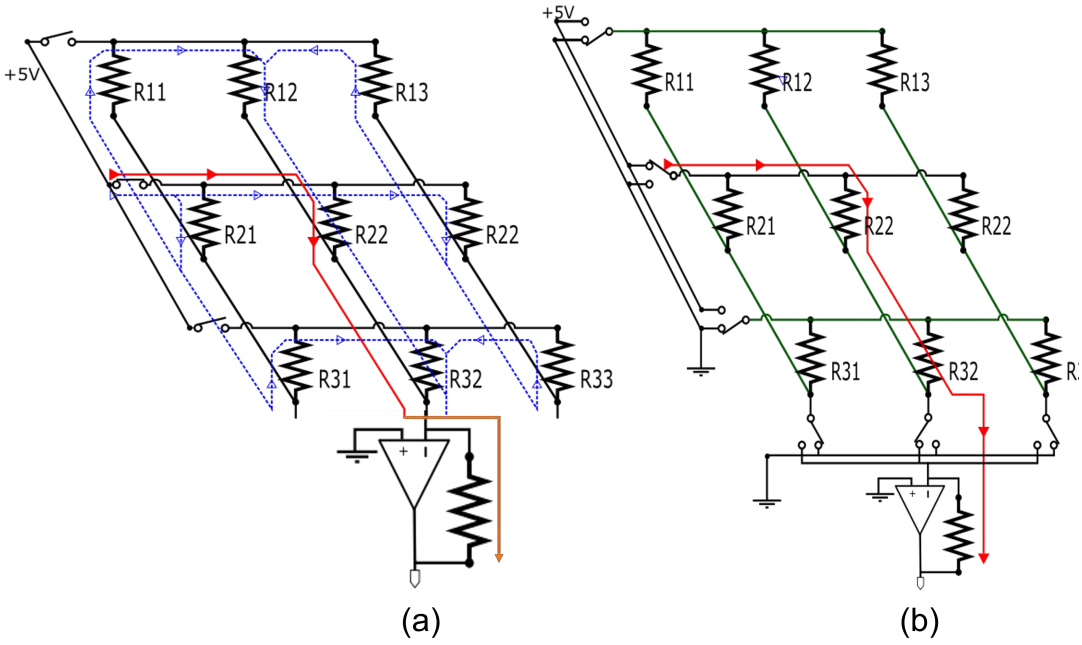


Figure 3.10: Illustration of crosstalk interference through a 3×3 resistor array network (a) Parasitic parallel paths (blue) develop across the 3×3 2D resistor sensor array when attempting to read the voltage across the sensel R_{22} though an operational amplifier in the absence of any crosstalk suppression technique. (b) The ideal scenario where no crosstalk occurs due to the momentary formation of parasitic parallel paths in the resistor sensor array during sensel R_{22} readout

3.5 Crosstalk Suppression

Several implementations have been investigated in literature to substantially mitigate the spread of information and interconnect overloading associated with shared row-column architecture of sensor arrays. These crosstalk suppression techniques inevitably curtail the bypass currents flowing through parasitic parallel paths.

Traditional crosstalk suppression techniques involve inserting a diode [104] or a transistor [105, 106] across each individual sensing element. Although, it is a feasible for smaller sensor arrays inserting diodes/transistors are not a sensible approach for larger sensor arrays. Besides, inserting diode/transistor techniques have often been employed for sensor arrays with a smaller number of sensors. In addition, prospects of several other techniques such as passive integrator method (PIM) [91, 107], resistance matrix approach (RMA) [108], incidence matrix approach (IMA) [109], voltage feedback method (VFM) [103, 110–112] and zero potential method (ZPM) [113–116] have also been investigated.

However, VFM and ZPM have clearly offered several compelling benefits surpassing all other techniques discussed, in terms of simplicity in implementation (less wiring requirement), low complexity of operation, high precision and accuracy in measurements and low cost of implementation [102]. Both these methods follow the principle of creating an equipotential zone around the sensel that is being read momentarily, which is referred to as the "Element Being Tested (EBT)" (Sensel R_{22} in case of Figure 3.10(a).

3.5.1 Voltage Feedback Method

Voltage feedback method instantly feed the output voltage read (V_{read}) from the EBT (R_{22}) to all the columns and rows of the non-scanned sensels in the sensor array as shown in Figure 3.11, thereby retaining all the nodes except the EBT in an

equipotential state disallowing bypass currents to flow [102]. Hence, resistance of the EBT can be measured though voltage drop across it, by electrically isolating it from the sensor array [102].

According to Feng Wu [102], VFMs are often susceptible to a wide range of cirtuit parameters such as multiplexer switch-on resistances, wire resistances, operational amplifier (op-amp) parameters, circuit noise, Analog to Digital Converter (ADC) sampling frequency etc. Reason being that, in order to ensure that all non-scanned rows and columns remain at the same V_{read} voltage, voltage drops within the circuit components and paths should be a bare minimum. Depending on the type of feedback provided, VFMs can be further divided into three main categories as follows [94, 102].

1. Voltage feedback non-scanned-electrode (VF-NSE) method
2. Voltage feedback non-scanned-sampling-electrode (VF-NSSE) method
3. voltage feedback non-scanned-driving-electrode (VF-NSDE) method

Upon a thorough analysis of crosstalk suppression thorough VF-NSE, VF-NSSE and VF-NSDE methods, Liu et al. [94] has determined that VF-NSSE method is far more effective compared to the other two methods.

3.5.2 Zero Potential Method

Zero potential method rely on connecting all nodes of non-scanned sensels in the sensor array to virtual ground, thereby, preventing the formation of parasitic parallel paths and resultant bypass currents when the output is measured [102]. Similar to the VFM, EBT is therefore isolated from the sensor array and the voltage drop across it provides a reasonable estimate of the resistance of the EBT [94]. Figure 3.11(b) demonstrate a 3×3 resistor sensor array where all non-scanned sensels are retained at

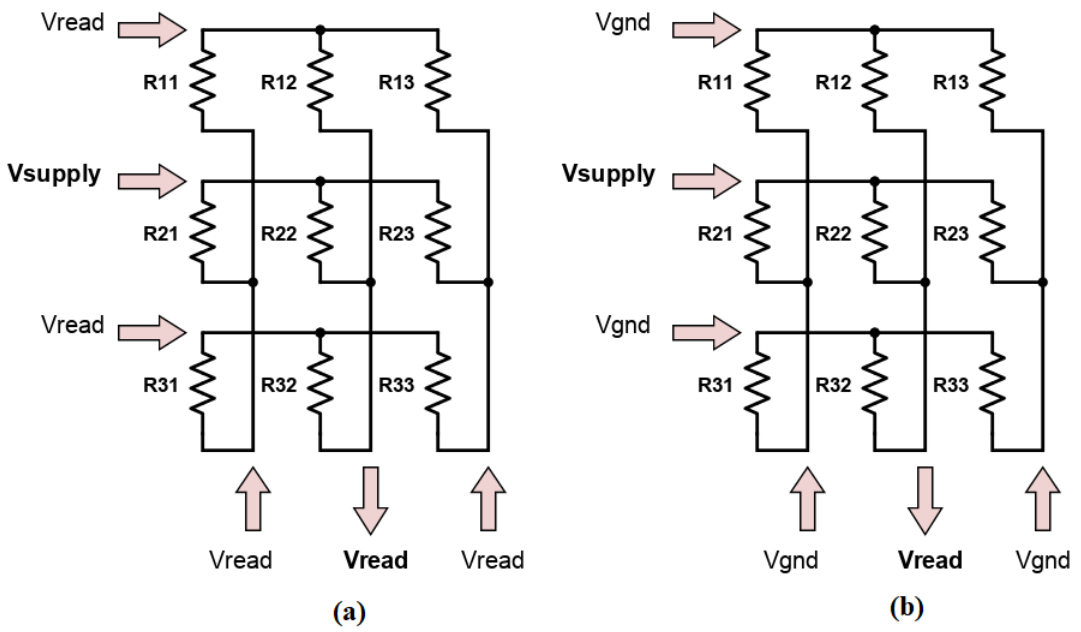


Figure 3.11: A voltage is supplied (V_{supply}) to the row 2 and the resultant voltage drop across the sensel (V_{read}) is measured from the column 2 in both 3×3 resistor sensor array models. **(a)** The output voltage (V_{read}) is fed to the rows and columns of the non-scanned sensels through feedback loops, so that both ends of non-scanned sensels are in an equipotential voltage equal to the output voltage. EBT is electrically isolated from the sensor array when measurements are taken. Therefore this is a voltage feedback crosstalk suppression mechanism based on VF-NSE method. **(b)** All the non-scanned rows and columns are momentarily connected to virtual ground via a switching mechanism inducing an equipotential voltage across all the non-scanned sensels while electrically isolating the EBT to take measurements. This is a zero potential crosstalk suppression mechanism based on S-NSE-ZP method

an equipotential ground voltage, avoiding any provision for formation of parasitic parallel paths, while reading the EBT (R_{22}).

Besides, based on an extensive series of simulation studies, Liu et al. [94] has demonstrated all three ZPMs are more competent in crosstalk suppression than all three variations of VFMs. Considering that, in ZPM no feedback loops are required to transmit the output voltage of an EBT (V_{read}) to the non-scanned rows and columns unlike VFM, the complexity of implementation is comparatively less. Moreover,

ZPM are more resistant to external interference, and they have shown to yield higher sensor array scanning rates and comparatively linear outputs than VFMs [94, 102]. In addition, Feng Wu [102] declares that ZPM have demonstrated better reliability and accuracy for implementations involving larger sensor arrays. Hence, zero potential based crosstalk suppression techniques appear to be the most formidable crosstalk suppression mechanism for platform based plantar pressure measurement systems.

Similar to the VFM, ZPM can further be classified into three main categories. This categorisation is based on the nature in which virtual grounding is achieved in the sensor array through row driving electrodes and column sampling electrodes. Sensor array scanning mechanism through row driving electrodes and column sampling electrodes is discussed in Section 3.9.

3.5.2.1 Setting Non-scanned Electrode Zero Potential (S-NSE-ZP) method

In this method, both row driving electrodes and column sampling electrodes of non-scanned sensels are connected to the virtual ground [94] as shown in Figure 3.11(b) when the EBT output is measured. Although, this method appear to be foolproof, adopting it into larger sensor array, adds to the complexity of implementation. As a result, mechanisms which virtually ground either the row driving electrodes or column sampling electrodes have been proposed [94, 102].

3.5.2.2 Setting Non-Scanned Sampling Electrode Zero Potential (S-NSSE-ZP) method

The S-NSSE-ZP method drives the column sampling electrodes of the non-scanned sensels of the sensor array to a virtual ground, while retaining the non-scanned row driving electrodes in a floating state when the EBT readings are taken [94] as shown in Figure 3.12. This method hypothesize that by keeping all non-scanned column sampling electrodes in virtual ground, no parasitic voltages are induced at nodes of

the sensor array as all the row driving electrodes are also in a floating state. Although this assumption does not hold true in practise, the induced errors are significantly true if component selection is done properly [94, 102]. VF-NSSE technique is analogous to S-NSSE-ZP technique where EBT output voltage (V_{read}) is fed back to the non-scanned sampling electrodes instead of driving them to virtual ground.

3.5.2.3 Setting Non-Scanned Driving Electrode Zero Potential (S-NSDE-ZP) method

The S-NSDE-ZP method involves driving the non-scanned row driving electrodes to a virtual ground, while retaining the non-scanned column sampling electrodes in a floating state when EBT readings are taken [94] as shown in Figure 3.12. The same assumption made in Section 3.5.2.2 is valid for this method too. That is, By retaining all non-scanned row driving electrodes in virtual ground, the likelihood of inducing parasitic voltages at nodes of the sensor array is sufficiently low, as all the column sampling electrodes are in a floating state. Then again, external interference could be kept at a bare minimum through careful component selection. VF-NSDE is analogous to S-NSDE-ZP technique such that in place of driving non-scanned row driving electrodes to virtual ground, the EBT output voltage is fed back to the on-scanned row driving electrodes [94].

3.5.3 Behavior of Biased Currents in Different Zones of the Sensor Array

Saxena et al. who quantified crosstalk within a resistive sensor array [100, 114, 117, 118] analysed the bias current flowing in a resistive sensor array with identical sensors (same resistance and same response to input). It was determined that a uniform resistor sensor array could be divided into 4 distinct zones as shown in Figure 3.13 such that in each zone, the bias current flowing is identical [99]. The four zones of bias current

distribution are given below.

1. Zone 1 - The EBT
2. Zone 2 - Group of sensels which share the same row as EBT
3. Zone 3 - Group of sensels which share the same column as EBT
4. Zone 4 - Group of sensels which are not directly conneced to the EBT

Moreover, Saxena et al. [99] derived the relationship between the bias currents flowing in each zone and discerned that sensels in a given zone shows identical behavior owing to the circuit symmetry exhibited by a uniform sensor array.

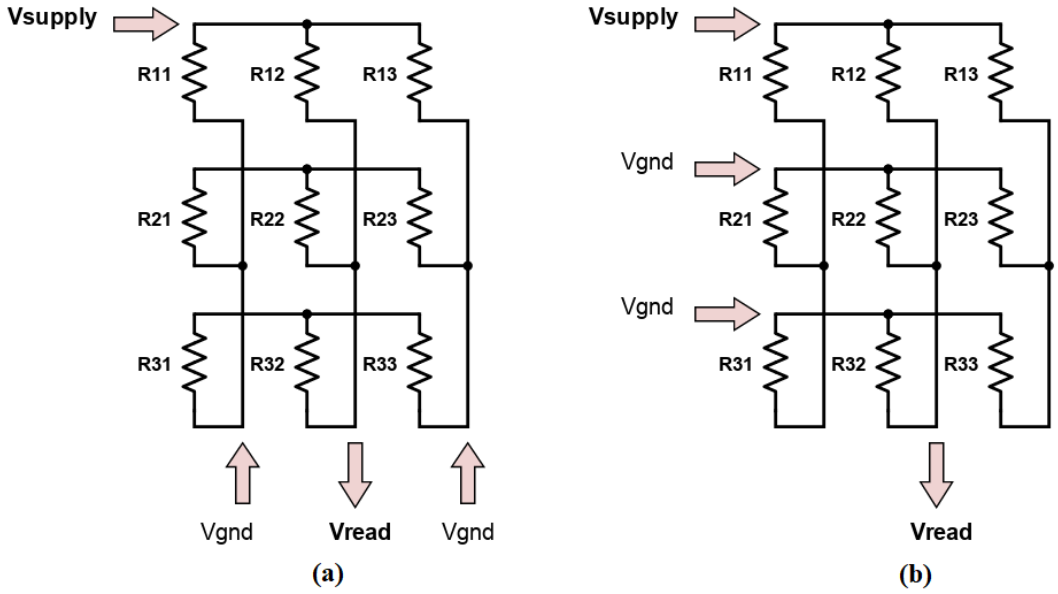


Figure 3.12: **(a)** Crosstalk suppression by setting non-scanned sampling electrode zero potential (S-NSSE-ZP) method. EBT is R_{12} as V_{supply} is given to row 1 and output (V_{read}) is measured through column 2. All the non-scanned rows (row 2 and 3) are kept floating while all non-scanned columns (column 1 and 3) are retained at ground voltage (V_{gnd}). **(b)** Crosstalk suppression via Setting non-scanned driving electrode zero potential (S-NSDE-ZP) method. R_{12} is the EBT of concern similar to (a). However, all non-scanned rows (row 2 and 3) are retained at ground voltage (V_{gnd}) while all the non-scanned columns (column 1 and 3) are kept floating

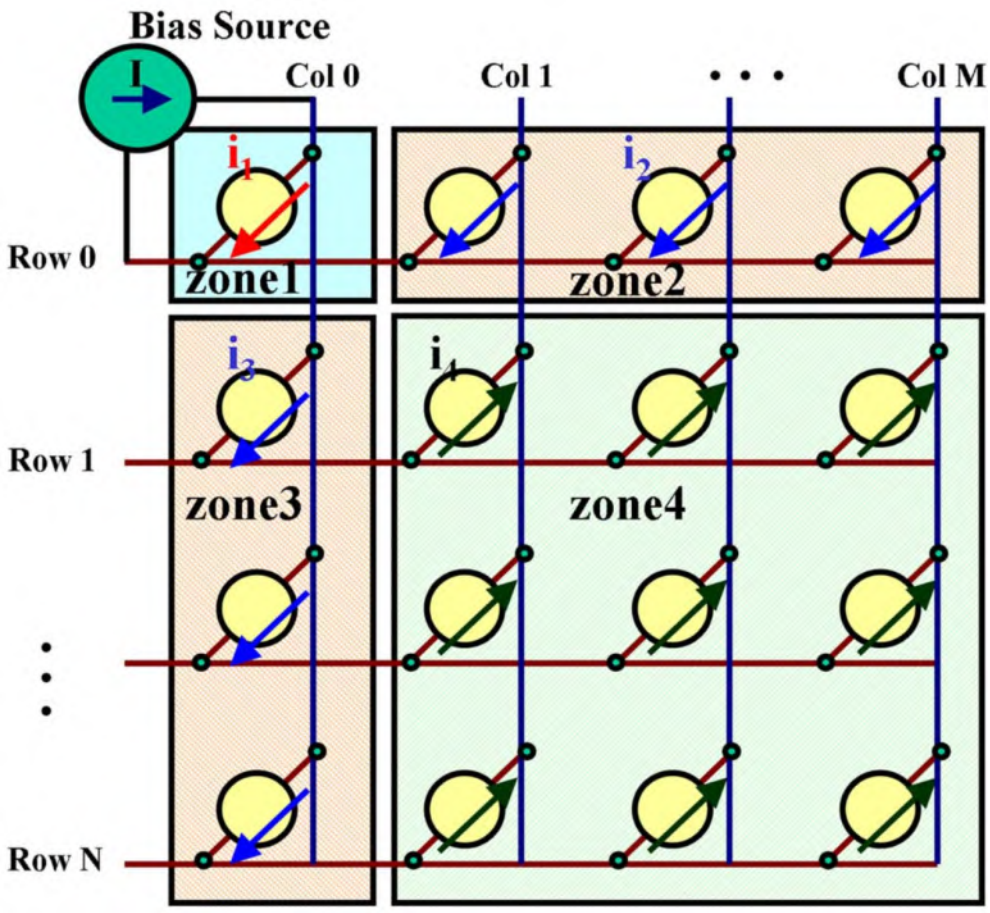


Figure 3.13: Four distinct zones that a uniform resistor sensor array could be categorized depending on the bias current. The bias current was determined to be the same in each zone. Image courtesy Saxena et al. [99]

3.6 Commercial Platform Systems and their Limitations

Several leading commercial vendors such as Sensor Medica®, Emed®, Tekscan®, Medilogic® etc. are manufacturing variety of different platform systems using different sensors, dimensions, spatial resolutions, scanning rates and measurable pressure ranges as shown in Table 3.2. Conventionally, an operation frequency of over 200 Hz is desired for measurements under both static and dynamic conditions [64, 77]. High spatial resolutions are favored when the structures of

interest that needs to scanned are smaller in size [119].

One of the notable limitations of a typical commercial platform system is that a high spatial resolution (around 4 sensels per unit area) and a high scanning rate (≥ 200) could not be achieved simultaneously. As indicated by the Table 3.2, high scanning rates are possible only at the expense of low spatial resolutions and vice versa. However, high spatial resolution and high scanning rates are always desired for better detection of diabetic foot complications and related morbidity [77, 119].

Table 3.2: Comparison of the main features of commercially available platform systems. Sources: [83, 120, 121]

Sensor Name	**Sensor Type***	**Sensor Resolution (per cm^2)****	**Sensing Area ($cm^2 \times cm^2$)**	**Scanning Rate (Hz)**	**Pressure Range (kPa)**
MobileMat 3140	P	1	48.7×44.7	100	345–862
MobileMat HR	P	3.9	48.7×44.7	185	345–1103
Matscan 3150	P	1.4	43.6×36.9	100	345–862
Matscan VersaTek	P	1.4	43.6×36.9	440	345–862
HR Mat 7101E	P	4	48.8×44.7	185	345–1103
Strideway 3160	P	0.968	65×520	500	276–862
Strideway 3162	P	2.19	65×520	250	276–862
Strideway 3164	P	3.88	65×520	250	276–862
Emed-xl	C	4	14.40×44	100	10–270
Emed-x400	C	1 or 4	47.5×32	100	10–270
Emed-q100	C	4	47.5×32	100	10–270
Emed-n50	C	4	47.5×32	50	10–270
Tactilus	C	–	40×40	100	13–855

* P – Piezoresistive, C – Capacitive
** Sensor Resolution is calculated as Sensels per cm^2

Platform systems are inherently subjected to crosstalk interference as discussed in Section 3.4.2. Therefore, effective crosstalk suppression mechanisms are essential to

ensure the accuracy of the plantar pressure measurements taken from commercial platform systems. However, almost all the commercial platform systems incorporate software based crosstalk suppresion techniquess [77, 121, 122]. The issue with software based crosstalk suppression techniques is that they use proprietary algorithms to enhance certain features while diminishing others.

Generally for commercial platform systems, accurate measurement of the pressure distribution can only be obtained through crosstalk suppression algorithms. In foot complication detection using plantar pressure measurements, analysis of shape contours related high/low pressure localisation in the feet is of prime importance. However, an improved estimation of shape can only be obtained through algorithms which repress actual pressure values to estimate a precise shape.

Figure 3.15 demonstrates this complication associated with software based complications where no perfect algorithm exist to estimate an accurate shape meanwhile providing accurate measurements. Figure 3.14 shows the metal disc which was used to obtain pressure and shape measurements shown in Figure 3.15 under static and dynamic conditions. Figure 3.15(b) and (d) illustrate how dimensional features have been repressed in order to enhance accurate measurement values in static and dynamic conditions respectively through algorithms. Similarly, Figure 3.15(a) and (c) illustrate how measurement accuracy is repressed to enhance accurate shape estimation via algorithms. Although, this discrepancy exist in both static and dynamic measurement conditions, incorporated error while shape determination and pressure determination are comparatively high under dynamic conditions (Figure 3.15(c),(d)).

Figure 3.14: Metal disc which was placed on a SensingTex® platform system to measure pressure distribution under two different loading conditions (static and dynamic) and using two different compensation algorithms

3.7 Prospects of the Proposed Pedobarographic System

The present research investigates the possibility of overcoming the inherent drawbacks in commercial platform systems for plantar pressure measurement. Since it is evident from literature that hardware based crosstalk suppression techniques are bound to be rather effective than software based crosstalk suppression techniques (Section 3.5), our primary goal in this study was to implement a suitable hardware based crosstalk suppression mechanism to a sensor array. Effectiveness of implemented crosstalk suppression is reflected through the measurement accuracy (ability to measure the pressure values correctly) and the shape accuracy (ability to estimate the shape of object) of the developed circuitry which will be discussed in Section 3.8

Considering that both static and dynamic conditions needs to be assessed, a larger sensor array based on piezoresistive sensors with a high spatial resolution of 4 sensels

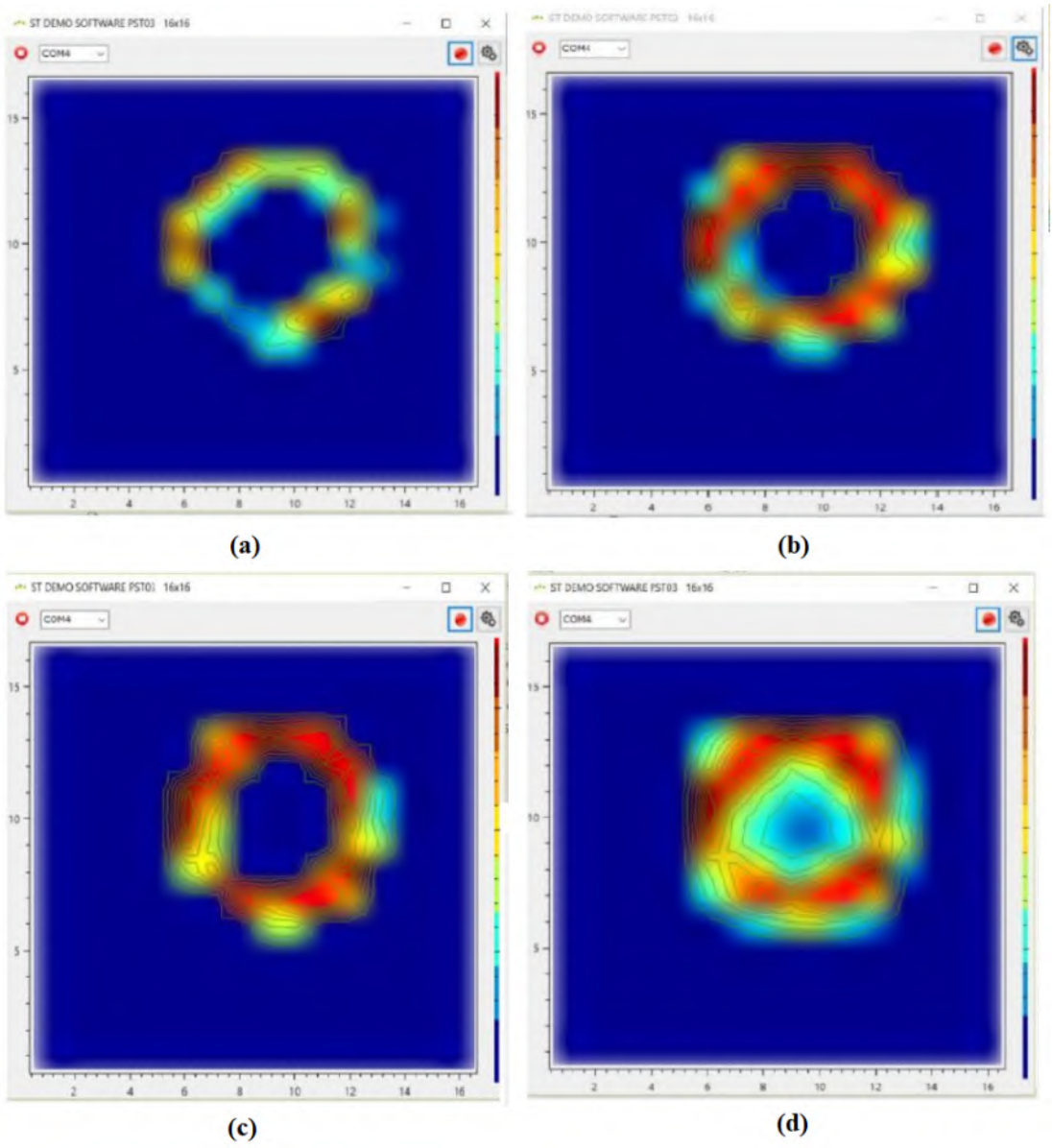


Figure 3.15: **(a)** In static measurement mode when shape accuracy is more important than measurement accuracy. Shape of the object is more reliable than the measured pressure **(b)** In static loading condition when measurement accuracy is more important than shape accuracy. Pressure measurements are more reliable than predicated shape.. **(c)** In dynamic measurement mode when shape accuracy is more important than measurement accuracy. Shape of the object is more reliable than the measured pressure **(d)** In dynamic loading condition when measurement accuracy is more important than shape accuracy. Pressure measurements are more reliable than predicated shape. Source: SensingTex PST and MAT dev kits [122]

per cm^2 was selected. As smaller sensor array dimensions correspond to high scanning rates, we implemented the larger sensor array as ten distinct clusters that could be scanned separately and processed in parallel. Therefore, by incorporating effective hardware based crosstalk suppression technique on a large piezoresistive sensor array with high spatial resolution, we investigated the possibility of achieving a high scanning frequency.

3.8 Evaluating Crosstalk Suppression with Measurement Accuracy and Shape Accuracy

3.8.1 Measurement Accuracy

Assessment of measurement accuracy of a given scanning mechanism with crosstalk suppression has often been conducted through simulation studies. Saxena et al. [99, 100, 114, 117, 118] conducted several such simulation based measurement accuracy assessment. However, Kim et al. [116] proposed to evaluate a given scanning mechanism with crosstalk suppresion using a combination of simulation studies and physical resistor array model of 4×4 as shown in Figure 3.16. As discussed in Section 5.7, this approach was the most feasible in validating a given scanning architecture with crosstalk suppression.

According to Wu et al. [102], measurement accuracy is dependant on both conversion accuracy of the sensels (ability of the sensel to accurately provide a uniform excitation to pressure) and circuit parameters of the scanning architecture. Assuming the proper functionality of the sensels the measurement accuracy of the developed mechanism rely on the implemented scanning architecture and the degree of crosstalk suppression.

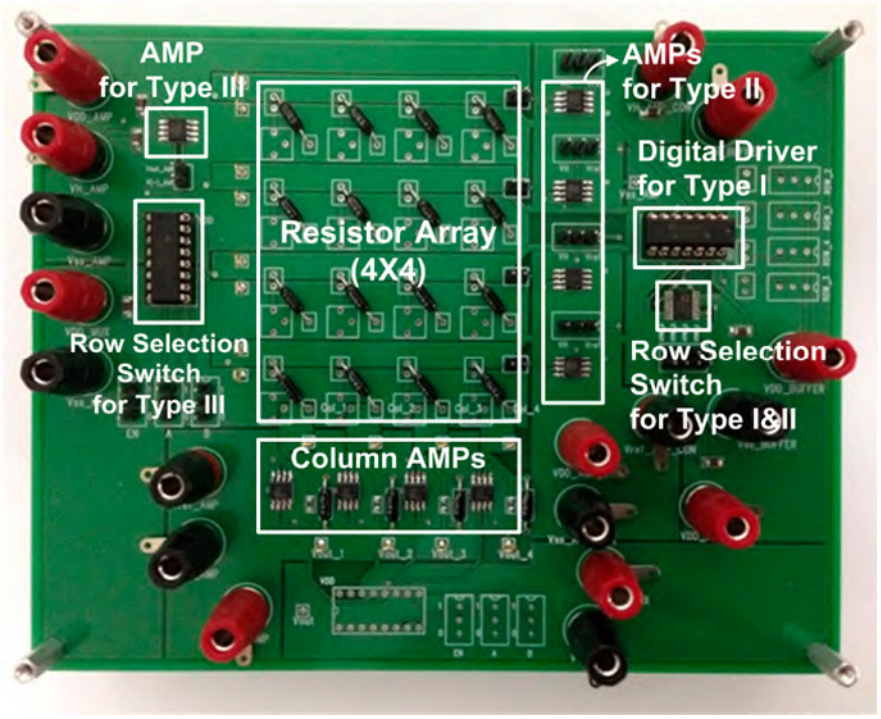


Figure 3.16: The 4×4 resistor array model developed by Kim et al. [116] to evaluate a newly proposed scanning architecture

3.8.2 Shape Accuracy

Vidal-Verdu et al. [107] were one of the pioneers who quantified the efficacy of a sensor array scanning technology using shape profiles of the sensor output. Different objects with unique shapes were placed on the sensor array and the propensity of the sensor array output shape and the actual shape of the object have been observed as shown in Figure 3.17.

Meanwhile, Yang et al. [123] evaluated the shape accuracy of a temperature and tactile sensor array by placing numerous shapes of varying temperature to monitor the impact of crosstalk on measurement.

Intuitively, shape accuracy is a qualitative assessment which provides insight into the degree of crosstalk suppression as impact of nearby non-scanned sensels will not feature in the final output, had crosstalk suppression been implemented completely.

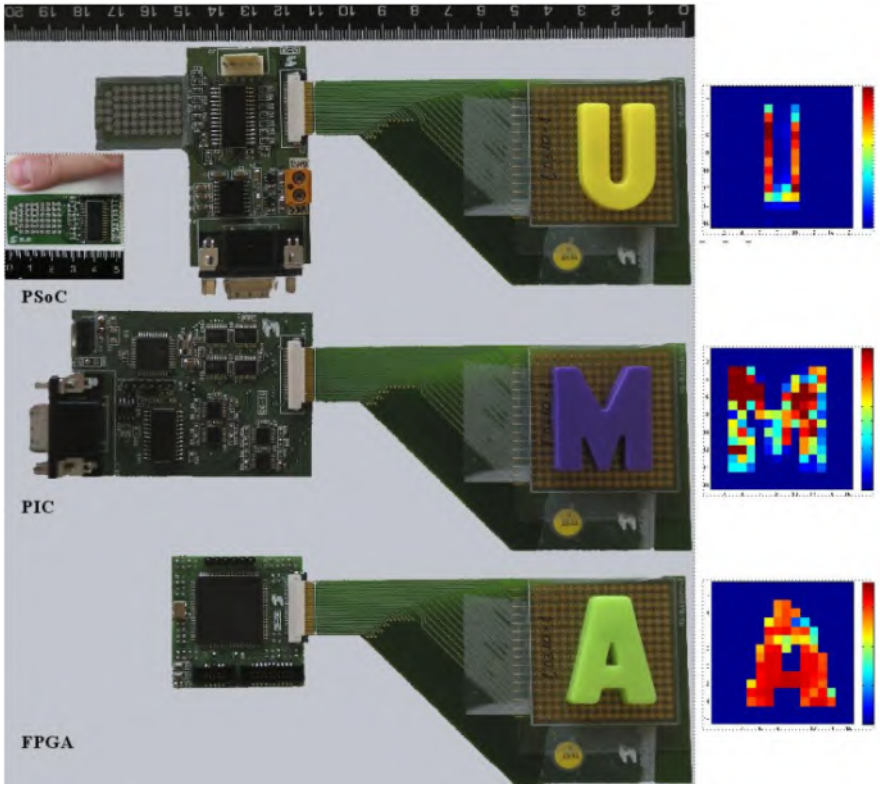


Figure 3.17: The Shape accuracy assessment conducted on different scanning mechanisms using different shapes by Vidal-Verdu et al. [107]

3.9 Scanning Architectures Used for Sensor Array Readout

On the grounds that each sensel in the sensor array is connected to a shared row and a shared column, each sensel can be assessed by connecting its corresponding row to a supply voltage and measuring the voltage output of the corresponding column while all the non-scanned rows and column are electrically disconnected [93]. Thereby, all the sensels in a given row of the array can be scanned by activating that row and scanning all the columns in the array. If this manoeuvre is repeated gradually across all the rows in the sensor array, the entire sensor array can be scanned [93, 94]. This basic principle behind scanning of a sensor array with a shared row-column architecture is illustrated in Figure 3.18.

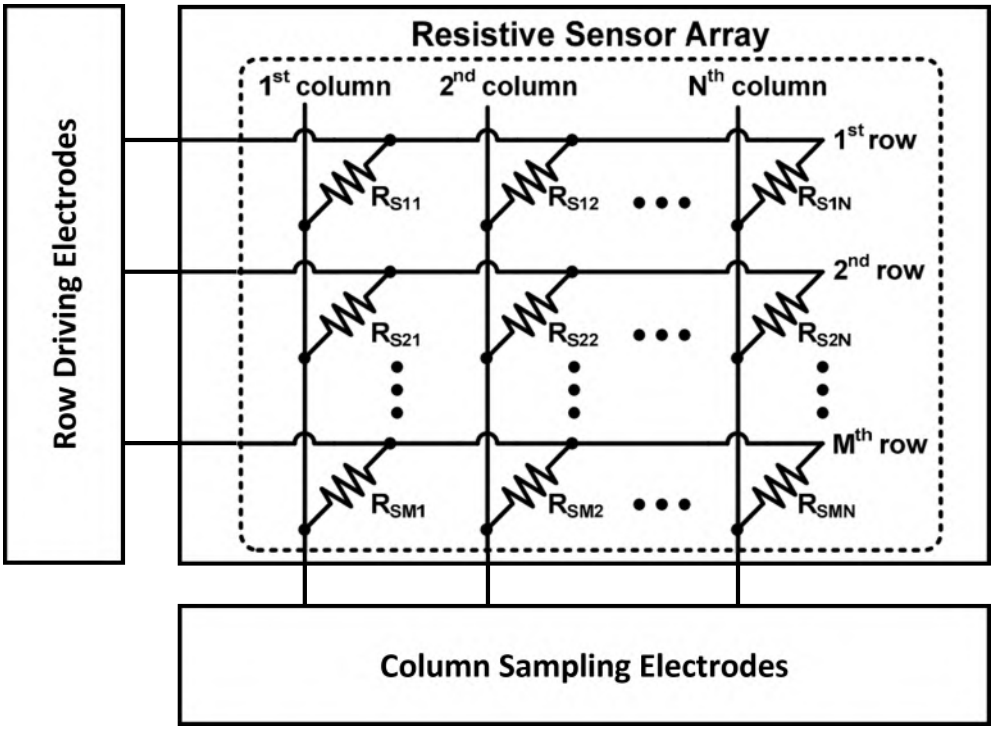


Figure 3.18: Basic principle behind sensor array scanning. The row driving electrodes connect the desired row to a voltage supply and the column sampling electrodes incrementally measure the output of each column of the selected row. By repeating this process whole sensor array could be scanned.

Almost all zero potential crosstalk suppression mechanisms realized in reported literature have adopted op-amps as the column sampling electrodes [93, 102, 103]. However, Kim et al. [116] has categorized row driving electrodes (sometimes referred to as row drivers) into two main types as those consisting of multiplexers (Type I) and op-amps (Type II) respectively.

Analog to digital convereters (ADCs) have been often relied upon to convert the voltage readings from column sampling electrodes to digital signals which are subsequently dispatched to a controller which transmit them to a computer for image construction (from individual data of all sensels), further processing and analysis.

3.9.1 Row Driving Electrodes with Multiplexers

In this type of zero potential based sensor array scanning method, row driving electrodes comprise of multiplexers (digital buffers) while the column sampling electrodes comprise of op-amps [107, 123–125] as shown in Figure 3.19. For a sensor array of $M \times N$, M number of multiplexers and N number of op-amps are required to realise the scanning electronics.

Switch-ON resistance of multiplexers (R_{ON}) used in the row driving electrodes contribute extensively to the accuracy of measurements [116], on the grounds that a voltage drop occurs across R_{ON} when scanning a row. Moreover, upon conducting a series of circuit simulation studies though PSPICE®, Kim et al. [116] has concluded that these types of row driving electrodes are associated with maximum error of 40% and 60% for sensor arrays containing 10 columns and 30 columns respectively.

3.9.2 Row Driving Electrodes with Operational Amplifiers

Op-amps form the key electronic foundation in this particular category of driving electrodes, where op-amps constitute for both row driving electrodes as well as column driving electrodes [95, 113, 126] as shown in Figure 3.20. Therefore, for a sensor array of $M \times N$ dimensions, $M + N$ op-amps are required to realize the related scanning electronics.

One of the main drawbacks of this type of scanning electrodes is that they require an excessive number of op-amps compared to Type I scanning electrodes. Op-amps being components with strenuous power consumption, drastically increases power consumption of the system [116]. Additionally, they increase the complexity, volume as well as the cost of the implemented system. These type II systems do not encounter erros associated with Switch-ON resistance (R_{ON}) unlike type I systems, for the reason that op-amps exhibit an infinite input impedance. However, these systems often suffer from inaccuracies due to the non-idealities present in op-amps [116].

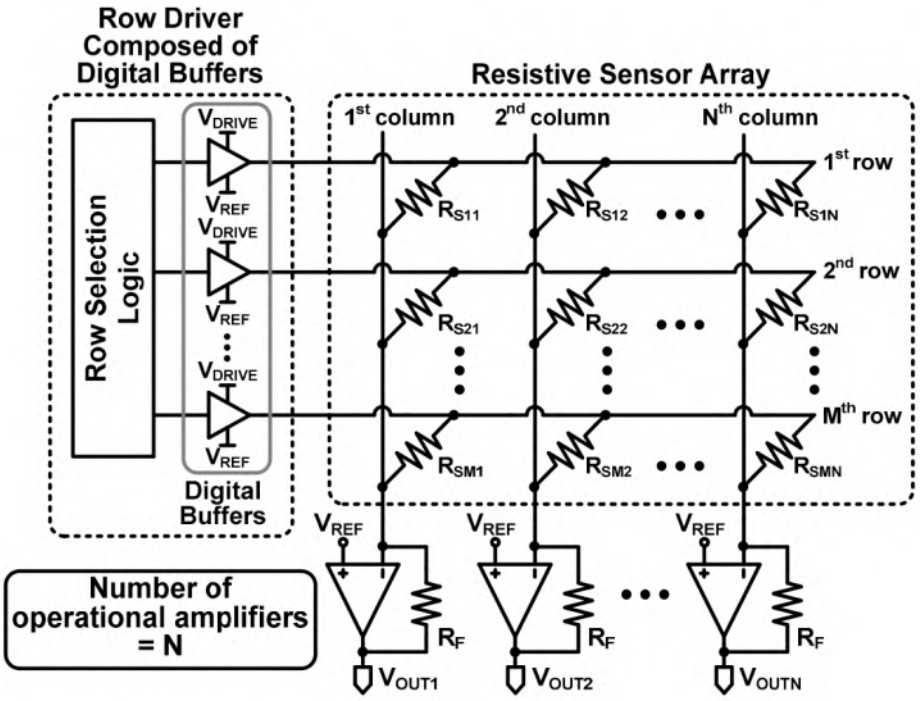


Figure 3.19: Sensor array scanning mechanism consisting of row driving electrodes with multiplexers. (Type I) Image source Kim et al. [116]

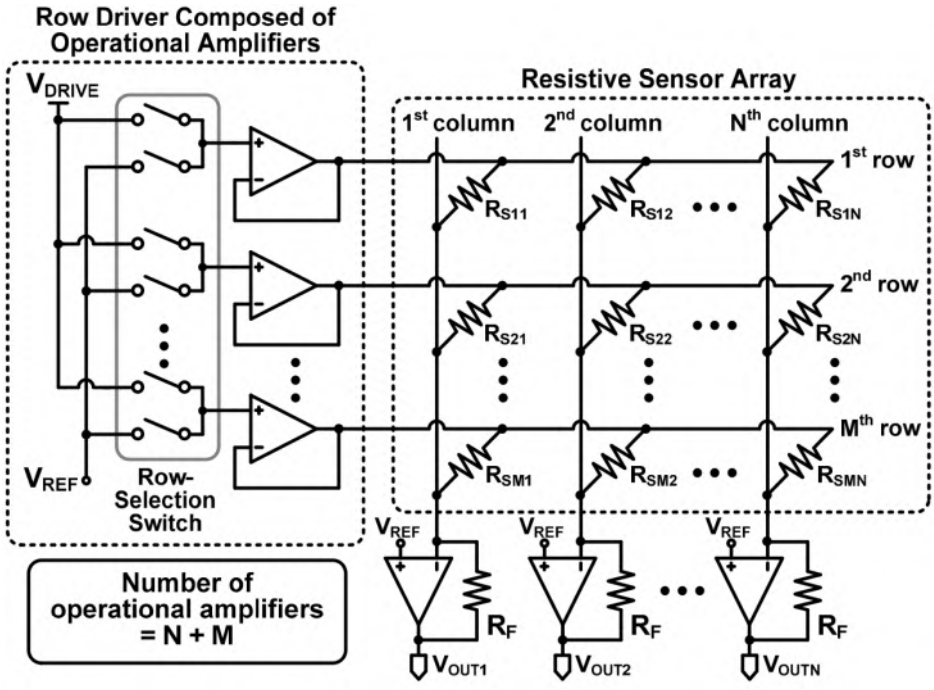


Figure 3.20: Sensor array scanning mechanism consisting of row driving electrodes with operational amplifiers. (Type II) Image source Kim et al. [116]

These non-idealities stemming from input offset voltages, input bias currents and gain error due to finite open loop gain [116] could be curtailed by carefully selecting a high precision op-amp for the given circuit parameters. According to Kim et al. [116], despite all these minor limitations, type II systems are capable of producing measurements with errors less than 1%.

3.9.3 Row Driving Electrodes with an Operation Amplifier and Switches

This is a novel concept for row driving electrode system proposed by Kim et al. [116] where the circuit complexity, power consumption and cost of implementation issue of type II systems have been reduced by a significant factor. For instance, a type III system requires only $N+1$ op-amps to scan a sensor array of $M \times N$ dimensions as shown in Figure 3.21. Kim et al. [116] explicitly declares that the proposed type III implementation is more suitable for implementation of large sensor arrays. However, the behavior of the op-amp used as row driving electrode, during high frequency switching when scanning large number of sensels within a short duration of remains a question [127].

3.10 Controllers Used for signal handling and Data Acquisition

Mere existence of a sensor array and scanning electrodes alone are not adequate to scan and generate a pedobarogram. Additional electronic circuitry are required for signal conditioning, control timing, signal handling, component addressing, control switching of row driving electrodes and column sampling electrodes, analog to digital conversion and subsequently transmit the corresponding digital data to a computer for further processing and image formation [91, 107]. Therefore, numerous hardware

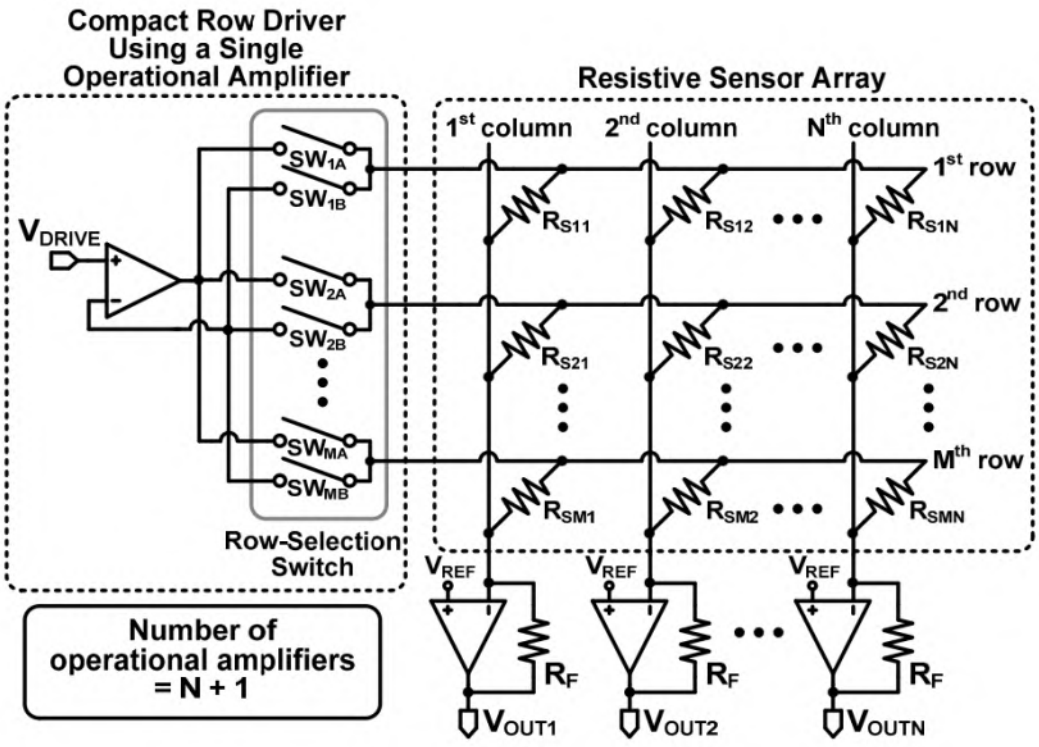


Figure 3.21: Sensor array scanning mechanism consisting of row driving electrodes with one operational amplifier and switches. (Type III) Image source Kim et al. [116]

components and circuitry are essential to realize a fully pledged pedobarographic system.

3.10.1 ASIC Based Systems

Application-specific integrated circuits (ASIC) are developed for specifically for a particular application unlike general purpose ICs. Several implementations based on ASIC chips which function as a co-processor to scan smaller sensor arrayw have been realized [128–130]. Most of these implementations are based on tactile sensor arrays, and are designed to be used as wearable devices or during minimally invasive surgery (to acquire heptic feedback) [129]. Although, such implementations are befitting for scanning smaller sensor arrays, limited data processing capability, programmability, upgradability upon manufacturing [107] brand them less desirable for plantar pressure

measurement applications.

3.10.2 Microcontroller Based Systems

Microcontroller centered scanning architecture overcome the limitations in data processing, programmability and upgradability posed by ASIC based systems by a substantial amount. Literature reports a diverse range of sensor arrays developed with microcontroller centered architecture [108, 131, 132]. Rathnayaka et al. [132] has implemented a pedobarographic assessment tool with 1024 sensels and an ARM Cortex M4 based STM32F3 development board.

Figure 3.22 indicate the local electronics involved in implementing a sensor array scanning mechanism using a type I scanning architecture (Section 3.9.1) with a PIC18F4680 microcontroller as the central controller. A CAN bus has been used to transimit the collected data from the microcontroller to a computer for further processing.

On the grounds that microcontrollers are sequentially processing devices, the scanning rate is comparatively low. Besides, they require several PCBs to perform the desired action if implemented for a platoform system. Hence intricate wiring requirement, large volume of space taken to a few drawbacks when implement the scanning architecture based on a microcontroller [107]. Nonetheless, microcontroller based systems are more pertinent for in-shoe plantar pressure measurement systems due to the minimal amount of sensels present in them [133–135].

3.10.3 Programmable System on Chip Based Systems

Sensors arrays encompassing Programmable System on Chip (PSoC) as the controller present an overall improvement over microcontroller based systems as they are highly reconfigurable, additional hardware requirement is less, has built-in provisions for

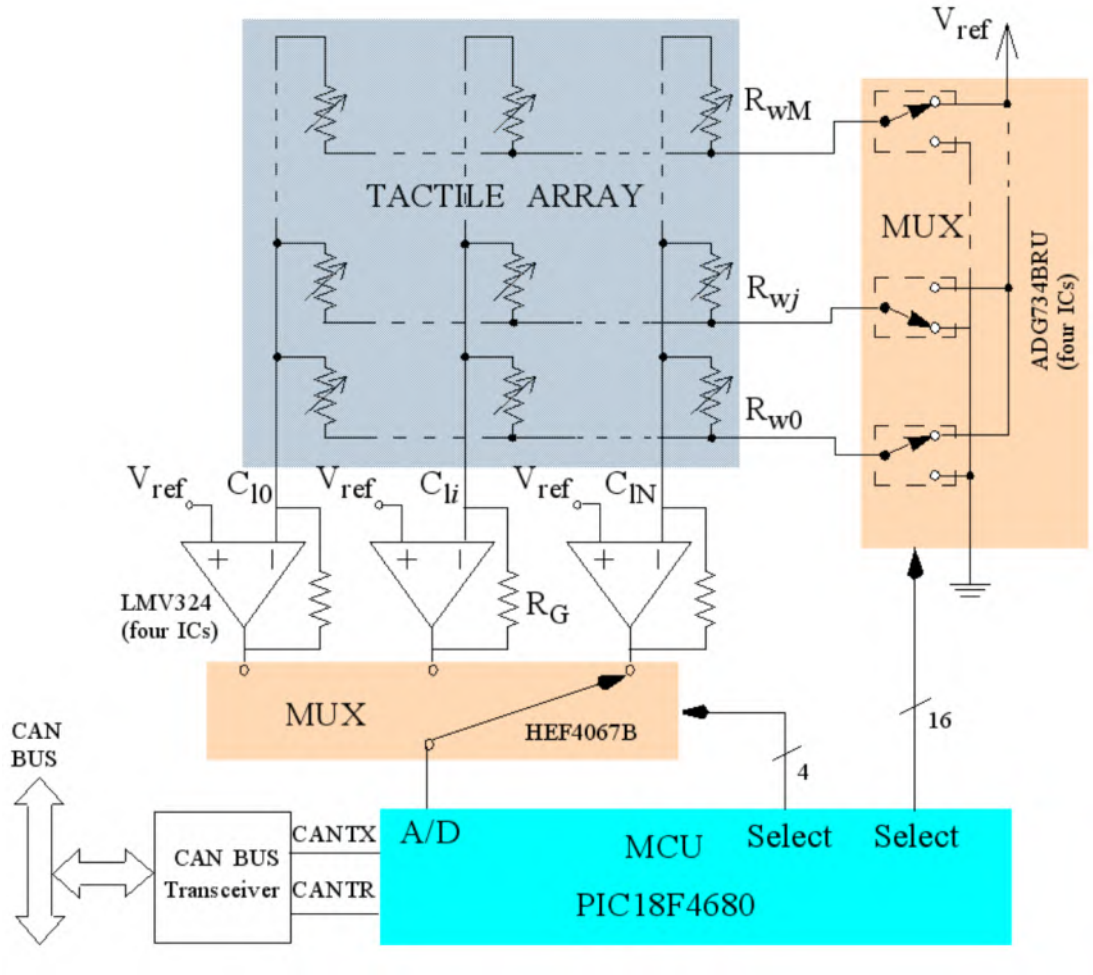


Figure 3.22: Microcontroller centered hardware architecture for scanning a sensor array. Image adapted from Vidal-Verdu et al. [107]

interacting with outside analog circuitry/signals and on-chips blocks enable parallel processing to a certain level [107, 136]. The main limitation when implementing a large sensor array is the resource limitation in the number of (General Purpose Input Output) GPIO pins [107].

3.10.4 Field Programmable Gate Array Based Systems

Sensor array scanning techniques incorporating development boards built around Field Programmable Gate Array (FPGA) as the main controller has been proposed and implemented [91, 107, 137]. These implementations offer remarkably high

performance owing to their parallel processing capability, making them more suitable for controlling large sensor array scanning as they can handle large volumes of data in real time [107]. In addition, they are reconfigurable hardware, thus, upgrade-ability and the flexibility rendered by these devices are remarkably high [91, 137].

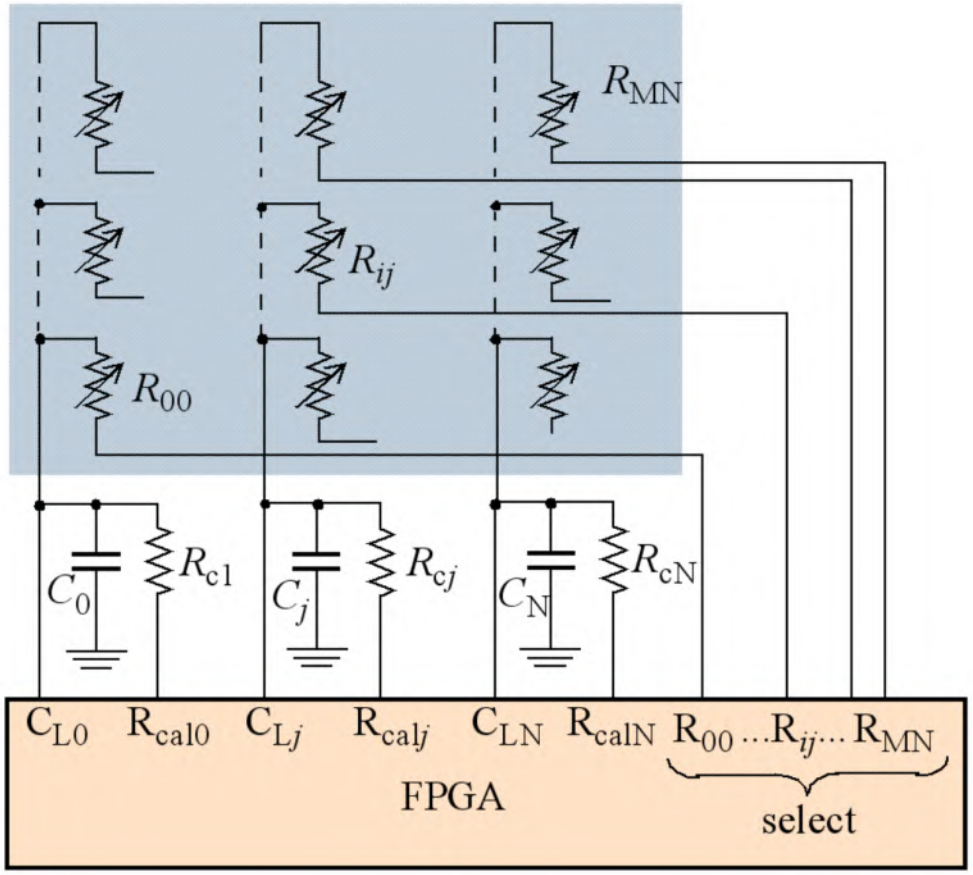


Figure 3.23: FPGA based hardware controller for scanning sensor arrays. Due to the high GPIO availability in FPGA based development board, all the rows and columns of a low-to-medium sensor array could be directly interfaced with the FPGA. Image adapted from Vidal-Verdu [107]

Traditional FPGA chips can not control a process alone as can only function as hardware accelerators [138]. Therefore, FPGA chips are embedded into a development boards which include several peripheral hardware components that allow the FPGA based system to offer enhanced performance [91, 139]. Most of the recent developments have in-built analog to digital conversion capabilities which helps in reduction in the secondary hardware requirement [91]. Besides, the recent

FPGA centered development boards house an extensive amount of GPIO ports which can directly interface with external component [107] as shown in Figure 3.23.

Therefore, among the existing hardware solutions to oversee signal conditioning, basic control, data acquisition and transmission when scanning large piezoresistive sensor arrays, FPGA based systems prove to be the most feasible solution.

3.10.5 All Programmable System on Chip Based Systems

System on Chip (SoC) is a silicone chip which include several IP blocks on a single silicone chip [140]. SoCs house numerous CPUs, GPIOs, GPIOs and a fixed number of hardware accelerators [141]. Although, there exists provision for software control though the configurations of IP blocks, the control of hardware accelerators is beyond the reach of the end user [141].

Conversely, conventional FPGAs, which are used primarily as hardware accelerators, are exclusively hardware platform which enables parallel processing with no provision for software controlability [138]. The flexibility and the dynamic performance of FPGAs are still exorbitant despite the advent of high end processors to the market [141]. The downfall of FPGAs are that their high power consumption, size and the cost [139].

Therefore, by consolidating benefits of both SoCs and FPGAs, a new line of hardware platforms called All-Programmable System on Chip (AP-SoC) (sometimes referred to as "Fully-Programmable SoC") have started to penetrate the market, which comprises of a dedicated hard core processor alongside FPGA which could communicate via interconnections [142]. Xilinx Zynq is a feature rich AP-SoC, which comprises of a dual core Arm Cortex processor (Prcessing Side – PS) with a Xilinx Kintex 7 FPGA fabric (Programmable Logic – PL). The architecture of Xilinx Zynq AP-SoC device is shown in Figure 3.24. The high design flexibility, limited resource utilisation and high dynamic performance due to the partitioning of software and hardware components

prompted the present study to investigate the possibility of implementing the proposed pedobarogrpahic system with the use of an AP-SoC based controller.

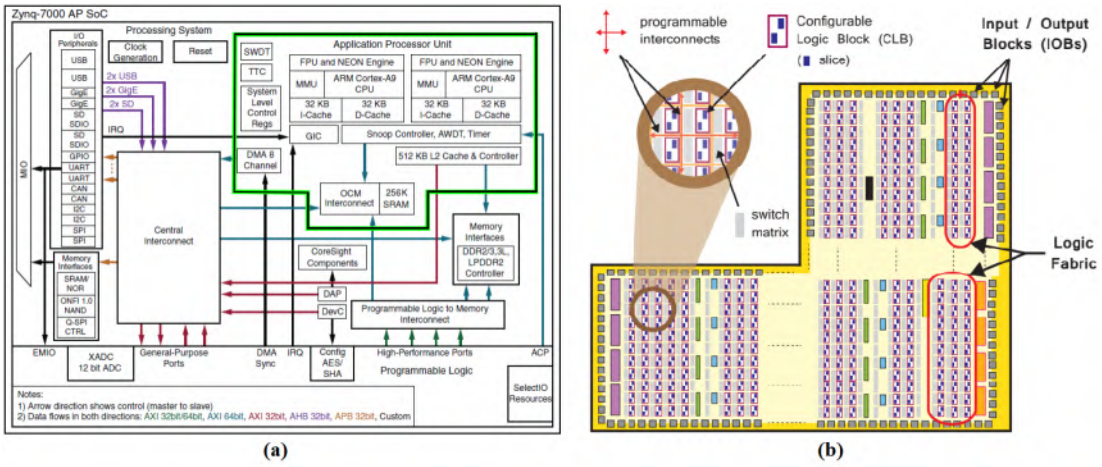


Figure 3.24: The AP-SoC architecture of the Xilinx Zynq device. **(a)** The architecture of the Processing Side (PS). **(b)** The architecture of the Programmable Logic (PL)

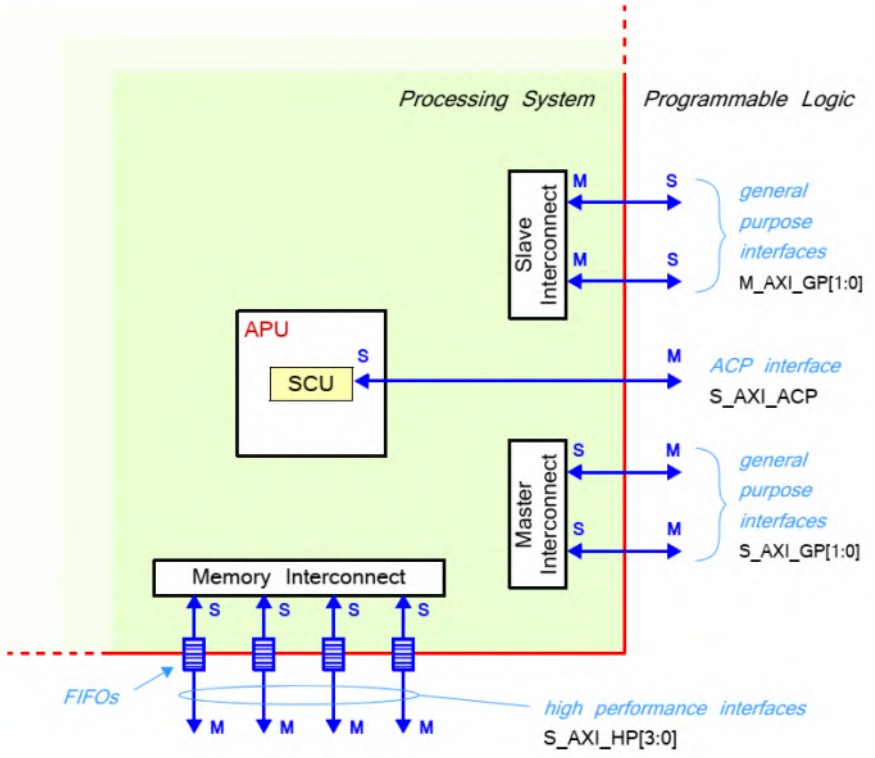


Figure 3.25: The three main types of interconnections between the PS and the PL of Xilinix Zynq APSoC

Advanced eXtensible Interface (AXI) which developed by ARM AMBA® is considered to be the "the de facto standard for on-chip communication", is the foundation for the interconnectivity between PS and PL. Interface between the PS and PL is established through nine dedicated AXI interfaces, namely, 4× General Purpose ports (GP), 1× Accelerator Coherency Port (ACP) and 4× High Performance (HP) Ports [142] as shown in Figure 3.25. Out of four GPs, two have PS as the master while other two have PL as the master. They all support low to medium rate communications between the PS and PL with a fixed bus width of 32. The four HPs are used to interface the PL with PS memory components at high speeds where PL assume the role of master in each port. Meanwhile ACP is used to generate coherency between the Snoop Control Unit and PL.

3.11 Summary and Conclusions

There exist two types of plantar pressure measurement systems, namely, platform systems and in-shoe systems. The limited number of sensels in in-shoe systems is not ideal to generate pedobarograms as opposed to platform systems. Platforms systems are manufactured with different sensor technologies among which, piezoresistive sensor arrays are the most popular. A shared row-column architecture is often preferred for reading piezoresistive sensor arrays, since it reduces the interconnect complexity due to the increased number of sensels.

Therefore, scanning of a piezoresistive sensor array is performed through a series of row driving electrodes and column sampling electrodes connected across the shared rows and shared columns of the sensor array respectively. Based on the composition of the row driving electrodes, the scanning architecture can be further categorized as type I, type II or type III systems. Type I systems which incorporate digital buffers as row driving electrodes are prone to high measurement errors while type II systems which incorporate op-amps as row driving electrodes are often exhibit high energy consumption. Although, type III systems which exhibit better performance over type

I and type II systems, the main limitations are the the high complexity and cost of implementation with the increased number of sensels.

Despite the reduction in interconnect complexity as a result of shared-row column architecture, the main limitation is the interconnect overloading which manifest as crosstalk among sensels. Crosstalk can be mitigated using either software or hardware compensation techniques and the degree of crosstalk suppression is often evaluated using the measurement accuracy and the shape accuracy of the output generated. Hardware compensation techniques allow simultaneous improvement of measurement accuracy and shape accuracy, making it the most attractive technique. Among several hardware compensation techniques the VFM and ZPM are the most endorsed crosstalk suppression techniques in literature with ZPM method demonstrating a superior performance over the others.

Several types of controllers have been used in literature to implement sensor array scanning and FPGA based approaches have proclaimed better performance for larger sensor arrays. However, novel class of controllers called APSoC devices have penetrated the market emphasising the enhanced performance due to their unique combination of a hardcore processor and a FPGA on the same chip.

In conclusion, a suitable scanning architecture that improves on the type III systems with regard to complexity and cost of implementation is desired for scanning of a piezoresistive sensor array with increased number of sensels. The novel scanning architecture must comply with a suitable ZPM based crosstalk suppression technique as a means to mitigate the undesired crosstalk among sensels. The effectiveness of the implemented scanning architecture and the degree of crosstalk suppression could be quantified through a thorough analysis of the measurement accuracy and the shape accuracy. Besides, the system implementation can be incorporated with an APSoC controller due to the high performance superiority exhibited as a result of separate processing side (PS) and a programmable logic (PL) which could be configured for software routines and hardware acceleration tasks respectively.

CHAPTER 4

Plantar Temperature Measurement

4.1 Risk Assessment of the Diabetic Foot Plantar Using Temperature Measurements

Humans being homeothermic animals, maintain a stable core-body temperature (thermoregulation) within ± 0.6°C. An alteration in the body temperature and/or the temperature of a specific region in the body, therefore is indicative of an underlying problem [143]. In fact, body temperature is considered to be the most routinely measured physical entity in the world after time [144].

Especially, cutaneous (skin) circulation is instrumental in human thermoregulation because vasodilation of the cutaneous blood vessels promotes heat emission from the skin surface while vasoconstriction promotes retention of heat within the body [145]. As Peripheral Artery Diseases (PADs) deteriorate the function of peripheral blood vessels, blood circulation to the foot plantar is often reduced or ceased. As a result, the subcutaneous blood supply to the peripheral nerves to the subcutaneous nerves are also reduced or ceased. In addition, inflammations that result due to tissue damages in the subcutaneous of the foot plantar are also known to elevate foot plantar temperature [143].

On the grounds that the surface skin temperature is reliant on many internal (age,

weight etc.) and external factors (environment temperature, use of foot ware etc.) obtaining an authentic diagnosis from temperature value alone is problematic [146]. As a solution, Kaabouch et al. [147, 148] proposed a mechanism to compare contralateral regions of both feet to determine diabetic foot related complications with an increased efficiency, which is refereed to as "Asymmetric analysis".

Several asymmetric analyses have advocated that a 2.2°Cor more between two contralateral regions in the diabetic foot plantar is an early indication of a diabetic related foot complication that pose the risk of a subsequent ulcer [149–151]. Moreover, Van Netten et. al [36] have demonstrated through a preliminary study that a temperature difference greater than 3°C measured via an asymmetric analysis is characteristic of a PAD which has begun manifesting into a diabetic foot complication that demands immediate medical intervention.

4.2 Existing Plantar Temperature Monitoring Techniques

Plantar temperature assessment revolves around the basic principle of measuring the surface temperature of the susceptible diabetic feet either through contact sensors or non-contact sensors [38, 149].

Contact sensors employ the principle of conduction to record the temperature of the object it is in contact with [144]. Thermostats, thermocouples and Resistance Temperature Detector (RTD) are some common contact temperature sensors [144, 152].

Conversely, non-contact temperature sensors employ radiation (and sometimes convection) principles to record the temperature of a nearby object which does not necessarily have to be in contact with the measured object [144]. Infrared temperature sensors and infrared thermal cameras are the most commonly used non-contact

temperature sensors in literature [144, 152].

Unlike plantar pressure measurements which is recorded under both static and dynamic conditions, plantar temperature is often preferred to be measured under static conditions. Considering that dynamic measurement involves temperature assessment when the foot undergoes mechanical loading due to gait, the true accuracy of skin temperature may not be reflected [153]. However, there exist numerous monitoring tools that could be used to examine temperature anomalies of the foot plantar.

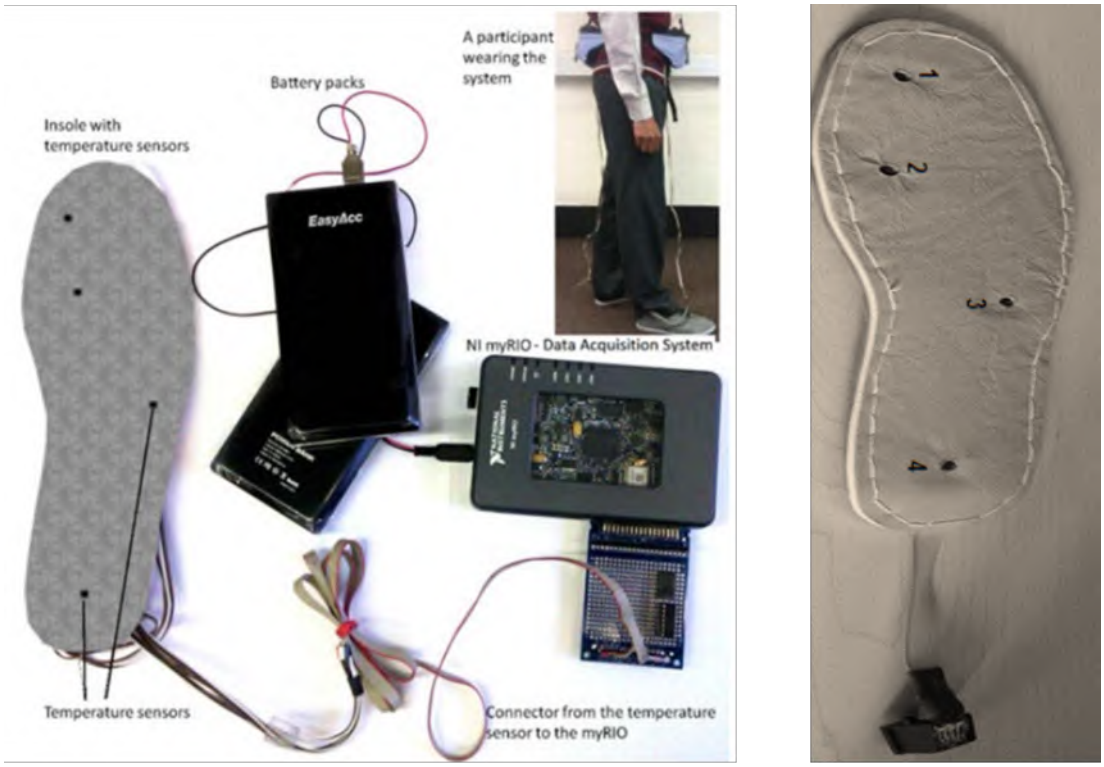
4.2.1 Conventional Methods

Conventional method of foot temperature assessment is through visual inspection followed by manual palpation as shown in Figure 4.1. Because underlying deformations can not be observed with the naked eye, proper diagnosis is problematic through this non-invasive technique [146].

4.2.2 In-Shoe Systems

These systems record the temperature of the feet continuously during dynamic activities (walking, running etc). Numerous in-shoe temperature measurement systems have been implemented by incorporating LM35D and TMP35 analog temperature sensors into shoe insoles, covering the most vulnerable regions of the feet for ulceration (Section 3.1.3.2). One major drawback of these measurements are that temperature can only be recorded at predefined regions on the foot plantar preventing asymmetric analysis using both feet. Besides, wearing shoes for a prolonged duration might elevate the temperature inside the shoe where sensors are placed. Although, dynamic temperature measurement via in-shoe systems deems controversial as discussed in Section 4.2, several prototypes have been made as shown in Figure 4.2.

Figure 4.1: Palpation of the foot plantar to diagnose PAD complications associated with diabetic foot syndrome. Image source: Stanford Medicine [154].



(a) (b)

Figure 4.2: In-shoe plantar foot temperature measurement system developed by Reddy et al. [155] and Murillo et al. [156]

4.2.3 Handheld Infrared Thermometers

This category of devices are equipped with a touch sensor to record the temperature of a single spot in skin that display the recorded temperature value digitally on an LCD display. Although it provides very little diagnostic insight, they are being used clinically owing to their simplicity to use, smaller size, lower cost [153].

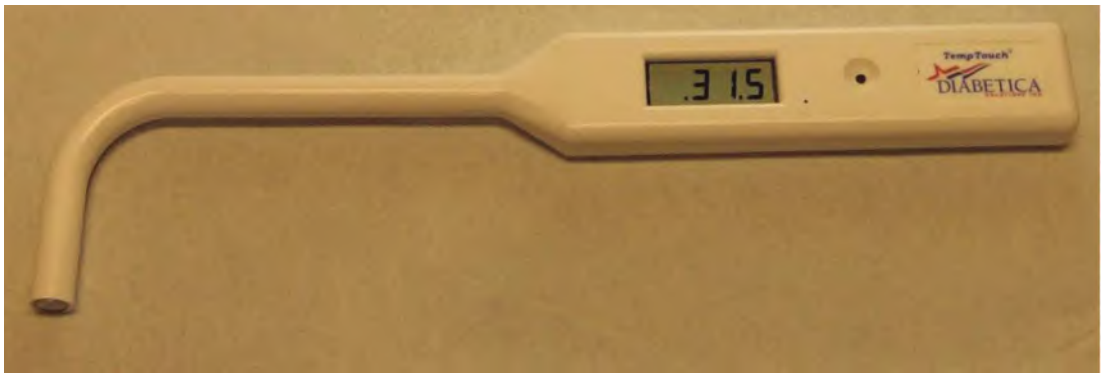


Figure 4.3: TempTouch handheld infrered thermometer used in diabetic foot assessment. Image Hazenberg et al. [157]

The flexibility offered by these systems is that, they can scan any suspicious region of the feet. However, they do not facilitate asymmetric analysis dictated by Kaabouch et al. [146]. Nonetheless, Several infrared thermometers such as TempTouch (Figure 4.3), MT4-Diabetik Footcare are commercially available and have been utilized in several research studies [157–159]. However, at the time of this review, production of the TempTouch IR thermometer has been discontinued.

4.2.4 Infrared Thermography

Infrared thermography is a process by which infrared energy (heat) emitted by an object (every object which is not at absolute zero temperature (0 Kelvin) emits infrared radiation) is used to determine the surface temperature of that object [160–162]. Thermography is gaining in popularity as a promising modality for diabetic foot complication diagnosis as it allows the measurement of surface

temperature of the measured object while visualising the heat distribution of the foot plantar [161–163] as illustrated in Figure 4.4.

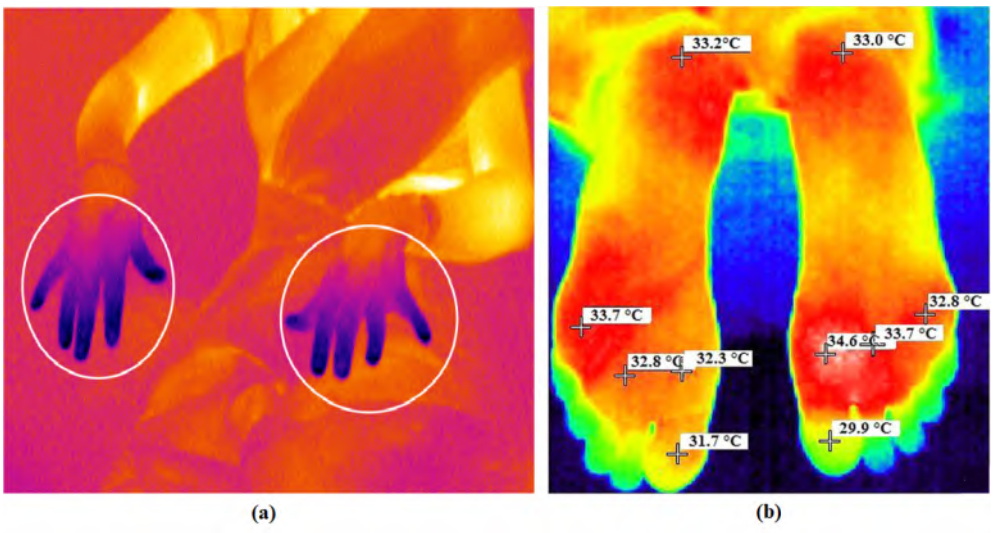


Figure 4.4: Infrared thermography technique used for measurement of PAD manifested diabetic foot complications. **(a)** Infrared thermography facilitating the visualisation of heat distribution. Temperature of the fingers are comparatively less compared to the rest of the hand. **(b)** Infrared thermography facilitating visualisation of temperature at specific locations in the foot plantar. Image sources: Bagavathiappan et al. [44] and Balbinot et al. [39]

In fact, infrared thermography has been successfully used as a clinical diagnostic tool by Bahara et al. [164, 165]. Moreover, Van Netten et.al [36] has implemented a screening tool using FLIR® thermal camera and a Canon® Eos-40D color camera. The thermal camera captures thermographic data while the color camera is used to define the contour of the foot and deduce the region of interest (ROI).

Apart from provision to conduct asymmetric analysis, infrared thermography is a non-contact measurement tool which prevent the transmission of pathological organisms when used as a screening tool [153]. Further, multiple studies have disseminated that diabetic foot complications which originate due to PAD could be detected with a high degree of specificity and accuracy at a low cost, less time with minimum technological dexterity by employing infrared thermography as a screening tool during routine clinical assessment [151, 166–169].

Figure 4.5: Experimental setup used by Van Netten et al. [151] for scanning foot plantar for diabetic foot complications

4.3 Limitations in Existing Infrared Thermography Techniques

The intent of the present study is to implement a foot plantar temperature measurement system, using NIR imaging technique, that we call "Pedothermographic system", which aids in routine clinical assessment of feet with PAD complications. One of the main limitations in the existing infrared thermography technique implemented is the thermal noise from objects captured in the frame. As the opening

with which the patient inserts the legs are kept open, thermal noise from surrounding objects are visible through the opening are captured by the thermal imaging sensor. These thermal noise becomes significantly difficult during feature detection through image processing techniques as they incorporate to foreground resulting in errors in automating the process.

Besides, the implementation by Van Netten et al. [36, 151] is comparatively larger size as shown in Figure 4.5. Moreover, vertical movement to bring the system to the same level as the patient feet is not plausible by the implementation. These hardware limitations, reduces the prospects of using the implementation by Van Netten et al for routine clinical use.

Moreover the thermal imaging camera used by Van Netten is FLIR® SC305 which costs over $ 10,000. Although, it appeals to be a valuable high end tool for research purposes, such high costs makes it a non-feasible tool for implementing a routine clinical assessment tool.

Acquired data from colour imaging sensor and the thermal imaging sensor are transmitted via Ethernet to a computer for processing and visualization. Therefore, a dedicated computer is required for the operation of the device. Hence, the high cost and hardware limitations associated with these implementations were identified and addressed by implementing a pedothermographic system using a relatively low cost yet efficient and robust thermal imaging sensor, colour imaging sensor, a processor while overcoming existing hardware limitations for routine clinical assessment.

4.4 Summary and Conclusions

The skin temperature of the foot plantar has proven to be a reliable indicator of the manifestation of diabetic foot complications related to PAD. There exist several modalities to measure skin temperature of the foot plantar. However, infrared thermography being the only modality which sanction an asymmetric analysis of the

foot plantar is by far the superior technique. The basis of infrared thermography is the use of a thermal imaging sensor to capture a thermogram of the foot plantar.

The main limitation of the use of a thermal imaging sensor is that it captures the temperature of all nearby objects focused on its lens. Therefore, capturing thermal images of the foot plantar at ambient conditions restrict the generation of thermograms with high specificity due to the presence of thermal interference. Hence, a device with a thermal camera installed inside a closed unit which isolate the feet from the surrounding objects, would significantly curtail the thermal interference. However, the proposed implementation restrict the operator from orienting the patient foot inside the covered unit. Orientation of the foot plantar is critical in the subsequent image processing during the thermogram generation. For that reason, a colour image camera accompanied by a low powered light source that could assist in orientation of the feet inside the covered unit which could be turned off during the acquisition of thermal images could be used.

In conclusion, a thermal camera, a colour image camera with a similar resolution and a LED light source embedded inside a closed unit into which feet can be extended inside, offer significant benefit over the existing techniques discussed in literature for thermogram generation.

CHAPTER 5

Pedobarographic Assessment Tool

5.1 Introduction

The overall design, the development process, performance evaluation, results of the pedobarographic assessment tool and a discussion based on the obtained results are presented in this chapter. Therefore, the key elements covered under this chapter are:

1. Selection of an effective crosstalk suppression technique (Section 5.3)
2. The novel scanning architecture implemented (Section 5.4)
3. Development and implementation of the readout circuit (Section 5.5)
4. Implementation in the Xilinx APSoC (Section 5.8)
5. GUI implementation for image visualization and analysis (Section 5.9)
6. Limitations in the present implementation (Section 5.12)

5.2 Specifications of the Piezoresisitive Sensor Array

Due to the fact that conductive polymer sheets with a conductive ink substrate has been proven to be the most efficient form of piezoresistive sensor array fabrication

technology for reasons discussed in Section 3.3, a conductive polymer sheet was custom manufactured from Sensing Tex® , Barcelona. The specifications of the fabricated sensor array are given in Table 5.1 and the characteristic curve of the conductive polymer sheet sensor provided by the manufacturer is shown in Figure 5.1.

Table 5.1: Specifications of the piezoresisitive sensor array custom manufactured from Sensing Tex®

Sensor Characterisitics	**Magnitude**
Total number of sensels	30,000
Sensel Arrangement	100 rows$\times$ 300 columns
Number of sensel clusters	10
Number of sensels per cluster	3000
Spatial resolution	4 sensels per cm^2
Pitch*	5 mm
Effective sensing area	50 $\times$ 150 cm^2
Total Area	70 $\times$ 160 cm^2
Effective sensel area	6.25 mm^2
Effective resistance range	1 kΩ – 1 MΩ
Effective measurement range	1300 kPa – 1700 kPa
Response time of a sensel (90%)	$\leq$ 3 ms

* The maximum distance between two sensels is considered as the pitch

The 30,000 sensels of the piezoresistive sensor array were grouped into 10 separate clusters, each containing 3000 sensels, so that each cluster could be independently accessed to facilitate parallel data acquisition. The 3000 sensels in a single cluster were arranged into 50 rows and 60 columns which were interfaced with the row sampling electrodes and column scanning electrodes respectively. The physical architecture of the fabricated piezoresistive sensor array is illustrated in Figure 5.2.

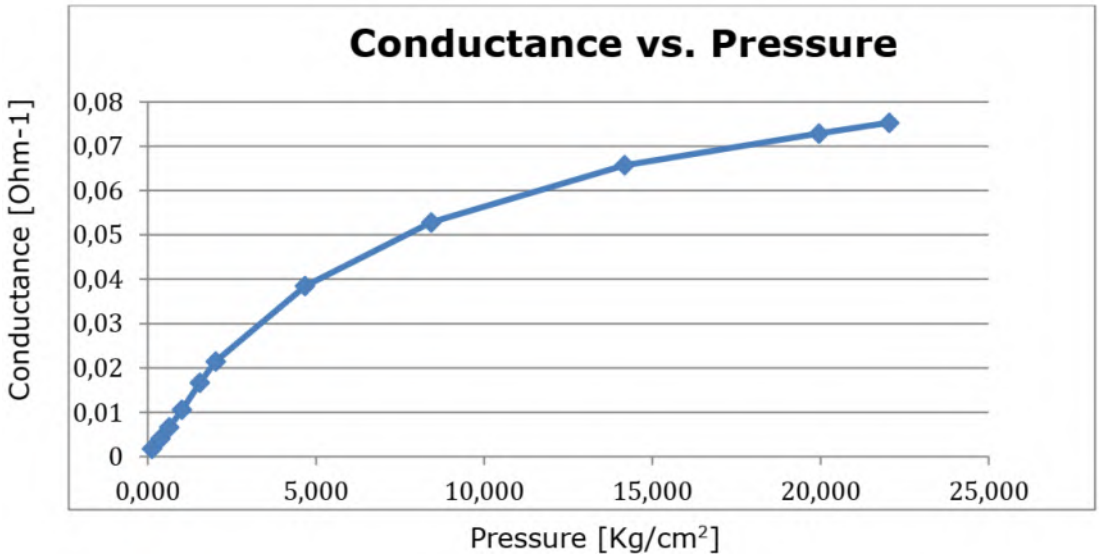


Figure 5.1: The characteristic curve of the conductive polymer sheet sensor provided by the manufacturer SensingTex®

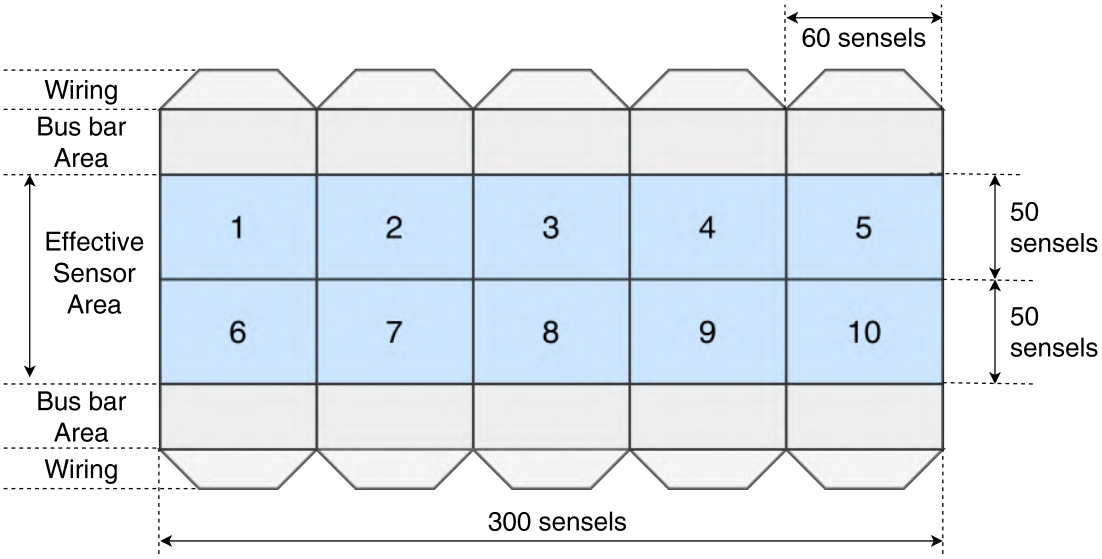


Figure 5.2: Architecture of the fabricated piezoresistive sensor array from Sensing Tex®. Sensor array is arranged into 10 clusters with 3000 sensels (50 rows × 60 columns) each which can be accessed separately

5.3 Selection of Effective Crosstalk Suppression Techniques

Although, VFM and ZPM are the most reliable crosstalk suppression mechanisms reported in recent literature, ZPM is endorsed as the most effective between the two [94, 116]. However, most of these conclusions are derived based on simulation studies and/or mathematical analyses rather than actual circuit implementations. Therefore, it was decided to conducted a pilot study to verify that ZPM is indeed the most effective among the two.

Since there were six different ways to implement ZPM and VFM based crosstalk suppression, the two most basic types of ZPM and VFM based crosstalk suppression methods, S-NSE-ZP and VF-NSE were selected as they retained both non-scanned rows and non-scanned columns at ground voltage or feedback voltage respectively. As, implications existed that ZPM is better of the two, the ZPM method was implemented using type-I scanning architecture which is more error prone than type-II and type-III. Thereby, if the most error prone ZPM based crosstalk suppression performs better than VFM it could ensure that ZPM is definitely the most effective form of crosstalk suppression even in practical implementations.

A PCB which encompasses all the necessary electronics for driving an array of sensors and sampling the same array of sensors, conduct signal conditioning, signal processing and analog-to-digital conversion which result in scanning the entire array is referred to as a "Readout Circuit" [94, 102, 170]. Two separate readout test circuits were designed, based on S-NSE-ZP method and VF-NSE method to scan a resistor sensor array (RSA) of 64 elements arranged into 8 rows $\times$ 8 columns (refer Section 5.3.3).

All the components which will be used for the final circuit implementations were used in the readout test circuit developments as well, so that an overall performance estimate can be obtained even though the number of rows and columns are different. Besides, same component models were used in developing both ZPM and VFM based readout

test circuits. The list of all components used for VFM and ZPM based readout test circuits are presented in Table 5.2.

Altium Designer 19® was used for schematic design which was converted to a PCB design by appropriate placement of components, power and signal lines followed by generating Gerber files required for PCB fabrication. These PCB test circuits were outsourced to be fabricated by PCBWay®. Then, these fabricated PCBs were manually populated at the University.

5.3.1 Development of the Readout Test Circuit using the Voltage Feedback Method

The voltage feedback based readout circuit was implemented with the architecture depicted in Figure 5.3. Here, the column sampling electrodes comprised of eight resisters in voltage divider configuration, a decoder and eight 2:1 multiplexers. Hence, voltage across a given column in the resistor sensor array due to the effective resistance could be measured through the voltage divider. The measured voltage was multiplexed and passed on to an op-amp in inverting configuration (A) to record the output *(V_{out})*. The same output from the op-amp (A) was buffered through another op-amp (B) in unity gain (voltage follower) and transmitted to the decoder-multiplexer unit (of sampling electrode unit) which retained all seven non-scanned columns at the feedback voltage measured (V_f) where $V_f = V_{out}$. One input of 2:1 multiplexers were connected to the feedback voltage channel *(V_f)* from the voltage buffer while the other input was left not connected (NC). When a specific column is to be sampled, the 2:1 multiplexer connected to the corresponding column is switched to *NC* channel while retaining other 2:1 multiplexers at $_f$ as shown in Figure 5.3. This technique ensures that effective voltage feedback is supplied for all non-scanned column sampling electrodes.

The row driving electrodes consisted of a decoder, eight 2:1 multiplexers and and eight op-amps in unity gain configuration (voltage follower). The voltage buffer connected

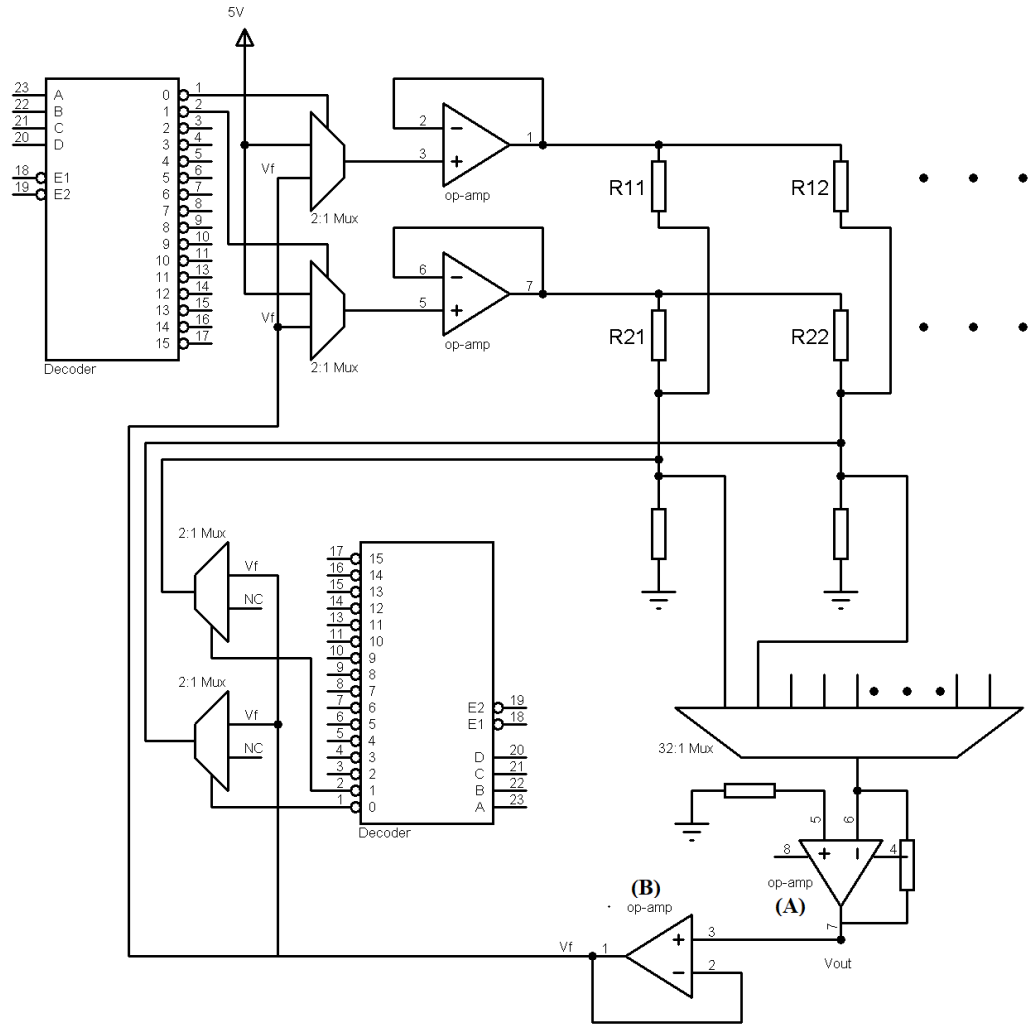


Figure 5.3: Scanning architecture of the developed voltage feedback crosstalk suppression readout circuit for pilot study on crosstalk suppression

to column sampling multiplexer (32:1 mux) was also connected to one channel of all eight 2:1 multiplexers of the row driving electrodes while the other end was connected to the driving voltage (5 V) as demonstrated in Figure 5.3.

At the time of driving a given sensor array via a decoder, the selected row by the decoder was connected to 5 V by switching its corresponding multiplexer channel to 5 V. The remaining non-scanned rows are fed with feedback voltage *(V_f)* through other multiplexer channels. Thus, all non-scanned rows and columns are retained at the feedback voltage V_f during array scanning.

The readout test circuit developed utilizing the scanning architecture described using VFM crosstalk suppression to scan the 8×8 RSA is shown in Figure 5.5 and 5.6.

5.3.2 Development of the Readout Test Circuit using the Zero Potential Method

The zero potential method based crosstalk suppression was implemented using the scanning architecture demonstrated in Figure 5.4. The row driving electrodes consisted of decoder and multiplexer system similar to the voltage feedback readout test circuit. The rows were directly switched through multiplexers satisfying the type-I scanning architecture. One terminal of 2:1 multiplexer was connected to ground while the other was connected to 5 V. All the non-scanned rows were switched to ground voltage through the 2:1 multiplexer and the scanned row was connected to 5 V.

Meanwhile, the column sampling electrodes comprised of op-amps in inverting configuration (A) which measured the voltage across a given resistor due to its effective resistance. Virtual grounding of all the non-scanned solumn sampling electrodes were done through the same principle discussed in Section 5.4.2. The measured voltage was multiplexed and transmitted to an ADC through another op-amp (B).

The readout test circuit developed utilizing the described scanning architecture using ZPM crosstalk suppression to scan the 8×8 RSA (Section 5.3.3) is shown in Figure 5.7 and 5.8.

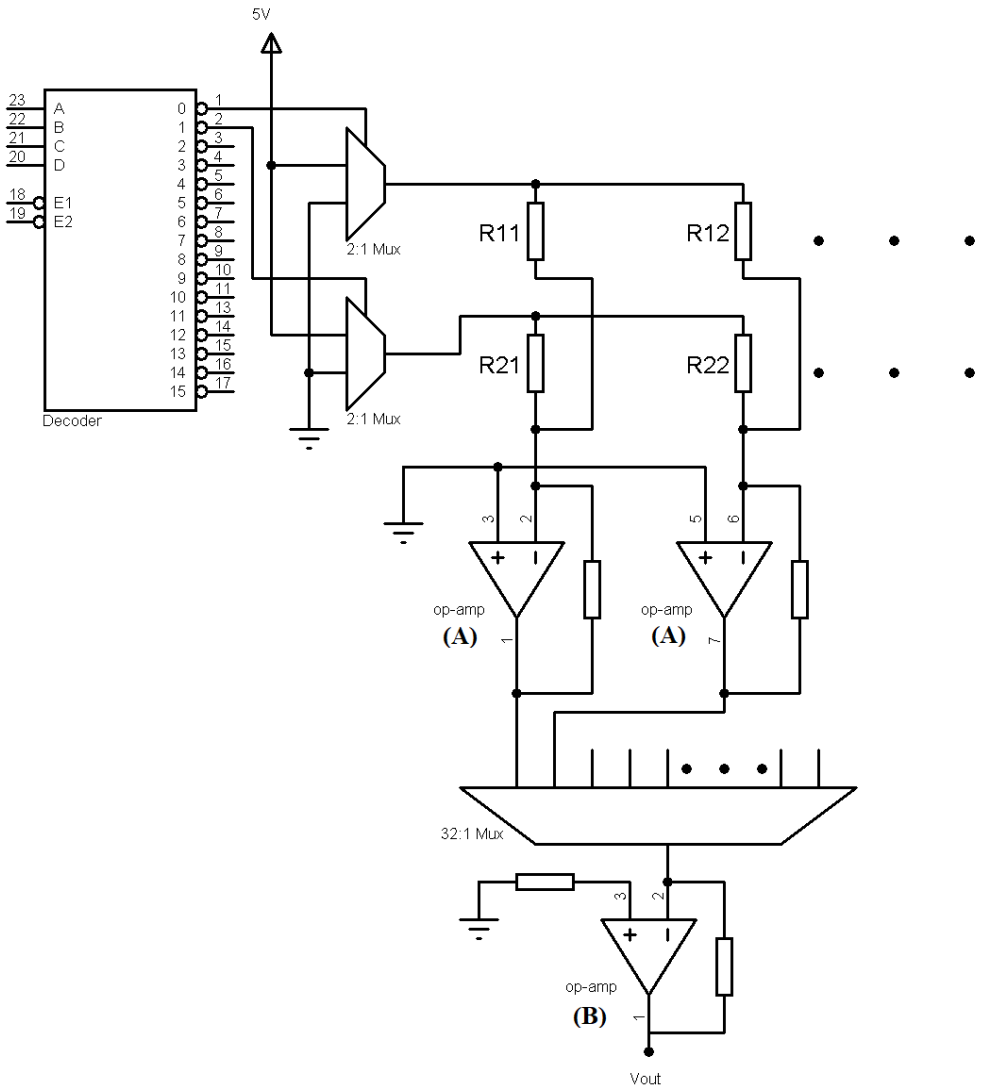


Figure 5.4: Scanning architecture of the developed zero potential crosstalk suppression readout circuit for pilot study on crosstalk suppression

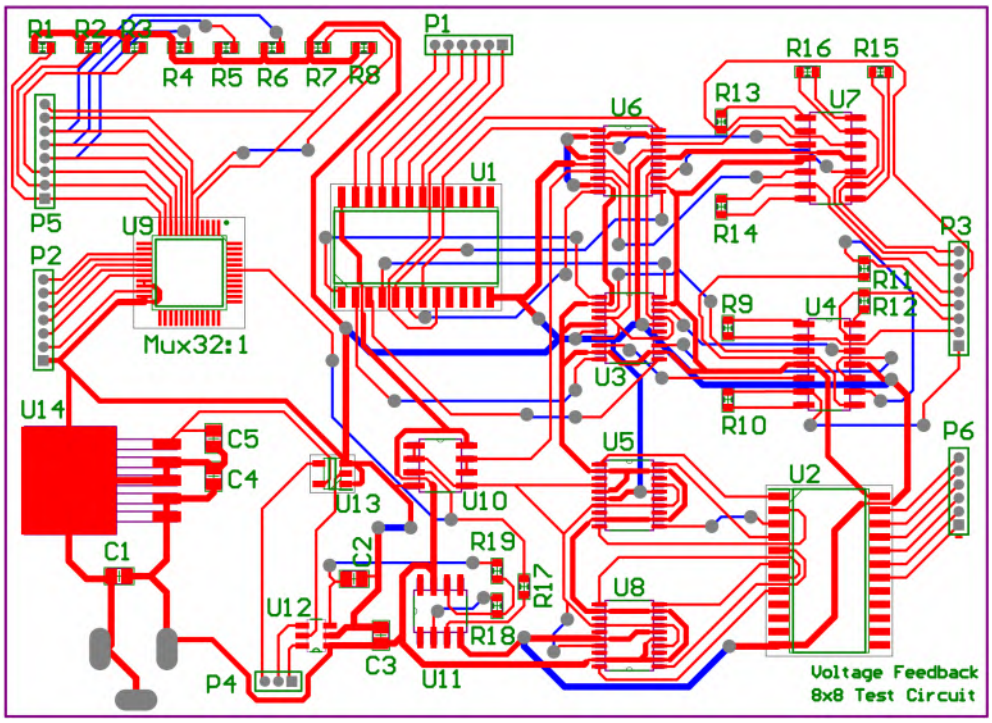


Figure 5.5: The component layout of the developed readout test circuit using VF-NSE method to scan the 8×8 RSA

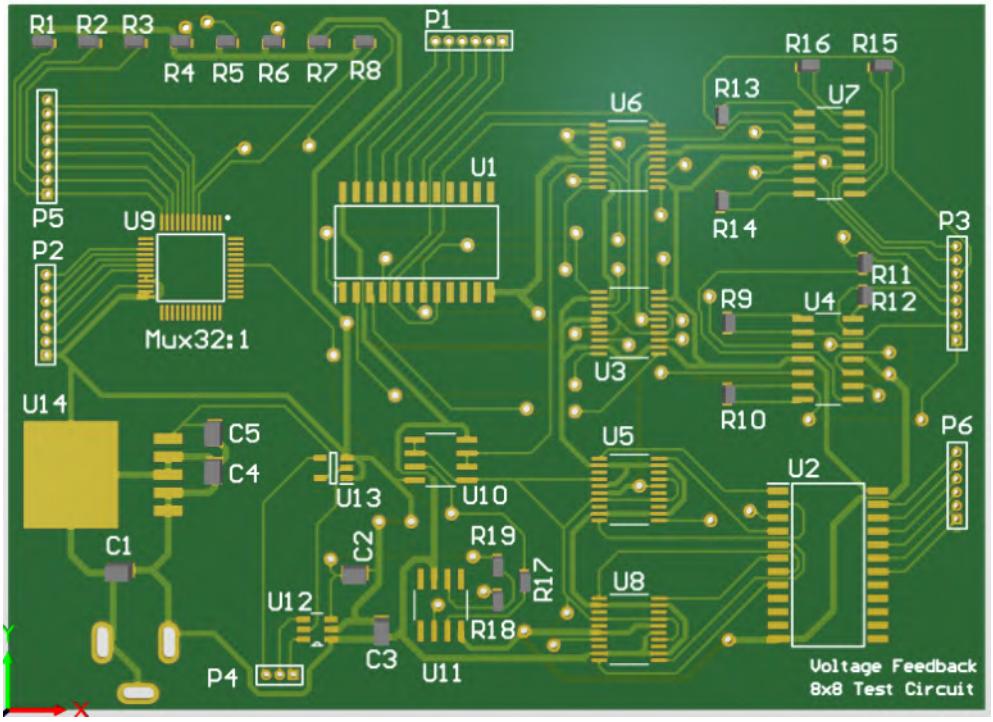


Figure 5.6: The component layout of the developed readout test circuit using VF-NSE method to scan the 8×8 RSA

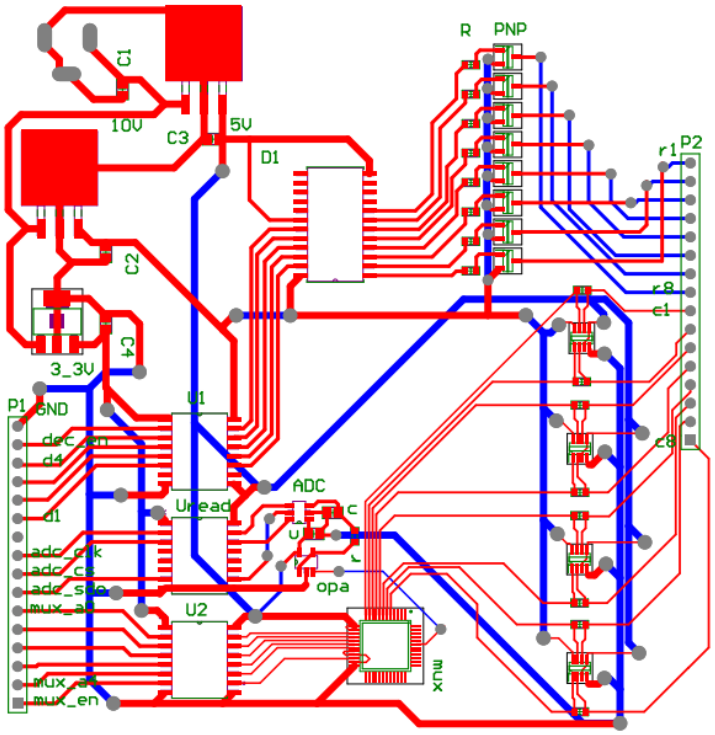


Figure 5.7: The component layout of the developed readout test circuit using S-NSSE method to scan the 8×8 RSA

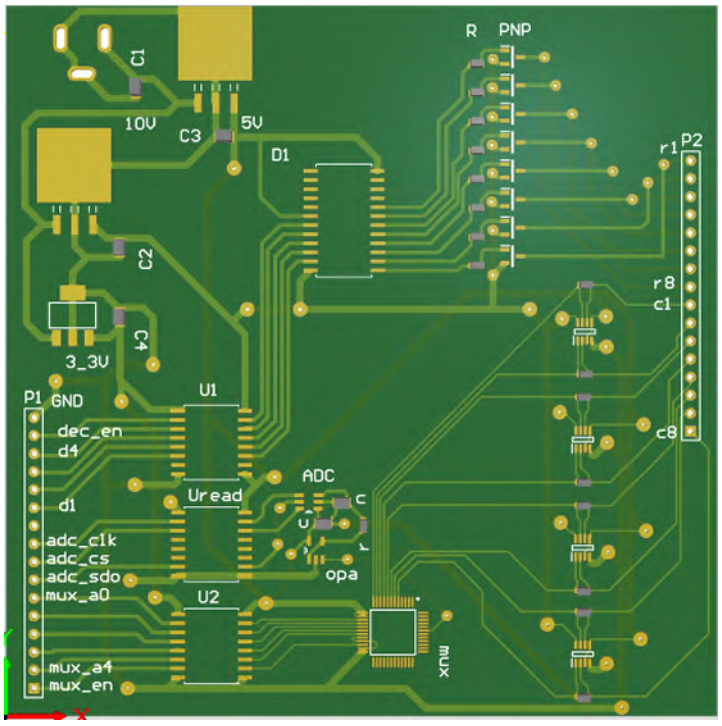


Figure 5.8: The component layout of the developed readout test circuit using VS-NSSE-ZP method to scan the 8×8 RSA

5.3.3 The Resistor Sensor Array Model Used for Evaluations

In order to evaluate the efficacy of readout test circuits developed using ZPM (Section 5.3.2 and VFM 5.3.1 and to evaluate and quantify their performance, a 8×8 Resistor Sensor Array (RSA) was developed to model with shared row-column architecture. The layout of the developed 8×8 RSA model is shown in Figure 5.9 and the realized PCB of the 8×8 RSA model is shown in Figure 5.10.

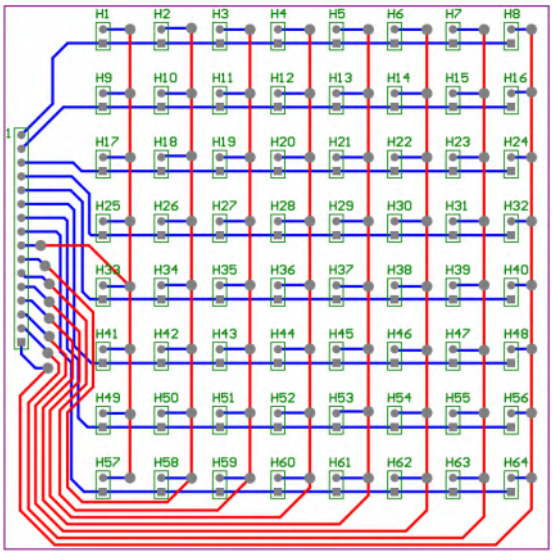


Figure 5.9: The component layout of the developed 8×8 RSA evaluate and quantify the performance of readout test circuits

Female header connectors were placed instead of sensels in the developed RSA so that fixed resistors and/or variable resistors of varying magnitudes could be mounted and desired readings could be obtained in order to quantify and obtain readings from readout test circuits. A maximum of 64 resistors could be mounted at a given time across 8 rows and 8 columns of either readout test circuit.

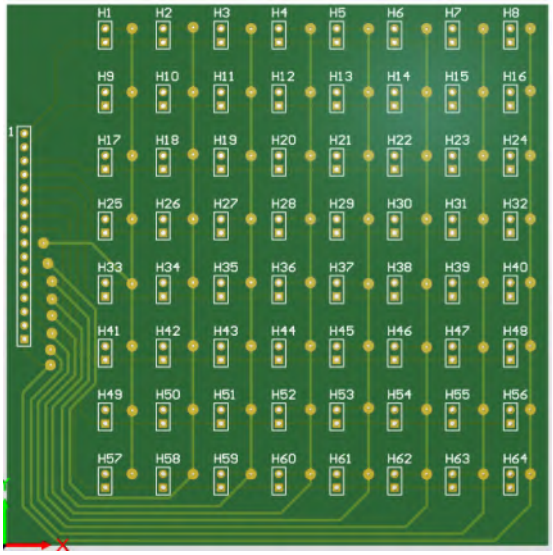


Figure 5.10: The component layout of the developed readout test circuit using VS-NSSE-ZP method to scan the 8×8 RSA

5.3.4 Evaluation Procedure of Readout Test Circuits

The thought process behind the pilot study was to connect variable resistors to all 64 slots of the 8×8 RSA model and obtain the voltage drop across a given variable resistor through the ZPM readout test circuit and VFM readout test circuit respectively. Then, calculate the expected voltage drop across the given variable resistor by dismounting it from the RSA and measuring it through a digital multimeter. The whole 8×8 array was populated with variable resistors to evaluate the impact of nearby variable resistors on the measurement through formation of parasitic parallel paths.

However, a drift in measured voltage was observed over time. Further investigations suggested that the resistance of the variable resistors changed over time. Therefore, the same process was repeated with fixed resistors by mounting them on the RSA and measuring corresponding voltage drop. By connecting resistors with different magnitudes either in series or in parallel, different resistor values were achieved which were then measured via the readout test circuits. Note that the zero resistance reading was taken by connecting a copper wire instead of a resistor at the measured location.

Based on these readings obtained, the output characteristic of both readout test circuits were generated as shown in the Figure 5.11. It was perceived from the output characteristics that the VFM readout test circuit produced corresponding voltages even when the resistance is close to zero. However, the output characteristic of VFM readout test circuit was comparatively linear compared to that of ZPM readout test circuit. However, the sensitivity of the readings (dv/dΩ) from VFM readout test circuits declined with increase in resistance whereas that of ZPM readout test circuit improved with increase in resistance. Given that the fabricated piezoresisitive sensor array has a measurement range of 1 kΩ –1 MΩ, and typical foot plantar pressure measurement falls between 1 kΩ –10 kΩ range, precedence was given to increased sensitivity at higher resistance values over linearity, as the ultimate goal was to improve accuracy of readings.

Besides, the cost of components (bill of materials) for the VFM readout test circuit was 38% higher than that for the ZPM readout test circuit. This experiments reflects that the ZPM readout test circuit is superior to the VFM in sensitivity, span, cost and complexity of implementation whereas VFM readout test circuit is only superior in linearity. Therefore, considering all these, it was concluded that the ZPM is more suitable for the implementation than VFM for the present implementation.

5.4 The Novel Scanning Architecture

This section outlines the main components of the readout circuit that was developed upon the conclusion of the Section 5.3.4 where ZPM based scaaning architecture was given precedence. The row-driving electrode system, column sampling electrode system and the mechanism of scanning using the proposed row-driving electrode system and column sampling electrode system are discussed in the subsequent sections.

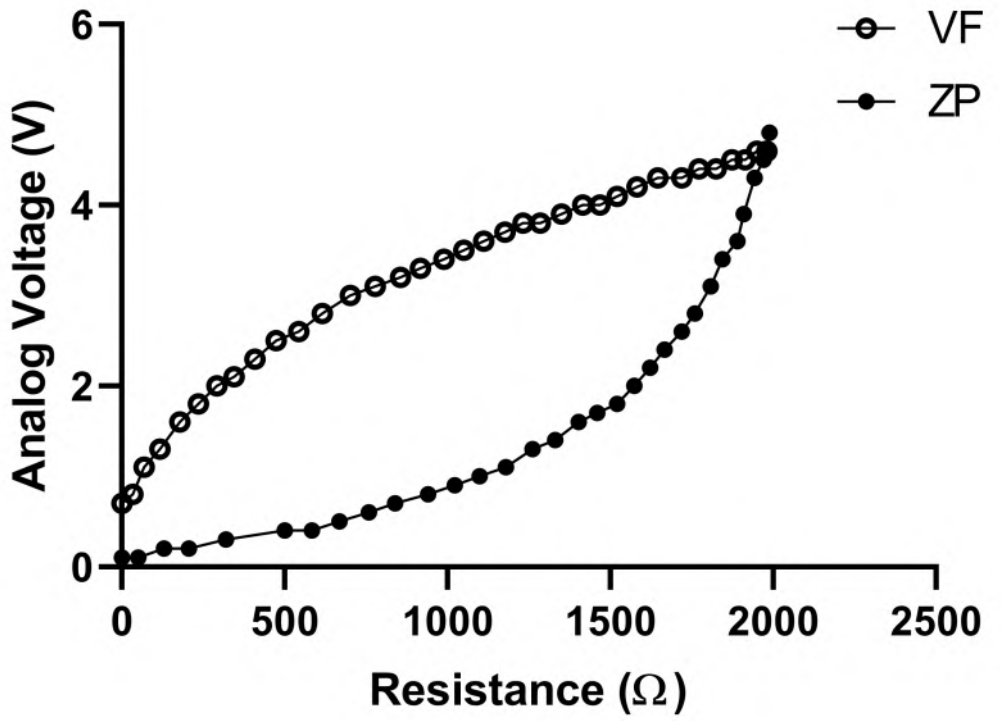


Figure 5.11: The output characteristic for the readout test circuits with ZPM and VFM crosstalk suppression respectively

5.4.1 Row Driving Electrode System

Kim et al. [116] proposed an improvement to the type-II scanning architecture which was the most accurate of the two scanning architectures that existed for sensor array scanning with zero potential crosstalk suppression as discussed in Section 3.9. He showed that this newly proposed type-III architecture could achieve the same accuracy with seemingly lesser number of op-amps. Therefore, the scanning architecture was modeled based on the type-III architecture. Without directly adopting it, several improvements were made to the type-III systems to facilitate large sensor array scanning as listed below.

1. Replaced energy-inefficient row driving op-amp with high frequency operational active low decoder

2. Replaced physical switches with more efficient transistor switches that consume less power and has negligible ON resistances

3. Replaced the dedicated ADCs attached at each column with a high frequency multiplexer and a single ADC for all columns in a cluster

4. Placed proper AA filters and voltage buffers along the signal conduction path

The inaccuracies associated with an op-amp driving the row driving electrodes through a series of physical switches was slightly altered. The op-amp in the type-III architecture was replaced with an active low decoder to drive the switches. In place of physical switches, PNP transistors were used as switches by biasing them in cut-off and saturation regions to turn them OFF and ON respectively. As decoders are based on digital logic, it is easier to interface them with the controlling unit and are less prone to external interference compared to an op-amp which operates on analog logic. ON resistance of the digital buffer which is one of the major drawbacks in the type-I architecture barely has any significance in the proposed model as the driving voltage (V_{Drive}) to the rows are provided directly through transistors as shown in Figure 5.12. Therefore, rows of the sensor array are not directly switched through decoders. Given that the ON-resistance across a transistor is rather negligible, a sufficient voltage drop to induce errors do not fall across them.

5.4.2 Column Sampling Electrode System

Op-amps are the most efficacious column sampling electrode system developed to date. All type-I, type-II and type-III systems adopt the same principle of column sampling using op-amps in inverting configuration (Section 3.9). The reason being, in an ideal inverting op-amp, there exist no potential difference between the inverting terminal and the non-inverting terminal [171]. As a result, the inverting terminal is virtually grounded though non-inverting terminal. Therefore, the non-scanned columns are retained at the virtual ground voltage through this unique property of

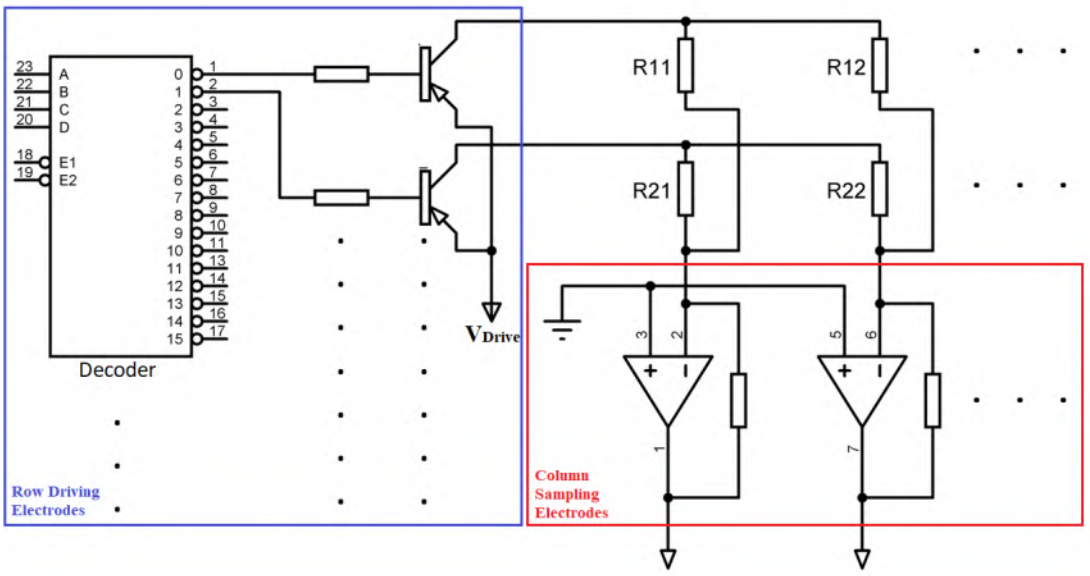


Figure 5.12: The modified type III scanning architecture using a decoder-transistor system

op-amps [127].

However, practical op-amps present non-ideal characteristics which shackles the integrity of the ZPM mechanism. However, a substantial crosstalk suppression can be achieved through restraining the non-ideal characteristics to a minimum. Presence of the offset voltage between the inverting and non-inverting terminals of the op-amp means that the virtual ground is not be present on the inverting terminal. Nevertheless, selecting an op-amp with a very low offset voltage was a primary concern when designing the sampling electrodes. Moreover, stability of the op-amp at unity gain is also an essential design constraint to warrant the operation is free of oscillations [172]. In addition, high Gain Bandwidth Product (GBW), high slew rate, low power consumption and rail-to-rail output contribute towards stable operation of the op-amp. Therefore, by selecting an op-amp adhering to these constraints ensure that effective ZPM based crosstalk suppression is achieved.

5.4.3 Mechanism of Scanning

The scanning mechanism of the sensor array using the improved type III architecture (decoder-transistor system) can be outlined as follows.

When the active low decoder receives an input signal from the controller (AP-SoC based Xilinx Zynq APSoC device), it switches one output pin LOW depending on the combination of the input, provided that the decoder has been enabled by the controller. As one decoder output pin gets LOW, the corresponding PNP transistor which is connected to it is driven to saturation. The PNP transistor functions as a high-side switch. A high-side switch configuration is when the load is connected across the ground and the collector terminal of the transistor (transistor is connected to the high side [V_{cc}] of the load) as shown in Figure 5.13. When the transistor saturates, it connects V_{Drive} to the corresponding row (load) connected to its collector terminal (output).

When a row is activated, all the column sampling electrodes are enabled incrementally by the control signals issued by the controller device. Once all the column sampling electrodes are transversed, the subsequent row will be switched through decoder-transistor system. This process repeated until all the rows are transvered to generate one frame.

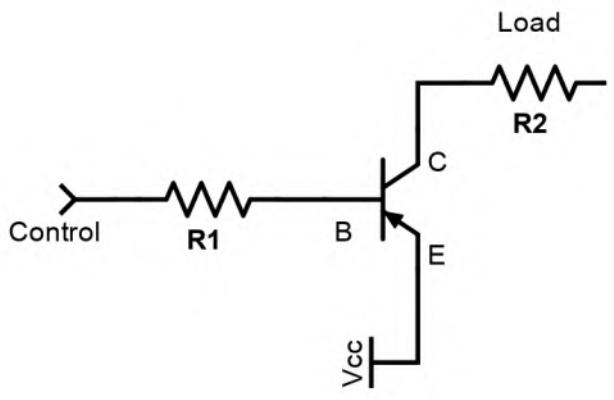


Figure 5.13: High side switch configuration used in the row driving electrodes

5.4.4 Mechanism of Zero Potential Crosstalk Suppression in the Decoder-Transistor Architecture

On the basis of Wu et al. [102] who demonstrated through a series of simulation studies that all three ZPM crosstalk suppression techniques are effective in crosstalk suppression compared any form of VFM, followed by the verification at the hardware level, the investigation was extended into the most appropriate ZPM crosstalk suppression technique out of the existing three. After iterating through the three main types of zero potential based crosstalk suppression techniques, S-NSSE-ZP method was chosen as the most formidable crosstalk suppression technique for our intended application. Besides, S-NSSE-ZP technique demanded the minimum resource requirement and minimum power consumption compared to other two techniques [94, 102].

The mechanism of scanning is such that, when a particular row is being switched ON through a PNP transistor in saturation region (Figure 5.14), V_{Drive} falls across that row as explained in Section 5.4.3. However, the remaining PNP transistors connected to non-scanned rows operate in cut-off region. As illustrated in Figure 5.14, both collector current (I_C) and base current (I_B) of the transistor are zero during cut-off mode of operation. Therefore, theoretically, there will be no currents flowing toward the rows, thus, formation of parasitic parallel paths is prohibited. As a result, non-scanned rows are retained in a floating state rather than at virtual ground because they are not directly connected to the ground unlike in the case of S-NSE-ZP method which was adopted for readout test circuit development as shown in Figure 5.4.

On the flip side, column sampling electrodes (op-amps in inverting configuration) connected to non-scanned columns are theoretically retained at virtual ground owing to the lack of offset voltages between inverting and non-inverting terminals of the op-amps as described in Section 5.4.2.

Although, both row driving electrodes nor column sampling electrodes induce any by

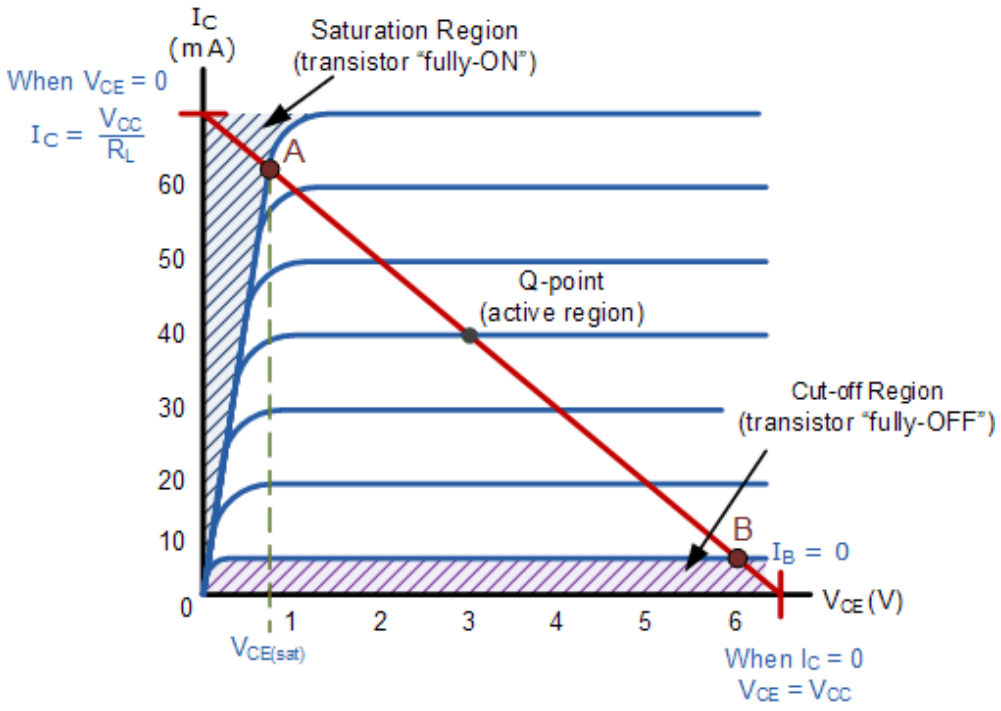


Figure 5.14: Operating regions of a transistor. Image Source: Electronic Tutorials [173]

pass currents to the non-scanned sensor array theoretically, non-ideal characteristics of both electrode systems discussed in Section 5.4 may induce bypass currents forming parasitic parallel paths. However, through effective component selection, and careful circuit design, these undesired characteristics could be contained. Therefore, in the proceeding sections, initiatives taken will be discussed to realize the sensor array scanning based on the proposed decoder-transistor architecture followed by an in depth performance evaluation quantitatively and qualitatively verify the accuracy of the realized architecture in terms of the measurement accuracy and the shape accuracy.

5.5 Development of the Readout Circuit for Scanning of the Piezoresistive Sensor Array

As discussed in Section 5.3, any readout circuit, within the context of sensor array scanning, comprises of a row driving electrode system, column sampling electrode system, analog to digital conversion unit and related supplementary electronics. Therefore, the developed readout circuit comprised of decoder, PNP transistor based row driving electrodes and op-amp based column sampling electrodes.

Seeing that the piezoresistive sensor array consisted of 30,000 sensels arranged into ten clusters of 3000 sensels each, one readout circuit was devised to scan two clusters simultaneously to reduce the overall silicon area occupied by components and reduce the resource utilization through sharing of components. Thereby, a total of five readout circuits are required to scan the overall piezoresistive sensor array. A structural overview of the readout circuit designed to scan two clusters of the piezoresistive sensor array is shown in Figure 5.15.

The path transverse by a signal that enters the readout circuit from the APSoC device through isolators transverses row driving electrodes, the piezoresistive sensor array, column sampling electrodes, signal conditioning unit, ADC and back to the APSoC device as shown in Figure 5.16.

Altium Designer® 19 was used for schematic design which was converted to a PCB design by appropriate placement of components, power and signal lines followed by the generation of Gerber files required for PCB fabrication. Thus deigned PCB test circuits were outsourced to be printed (fabricated) by JLCPCB®. PCBWay® were comparatively inexpensive in fabricating smaller PCBs while JLCPCB® was cheaper in fabricating larger PCBs. The fabricated PCBs were manually populated at the University through soldering.

Figure 5.16 demonstrates the path transverse by a signal that enters through the input

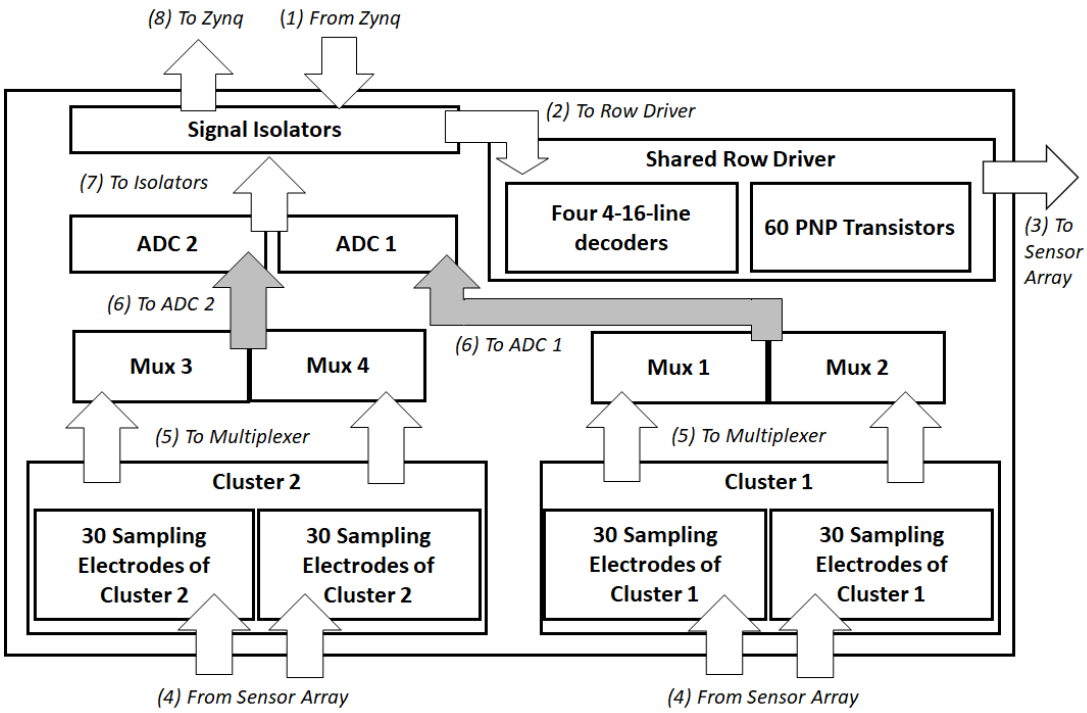


Figure 5.15: The structural overview of the readout circuit designed to scan two clusters of the piezoresisitve sensor array simultaneously. The signal pathway in the readout circuit is in the order of numbering used. Therefore, signal which enters the readout circuit from the APSoC device through signal isolators transverses the shared row driving electrodes, the piezoresisitive sensor array, which are acquired back by the separate column sampling electrodes for each cluster and then to a multiplexer through to ADC and back to the APSoC device through signal isolators. A signal conditioning unit comprising of an anti-aliasing filter, voltage buffer and a low pass filter at the input stage of the ADC is used which is depicted by the grey arrows

and exits through the output of the readout circuit. Separate blocks of this signal path will be described from Section 5.5.1 onward.

5.5.1 Signal Isolators

Signal isolators were placed at the interface between the readout circuit and the controller (Xilinx Zynq APSoC device) to isolate both input and output signals to and from it as shown in Figure 5.15. Decoder address input, multiplexer address input,

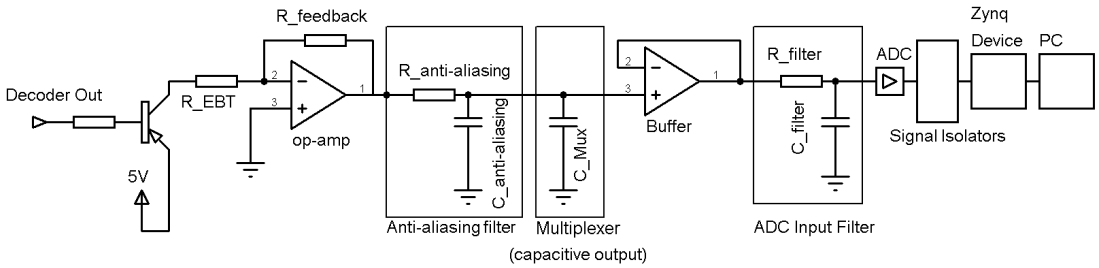


Figure 5.16: Path followed by signal from the decoder all the way to the PC through a Xilinx Zynq APSoC device is illustrated here. Decoder receives address information from its four binary weighted inputs which activates a given row through a bias resistor and transistor. At the same time, the corresponding multiplexer of the desired cluster is enabled by the APSoC device. Multiplexer then read the corresponding op-amp in the column sampling electrodes. The signal transverses through the anti-aliasing filter before reaching the multiplexer which has a capacitive output. Then the signal transverses a voltage buffer followed by a low pass filter and reaches the ADC. Digitized signals then reach the APSoC device through signal isolators and final reaches a computer

chip enable control signals were transmitted from the APSoC device to the readout circuit while ADC output from each cluster were taken as the only input to the APSoC device from the readout circuit. Purpose of accommodating signal isolators was to ensure protection for the controller from transient voltage fluctuations that may arise in the readout circuit. After a careful investigation, capacitive CMOS digital isolators were selected over optocouplers for their superior performance, reliability and ease of implementation [174]. Therefore, SI8660BA-B-IS1 one-way isolators and SI8662BB-B-IS1 two-way isolator were incorporated in the design.

5.5.2 Row Driving Electrodes

Since the 3000 sensels in a cluster are arranged into 50 rows and 60 columns (Table 5.1), 50 PNP transistors, 50 biasing resistors (connected between decoder and transistor) and a decoder with 50 or more output pins were required for each cluster.

However, these 50 row driving electrodes were shared between two clusters such that they drive the rows of two clusters at once. In order to generate a unique output signal to drive a given row, decoder should cater 50 output pins.

Therefore, NSS40200LT1G PNP transistors which are capable of driving currents upto 2 A, with base currents as low as 20 mA and low saturation voltages were selected for the row driving electrodes. Four 74HC154 4-to-16 line active low decoders with a maximum current drive of 20 mA were selected to access all the rows in a given cluster (16 unique outputs from 3 decoders + 2 unique outputs from the last decoder).

5.5.3 Column Sampling Electrodes

Two sets of column sampling electrodes comprising of 60 op-amps each were arranged separately to read each column of two clusters simultaneously as shown in Figure 5.15. Selection of op-amps were critical for the operation of the entire readout circuit as inverting op-amps induced the zero potential states for the non-scanned column sampling electrodes. Hence, all the criteria on op-amp selection discussed in Section 5.4.2 were considered and finally OPA2810 was selected as the main op-amp of the column sampling electrodes.

5.5.4 Multiplexer Unit

In literature, signals acquired by the column sampling op-amps were directly transferred to the analog to digital conversion unit which comprises of a dedicated ADC for each column of the sensor array [94] which is rather non-feasible for scanning of large sensor arrays. Hence, this mechanism was modified in such a way that the acquired signals through op-amps were multiplexed at higher frequencies to a dedicated ADC for each cluster, thus, lowering the number of ADC required from 300 down to 10.

In order to multiplex 60 channels for all the columns in a cluster it was necessary to use two 32:1 multiplexers. 30 input channels of each multiplexer was connected to 30 op-amps of the column sampling electrodes and the two multiplexers operated sequentially to multiplex acquired data from all 60 column sampling op-amps to the ADC.

CMOS ADG732 multiplexer with an ON-resistance of 4 Ω were used to sequentially switch 30 column sampling electrodes. Sequentially increasing address values were transmitted from the APSoC device to the multiplexer and appropriate channel was select by the multiplexer accordingly. Moreover, first 30 sampling electrodes of the two clusters connected to the readout circuit were designed to be scanned simultaneously. Hence, Mux 1 (cluster 1) and Mux 3 (cluster 2) operated concurrently while Mux 2 (cluster 1) and Mux 4 (cluster 2) operated concurrently as demonstrated in Figure 5.15.

5.5.5 ADC Unit

As discussed in Section 3.6, a sampling rate of at least 200 Hz is required to facilitate both dynamic and static measurement of foot plantar pressure. Moreover, the maximum attainable scanning frequency from the piezoresistive sensor array is 300 Hz (Because the response time is 3 ms as indicated in Table 5.1). Therefore, high resolution, high sampling rate, low cost, low power consumption and high accuracy were the parameters considered when selecting the op-amp. Upon a careful selection process, 12 bit 1-MSPS (Mega Samples Per Second) Successive Approximation Register (SAR) based ADS7886 was selected.

5.5.6 Signal Conditioning Unit

Anti-Aliasing Filter

In order to achieve a 1-MSPS sampling rate, the ADC input should receive data at 500

kHz or lesser according to the datasheet. Hence, a 500 KHz anti-aliasing (AA) filter was required at the input stage of the ADC. However, implementing the AA filter at the output stage of the multiplexer (input stage of the ADC) would result in loss of information related to measurement. Therefore, the AA filter was shifted to the input stage of the multiplexer (Figure 5.16). When placing the AA filter at input stage, the frequency should be $1/30^{th}$ of the frequency if it were to be placed at the output stage. Reason being the multiplexer input channels acquire signals from 30 columns (500 kHz$\div$30 =16.67 kHz). However, the maximum frequency with which the resistance of the piezoresistive sensor array can vary without inducing measurement errors is 300 Hz (Table 5.1).

Therefore, the circuit was initially designed with a 300 Hz AA filter so that no aliasing happens to the input signal while achieving band limiting of the signal, which prompted the use of physically large resistors and capacitors to implement a passive AA filter with such a low cut-off frequency. The RC component acts as a resistive and capacitive load as seen by the op-amp when the AA filter is placed at the output stage of the op-amp. Although a large resistor, which also acts as a dampening resistor lessen the capacitive load, placing a large capacitor in the readout circuit posed the risk of inducing thermal noise which prompted us to use a moderate resistor and a capacitor of 820 Ω (R_anti-aliasing in Figure 5.16) and 1 μC (C_anti-aliasing in Figure 5.16) respectively for the final circuit implementation which set the cut off frequency at 194 Hz which theoretically proved to be adequate to the current application.

Voltage Buffer and Low pass filter

The selected ADC, ADS7886 required a low impedance source to facilitate optimum operation. Therefore, a voltage buffer and subsequent low pass filter was embedded at the input stage of the ADC. It is implemented as shown in Figure 5.16.

5.5.7 Power Supply to the Readout Circuit

For the optimum operation of the selected components of the readout circuit, well-regulated, bypassed supply of power is critical. In order to establish zero potential condition using the readout circuit, a dual rail power supply was needed to supply voltage within the – 5 V to + 5 V range. As a Switch Mode Power Supply (SMPS) when used alone subjects the power line to switching noise, Linear Dropout Regulators (LDOs), low pass power line filters were placed as shown in Figure 5.17. Moreover, low equivalent series resistance (ESR) bypass capacitors were placed close to the V_{CC} and GND pins of the IC components to act as charge banks to prevent them drawing surge currents which may result in oscillations in the power supply [127].

The Table 5.2 summarizes the list of all major components used for the implementation of the readout circuit. Preference was given for SMD packages of the ICs and all the passive components (resistors and capacitors) during component selection.

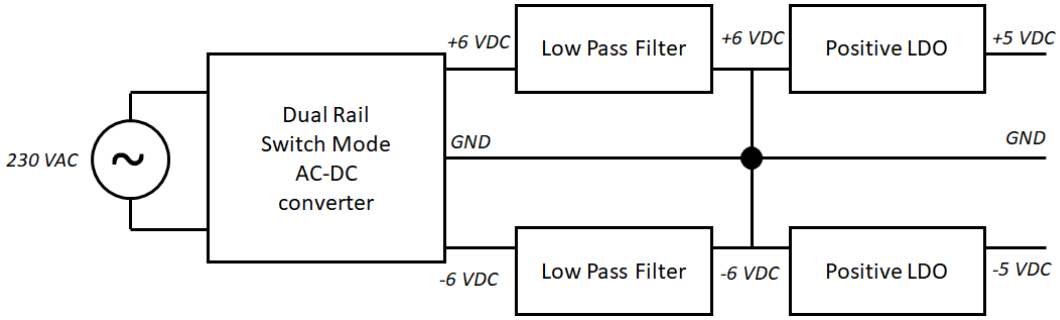


Figure 5.17: The composition of the power supply designed to supply power to the readout circuit

The final physical layout of the final readout circuit which simultaneously scans two clusters with a shared set of row driving electrodes, implemented using all the selected components and strategies is shown in Figure 5.18.

Table 5.2: Summary of the Selected Components for the Readout Circuit

Component	**Desired Features**	**Reason for the desired feature**	**Selected IC**
Decoder	Active Low output	Reduce errors due to interference (noise)	74HC154
	Higher number of output pins	Need to drive higher 50 rows	
PNP transistors	Low saturation voltages	Less voltage error during ON state and less voltage drop across switch	NSS40200LT1G
	Drive high currents (up to 2A)	Low resistive load	
	Quick switching (ns range)	Improve circuit response	
	High side switch	Decoder has active low output	
Op-amp	Stable at unity gain and High gain bandwidth product	Prevent oscillations	OPA2810
	Low offset voltage	Reduce measurement error	
	High current sinking and sourcing ability	High currents are involved in the circuit due to low resistance	
Multiplexer	Low ON resistance	Reduce error (less distortion)	ADG732
	Higher I/O pins	Need to read higher number of pins	
Voltage Buffer	Buffer ADC input	Prevent loading the source	OPA365
ADC	Higher sampling rate	Higher number of column data	ADS7886

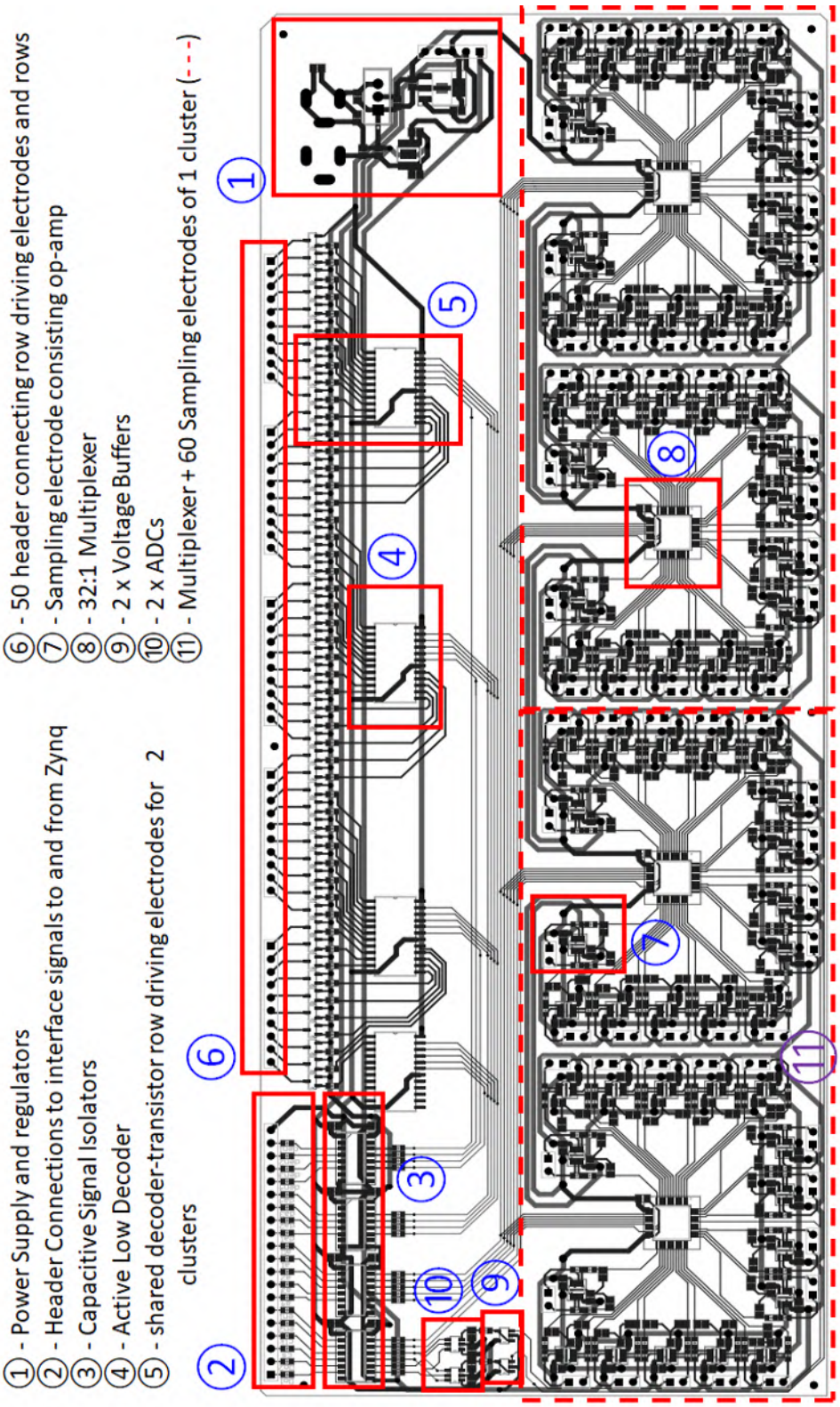


Figure 5.18: The physical layout of the implemented readout circuit

5.6 Design Considerations when Designing PCB

The PCB layout of the readout circuit was designed using hierarchical schematic design facilitated by Altium PCB design tool. This enabled designing the whole PCB across several sheets by accumulating components that undertake a given functionality together. Moreover, the readout circuit designed to scan two clusters simultaneously, accommodate over 700 components among which some groups of repetitive components delivered the same functionality such as column sampling electrodes and row driving electrodes. Therefore, multi-channel designing provided via the hierarchical design architecture of Altium proved to be invaluable to implement repeated functionality by reusing given sets of components, interconnections and nets. Therefore, 30 column sampling electrodes were were implemented by multi-channeling around one multiplexer so that all 60 column sampling electrodes are implemented around the two multiplexers for a given array.

Several design optimisation techniques were incorporated following the IPC-2221 standards [175] in order to ensure the proper functionality of the designed readout circuit at high frequency operation. Control signal lines were placed equidistant with each other with a trace clearance of 0.25 mm with equal lengths and widths. Moreover, a minimum umber of vias of equal dimensions were used in the PCB. Bypass capacitors were placed very close to power supply pin of components to limit the effect of current transients during switching while granting AC noise signals a low impedance path for ground. Series damping resistors were placed near the source to eliminate ringing and lowering the Q-factor.

5.7 Design Validation of the Developed Readout Circuit

Implementation of readout circuits with improved scanning techniques should always be proceeded with effective evaluation techniques to determine that the performance of the implementation is satisfactory. Therefore, Wu et al. [102] categorized existing evaluation techniques for readout mechanisms into three main categories as listed below.

1. Analyse the readout circuit with the actual sensor array at the hardware level [107, 176]
2. Analyse the circuit model with circuit simulations at the software level [93, 94, 99, 100, 114]
3. Analyse the readout circuit with a test model [101, 107, 117, 118, 177]

Intuitively, technique 1. above yields the most accurate performance analysis for the readout circuit implementation at the expense of high cost and extensive manual work [102]. However, almost all the analysis via technique 1. have been conducted for smaller sensor arrays of dimensions not greater than 4×4 [176]. Besides, the whole analysis is based on the assumption that the sensor array is free of manufacturing errors and operates under optimum conditions. When the resistivity of the different resistors were measured manually by connecting multimeter terminals across different rows and columns of the sensor array, the resistance measurements appeared to be non-uniform. Therefore, the true performance evaluation of the readout mechanism cannot be inferred with the actual sensor array [127]. As a result, technique 1. is seemingly non-feasible even for a large sensor array cluster with 3000 sensors.

Software based circuit simulations have been conducted extensively in literature to evaluate new circuit designs and implementations using analysis tools such as PSpice,

NI Multisim and Cadence Spectre [102]. These tools have effectively been used to quantify power consumption and measurement errors associated with a given readout mechanism. Although, Wu et al. [102] reports that the results are consistent, errors at hardware level such as interference, circuit path resistance etc. are not considered during simulation analysis. Therefore, circuit simulations alone is not a preferable validation tool.

Mathematical test models have also been proposed and implemented to assess the accuracy of a developed readout circuit. They are based on the principle that sensels of a given zone behaves identically in a uniform sensor array. Although they offer significant value when designing readout circuits, similar to the circuit simulations, mathematical test models do not present the true nature at the hardware level. However, Kim et al. [116] validated his readout mechanism through a hybrid approach of using circuit simulations and a 4×4 RSA model (Section 3.8. He showed that the measurement error between simulated measurements and actual measurements form the RSA model are less than 1%. As this method provides a better realistic estimation of the readout circuit performance than the conventional methods, a similar methodology was adopted for validating the readout circuit that was developed.

As initial tests with the real piezoresistive sensor array failed due to non-idealities present in it, the 8×8 RSA model was used to validate the voltage feedback and zero potential readout test circuits (Section 5.3.3). Using a RSA model onto which fixed resistors could be mounted proved invaluable when evaluating the effect of crosstalk suppression and the impact of non-scanned sensels on the EBT reading from the readout circuit.

The manufacturer of the piezoresistive sensor array SensingTex® had disclosed that the effective resistor range for plantar pressure measurements is 1 kΩ – 12 kΩ. Therefore, fixed resistors with a tolerance $\pm 1\%$ within the resistor range of 1 kΩ – 12 kΩ were selected. Resistances above 10 kΩ were created by connecting selected fixed resistors in series. As discussed in Section 3.7, the degree of crosstalk suppression

could be quantified using the measurement accuracy and the shape accuracy attainable from the implemented scanning mechanism. Therefore, two separate experiments were devised to evaluate the measurement accuracy and the shape accuracy of the developed readout circuit.

5.7.1 Derivation of the Transfer Function of the Developed Readout Circuit

In order to determine measurement accuracy of the readout circuit, first the transfer function of the readout circuit had to be derived. The transfer function conveyed the relationship between the readout circuit input and the output. The effective resistance experienced by the measured sensel which is reflected as a voltage signal is the input to the readout circuit while the ADC reading which is transmitted out of the readout circuit becomes the output.

In pursuance of determining the true relationship between resistance of RSA sensels and the corresponding ADC reading, the effect of crosstalk had to be completely negated. Reason being, the true correspondence between the input and output is obtained had non-scanned sensels induced any crosstalk interference on the measurement. Therefore, a crosstalk free environment had to be simulated in the RSA. Because crosstalk is by definition the formation of parasitic parallel paths as a result of the nearby non-scanned sensels, crosstalk in the RSA were eliminated intuitively by taking measurements in the absence of any non-scanned sensels.

Therefore, resistance of different fixed resistors within the measurement range of 1 kΩ – 12 kΩ were inserted into a specific sensor location (row 1, column 1) and ADC readings were recorded. The ADC readings were directly transferred to the computer from the APSoC device through UART. By utilizing Tera Term terminal emulator the ADC readings were recorded and visualized. Five different resistor types for measurements were selected including 1.5 kΩ, 2.4 kΩ, 3 kΩ, 6.5 kΩ and 9.1 kΩ expanding the desired measurement range. These resistors were mounted in series

and/or parallel at the measured sensel location to induce different resistance values as input. Ten readings were taken from different resistors of the same rated magnitude to eliminate component bias. Upon covering the entire measurement resistance range a non-linear regression analysis was conducted using SPSS version 23 to estimate the transfer function of the readout circuit. Upon several iterations a best fit curve was obtained with a co-efficient of determination of 0.99. The fitted curve for the inputs and outputs of the readout circuit is shown in Figure 5.19 The derived transfer function of the input/output relationship is demonstrated in Equation 1.

$$\text{ADC Value} = 4082.6906 - \frac{4071.3265}{\text{Resistor Value}} \tag{1}$$

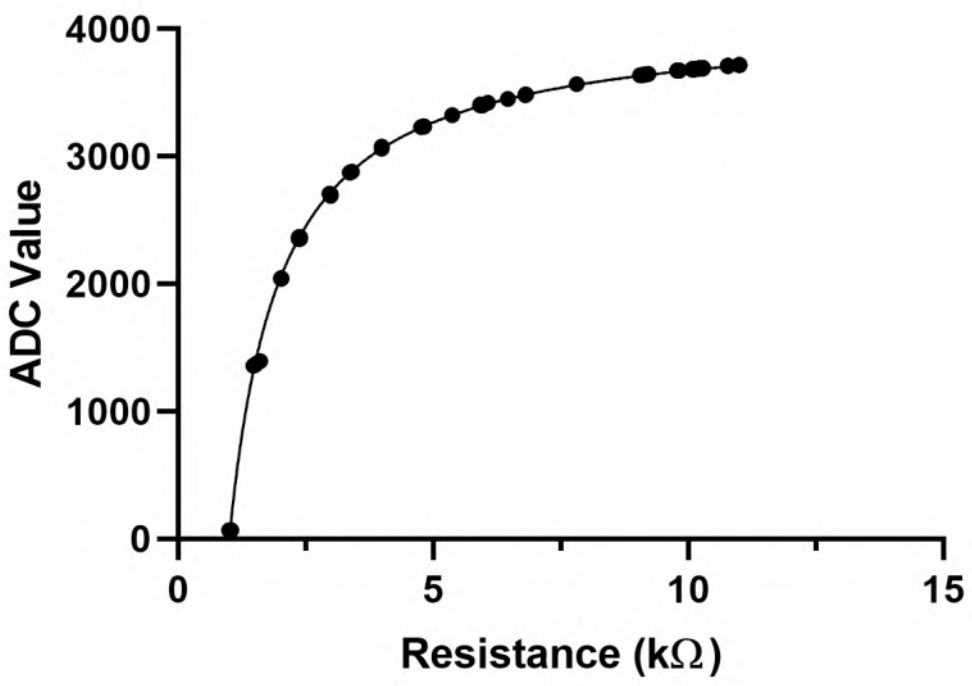


Figure 5.19: The non-linear regression model generated for the inputs and outputs of the readout circuit to determine its transfer function

5.7.2 Experiment to Determine the Measurement Accuracy

Measurement accuracy provides a quantitative analysis of the degree of crosstalk suppression within the implemented readout circuit. The experiment was designed to quantify the impact of non-scanned sensels on the measurement of a given EBT. The presumption behind the experiment was that closer the measurement of a given resistor by the readout circuit in the presence of non-scanned sensels to its actual resistance, greater the crosstalk suppression by the readout circuit. The RSA model and the developed readout circuit were used for the experiment.

Experiment Methodology

The eight rows of the RSA model was connected to the first eight row driving electrodes of the readout circuit and the eight columns of the RSA model was connected to the first eight column sampling electrodes of the readout circuit. The same set of fixed resistors used for analysing the transfer characteristic of the readout circuit was used (Section 5.7.1). First, the resistance of a 1.5 kΩ resistor was measured with a benchtop digital multimeter and its actual resistance was recorded. Then it was fixed at row 1, column 1 ((R1,C1) in Figure 5.20) location of the RSA model and the readout circuit output was recorded from the Tera Term serial terminal by connecting the APSoC to the computer via UART. Following that, the same EBT was surrounded with non-scanned resistors of 1.5 kΩ forming an array size of 2×2 as shown in Figure 5.20 (a) and the readout circuit output was recorded. Afterwards, the array size was gradually incremented to 3×3 (Figure 5.20 (b)), 4×4, 5×5, 6×6, 7×7 and finally to 8×8 (Figure 5.20 (c)) using 1.5 kΩ resistors. Therefore, the actual measurements form the readout circuit were measured using the stated method.

Subsequently, all 1.5 kΩ resistors were dismounted from the RSA model except the EBT mounted at (R1,C1). Same set of readings obtained with 1.5 kΩ resistors were taken gradually incrementing array size from 2×2 (Figure 5.20 (d)), to 3×3 (Figure 5.20 (e)) and all the way to 8×8 (Figure 5.20 (f)). Consequently,

readings were taken with 3 kΩ, 6.5 kΩ and 9.1 kΩ resistors with the same EBT of 1.5 kΩ. Eventually, EBT was replaced with 2.4 kΩ, 3 kΩ, 6.5 kΩ and 9.1 kΩ resistors and the same process conducted for 1.5 kΩ EBT was repeated.

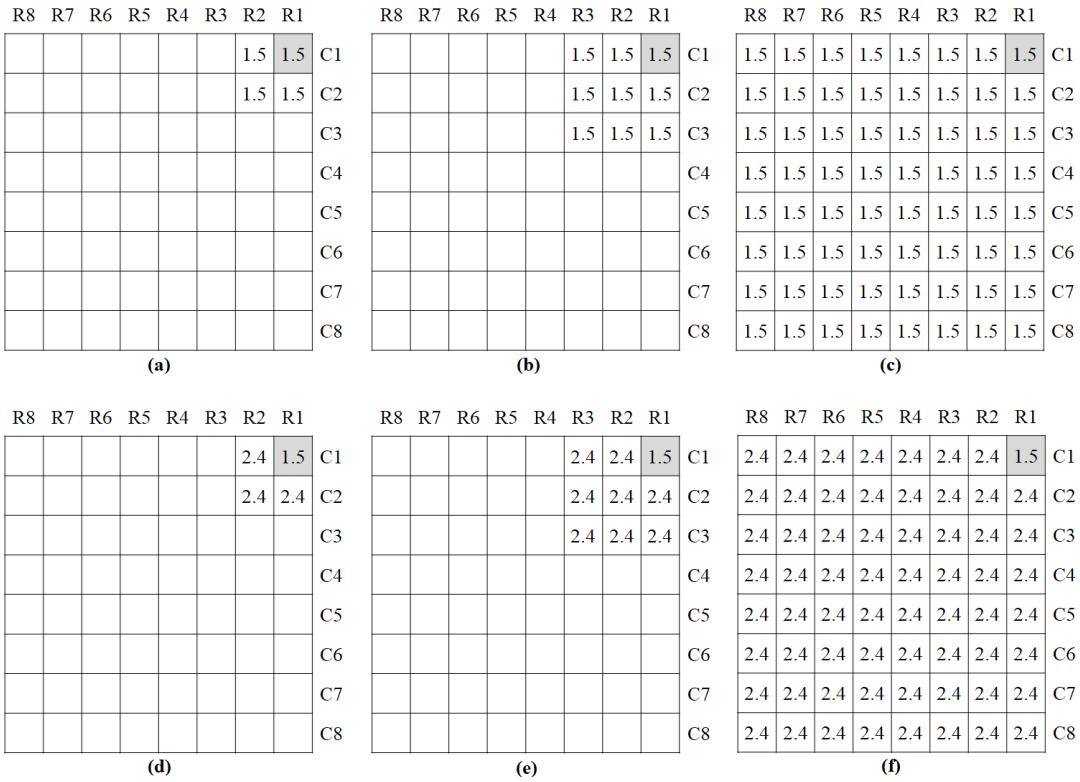


Figure 5.20: Experiment carried out to determine the measurement accuracy of the developed readout circuit by assessing the effect of non-scanned resistors on the measurement. The RSA is populated by non-scanned resistors forming a **(a)** 2×2, **(b)** 3×3 and **(c)** 8×8 array around the EBT fixed at (R1,C1) with 1.5 kΩ resistors. The RSA is populated by non-scanned resistors forming a **(d)** 2×2, **(e)** 3×3 and **(f)** 8×8 array around the EBT fixed at (R1,C1) with 2.4 kΩ resistors

In the aftermath of obtaining the true performance of the readout circuit through numerous EBTs in the presence of varied array sizes and non-scanned resistors a circuit simulation was conducted using PSPICE®. A circuit simulation model was implemented as shown in the Figure 5.21. Same component models/libraries of the components used in developing readout circuit were used for the simulation model as well. EBT was placed at the row 1, column 1 location and Single Pole Single Throw (SPST) switches were used in place of the decoder. However, they were left open to

simulate floating state of the non-scanned row driving electrodes. Since, column sampling electrodes of non-scanned columns were not measured, one op-amp was used to implement the zero potential state in all the non-scanned columns by selecting the desired number of columns through the corresponding ideal SPST switches as shown in the Figure 5.21. Ideal voltmeters were placed parallel to each resistor in the RSA to monitor their individual characteristics. Ideal SPST switches were also places between each resistor in a given row and a given column as shown in the Figure 5.21 so that desired array sizes could be formed as required. The layout of the experimental setup used to determine the measurement accuracy of the developed readout circuit is shown in Figure 5.22

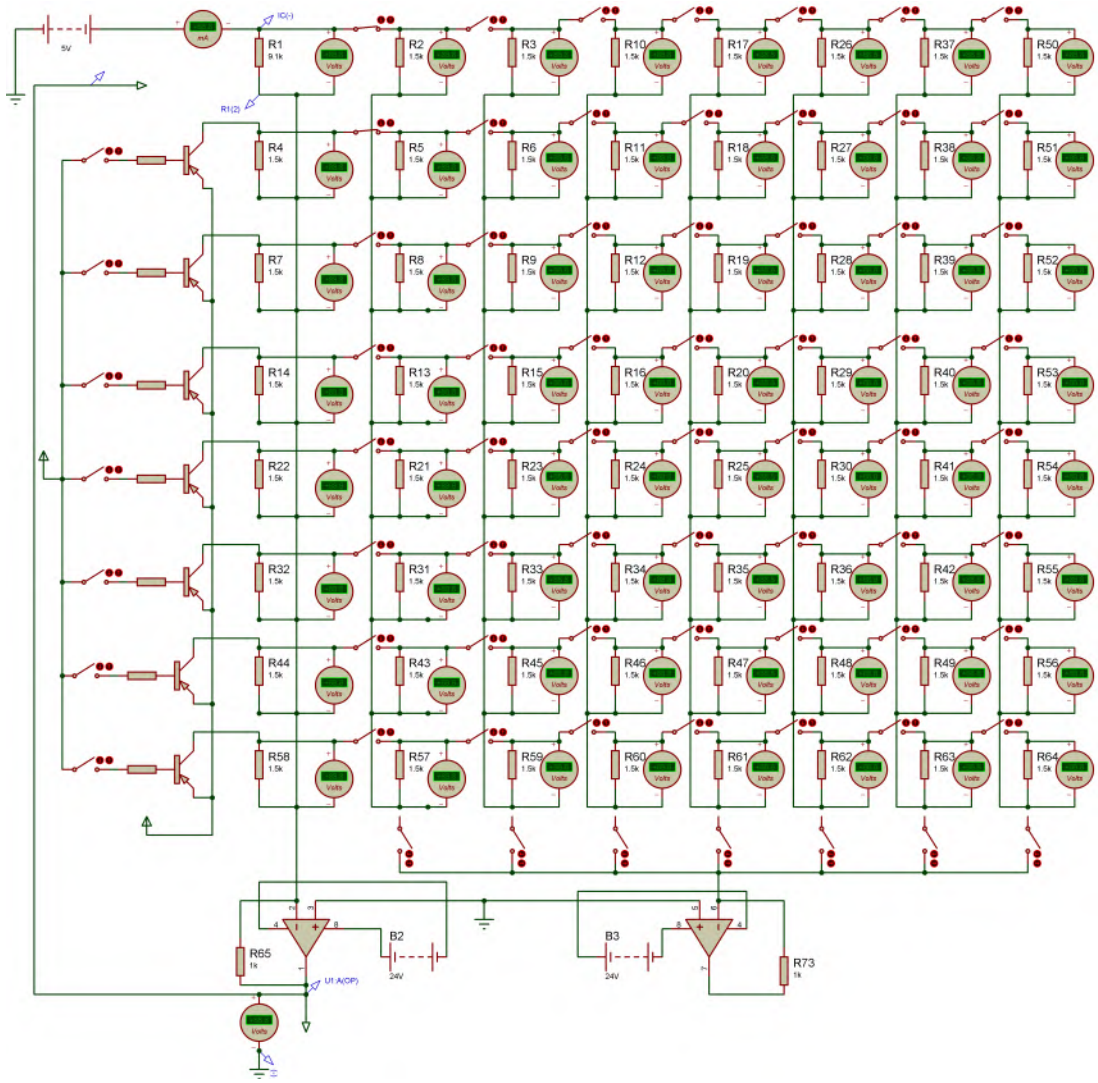


Figure 5.21: The 8×8 circuit simulation model developed in PSPICE®

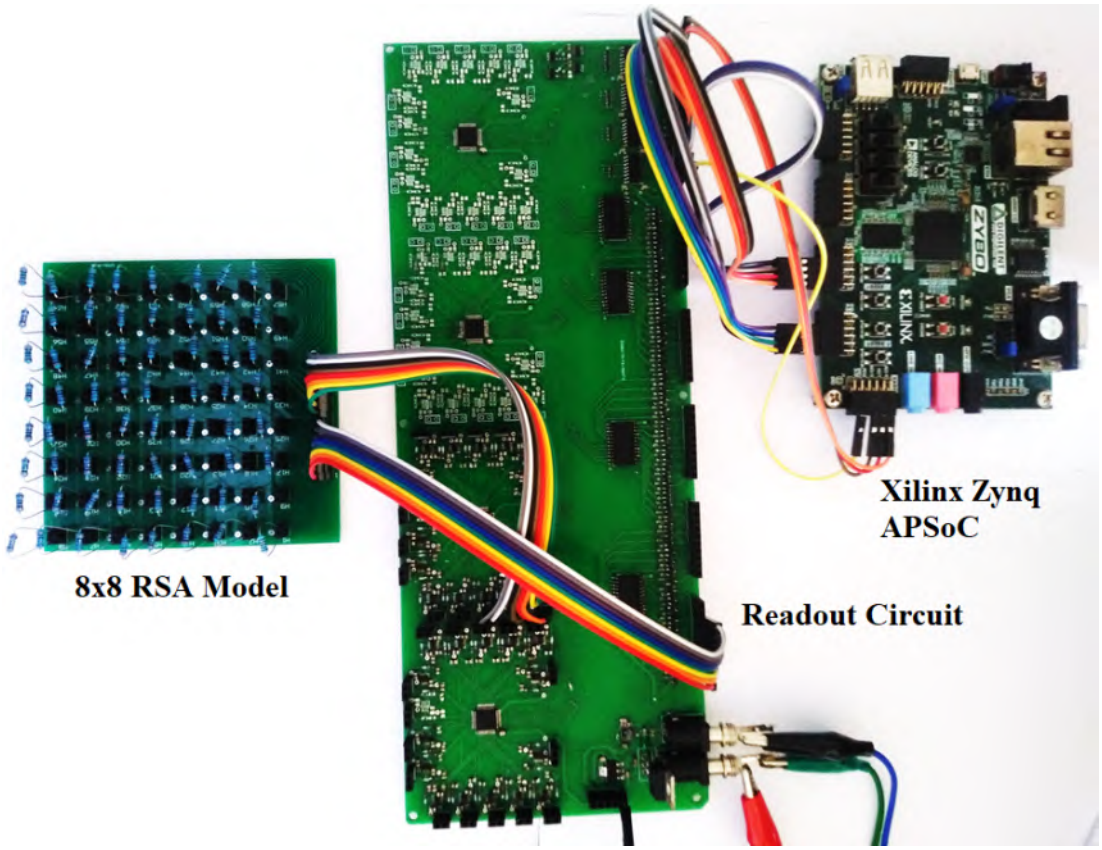


Figure 5.22: The layout of the experimental setup consisting of the 8×8 RSA, The readout circuit and the Xilinx Zynq APSoC board used to determine the measurement accuracy

All the corresponding readings taken from the 8×8 RSA model were also taken from the circuit simulation model by changing resistor values of the EBT and the non-scanned resistors. The measured voltage from the column sampling electrode of the column 1 (to which the EBT was connected) was converted to resistance using the readout circuit transfer function derived using the Equation 1. The circuit simulations, therefore, yielded the expected measurement from the RSA model.

Hence, the difference between the expected resistance measurement of the RSA from circuit simulations and the measured resistance recorded by the readout circuit deliver the measurement error caused by the readout circuit. Smaller the measurement error, greater the measurement accuracy of the developed readout circuit. The measurement

error was calculated as a percentage error as indicated in Equation 2.

$$\% \text{ error} = \left[\frac{\text{Expected Resistance}(\text{k}\Omega) - \text{Measured Resistance}(\text{k}\Omega)}{\text{Expected Resistance}(\text{k}\Omega)}\right] \times 100\% \quad (2)$$

Results and Discussion

The calculated percentage errors were plotted against the EBT value in the presence of different non-scanned resistors for different array sizes as shown in Figure 5.23. By way of explanation, consider the Figure 5.23 (a) which demonstrates the percentage error in measurement when the array size is 2×2 for different EBTs and different non-scanned resistors. The X-axis represents different EBT values used for measurement while the five distinct line plots shows the percentage error experienced by each EBT in the presence of different non-scanned resistors shown in the figure legend.

Therefore, from Figure 5.23 (a), it was deduced that when the EBT value is 1.5 kΩ and the array size is 2×2, the percentage error of measurement through readout circuit is the same irrespective of the non-scanned resistors present in the RSA. However, when the EBT value is 6.5 kΩ and 9.1 kΩ, there is a distinguishable difference between the percentage errors in the presence of different non-scanned resistors. Similarly, the Figure 5.23 (b), (c), (d), (e), (f) and (g) demonstrate the same functionality but for array sizes of 3×3, 4×4, 5×5, 6×6, 7×7 and 8×8 respectively.

It is evident from the percentage error analysis shown in Figure 5.23 that the measurement error of 1.5 kΩ EBTs remained consistent throughout the entire measurement process irrespective of the array dimensions and the non-scanned resistor value. Moreover, the measurement error displayed little-to-no fluctuation for all EBTs and non-scanned resistors for array dimensions of 2×2, 3×3, 4×4 and 5×5. However, measurement error seemed to amplify significantly beyond resistor array dimensions 6×6 onward. Although, initially it was thought that the error was propagated due to array size, further investigations revealed that the error was in fact due to rounding when calculating Resistor value from ADC Value from the

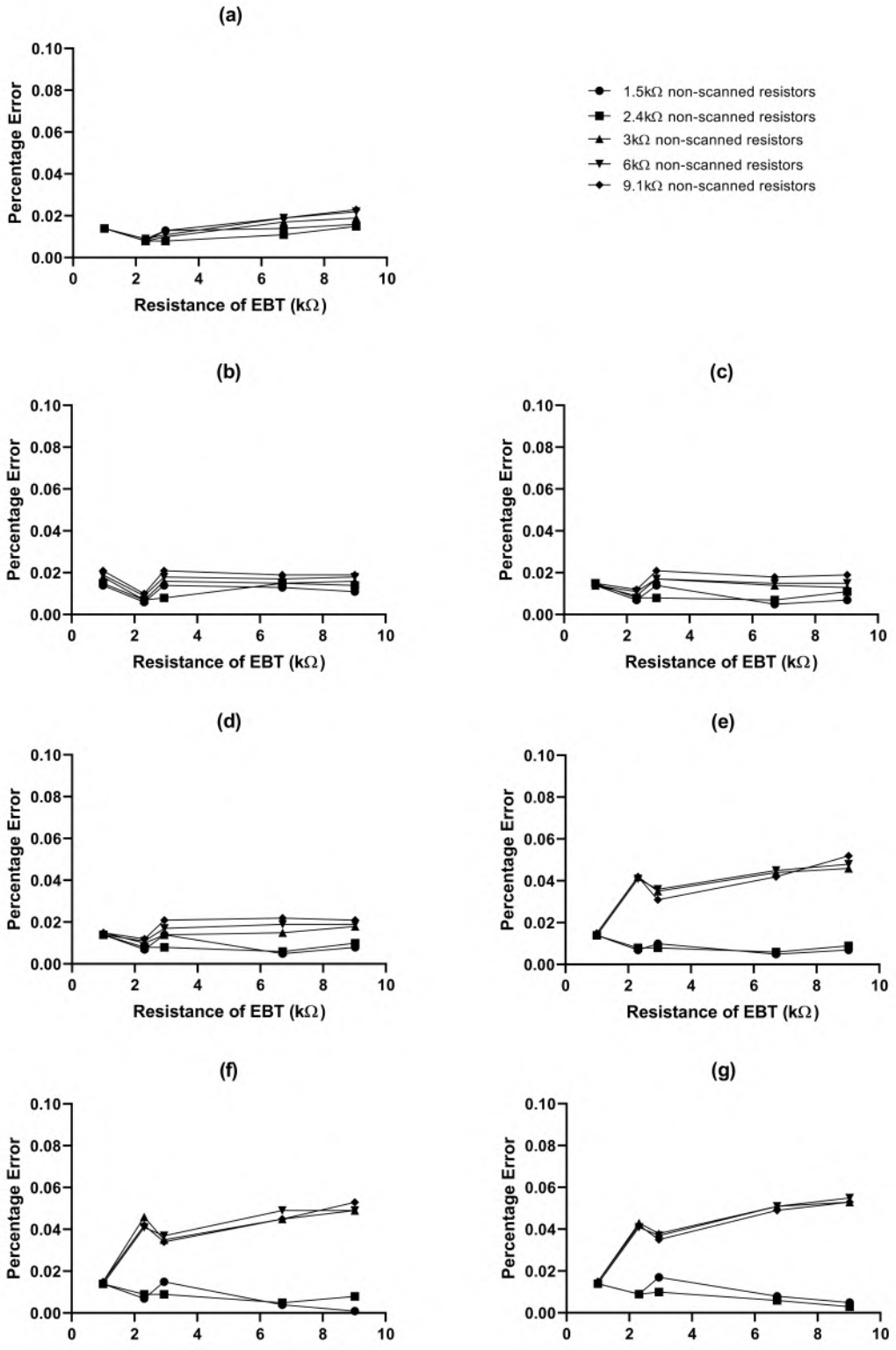


Figure 5.23: Percentage error measurement for the readout circuit under different EBTs in the presence of different non-scanned resistors and for different array sizes of **(a)** 2×2, **(b)** 3×3, **(c)** 4×4, **(d)** 5×5, **(e)** 6×6, **(f)** 7×7 and **(g)** 8×8

Equation 1. Calculating the percentage error to the second decimal place minimized the error significantly.

The reason for obtaining a consistent measurement error despite varying the RSA dimensions is a consequence of uniformity of the non-scanned resistors used. Owing to the circuit symmetry a RSA could be divided into four major zones as described in Section 3.5.3, if its sensels are identical (same response for excitation). The parasitic currents which result in crosstalk decreases drastically in zone 4 (sensels with no direct contact with the EBT) which include the majority of sensors. Since the fabricated piezoresistive sensor array theoretically have sensels with the same resistance when idling, above circuit property could be exploited so that array size has no significant impact on the measurement accuracy. Further, simulating the circuit model with increased array sizes up to 16×16 under non-ideal conditions reaffirmed the principle that the measurement error remained less than 0.1%. Therefore, it seems obvious that the novel decoder-transistor based row driving electrodes and accompanied scanning architecture boasts of the same degree of measurement accuracy (percentage errors $\leq 0.1\%$) which has been achieved by Kim et al. [116], however, with lesser hardware resources.

Given that the S-NSSE-ZP method rely on the retaining the non-scanned row driving electrodes at floating voltages while non-scanned column sampling electrodes at zero potential, low saturation voltages, low switch-ON resistances of transistors and low offset voltages, high open loop gain, low input bias currents of op-amps are the most critical design constraints in implementing the present scanning architecture. As the accuracy of the entire scanning mechanism depend heavily on these constraints they should receive the highest priority during component selection.

5.7.3 Experiment to Determine the Shape Accuracy

Measurement accuracy alone is not reflective of effective crosstalk suppression. The capability to accurately replicate a given shape, shape accuracy, is equally as

important. Shape accuracy analysis is nonetheless a qualitative analysis in contrast to measurement accuracy analysis which is a quantitative analysis (Section 3.8).

Experiment Methodology

The experimental procedure for determining the shape accuracy was as straight-forward as the techniques used by Vidal-Verdu et al. [107] and Yang et al. [123] discussed in Section 3.8. Rather than placing objects on the RSA, unique numerical, geometrical and alphabetical shapes were generated by mounting resistors that were used for the measurement accuracy assessment. The shape of a number (4), a basic geometric shape (triangle) and an English alphabet letter was initially repliacted on the 8×8 RSA model using 6 kΩ resistors as shown in the Figure 5.24. For the purpose of visualising the sensor array output a Python based graphical user interface was developed using matplotlib, numpy, seaborn and tkinter libraries (Section 5.9). The colour gradient was truncated to emphasize better contrast between background and the foreground during visualisation.

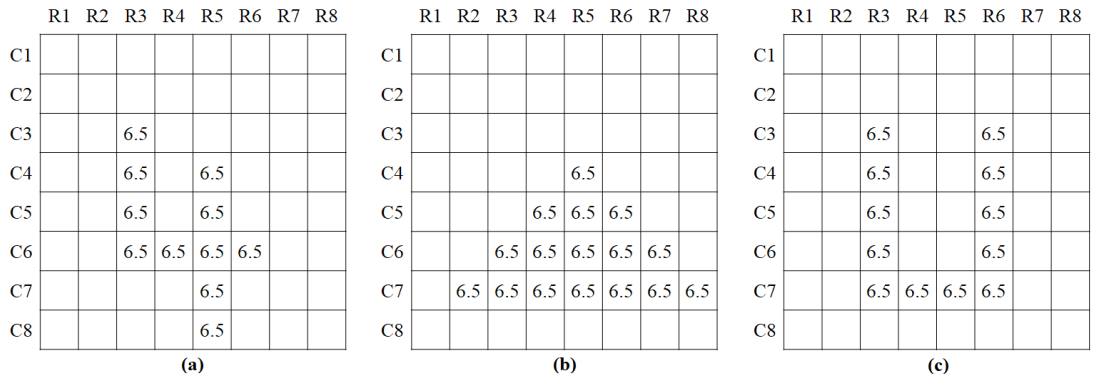


Figure 5.24: The resistor arrangement in the RSA to replicate the shape of **(a)** Number 4, **(b)** Triangular shape and **(c)** Letter U using resistors of 6.5 kΩ

Afterwards, a unique shape was created using a combination of 1.5 kΩ, 2.4 kΩ, 3 kΩ, 6.5 kΩ and 9.1 kΩ resistors to evaluate the behaviour of the readout circuit in the presence of variety of different resistors as shown in Figure 5.25. Here, full range of colour gradient (0 – 4096) was used to visualize resistor array implementation. Finally, to procure an overall assessment incorporating both measurement accuracy and shape

accuracy of the developed readout circuit, the ADC values of each and every resistor was obtained in the 8×8 RSA.

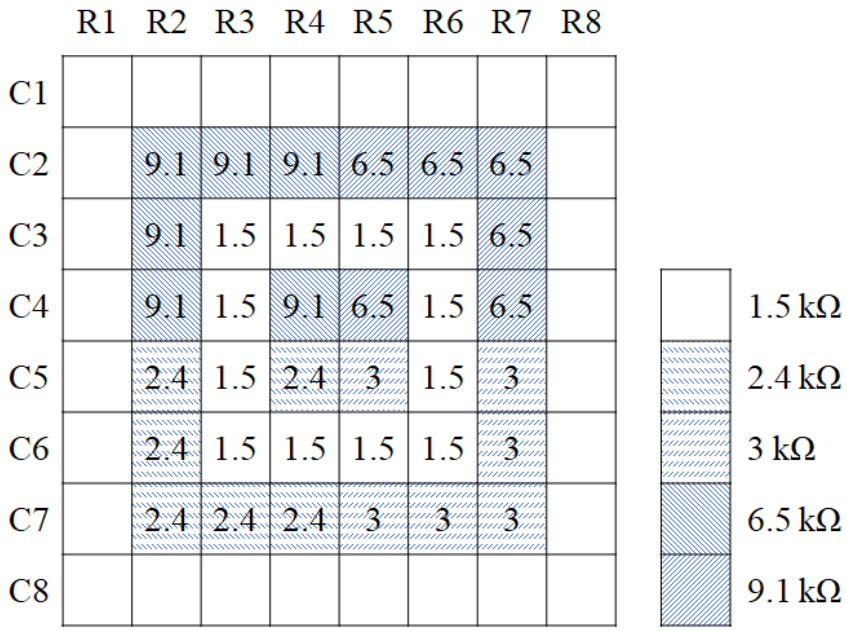


Figure 5.25: The compounded shape replicated on the 8×8 RSA model using five different types of resistors

Results and Discussion

Figure 5.26, 5.27 and 5.28 depicts output obtained for the three distinct numerical, geometrical and alphabetical shapes replicated on the RSA using resistors mounted on the RSA. It was seemingly obvious that the shapes configured on the RSA using resistors were accurately estimated by the readout circuit and APSoC assembly. Hence, the shape accuracy of the developed readout circuit is commendable without any crosstalk between adjacent sensels.

Moreover, the output visualized from the Python GUI for the compounded resistor arrangement shown in Figure 5.25 is presented in Figure 5.29. It was seemingly perceptible from the observations that the expected shape has been estimated by the readout circuit assembly. Figure 5.30 demonstrates the visualization observed when all the 64 sensels arranged in the same compounded shape as in Figure 5.25 were scanned and their resultant ADC value were annotated in their corresponding cells.

The range of ADC values attained for different resistor values are given in Table 5.3. Although the resistors mounted at (R4,C4), (R5,C4), (R4,C5) and (R5,C5) locations had four distinct resistor values in adjacent, they were also identified to deliver ADC readings in their respective ADC ranges denoted in Table 5.3. Therefore, it was clear that the readout circuit and APSoC system were able to demonstrate both measurement accuracy and shape accuracy simultaneously. The obtained results were published in the Q1 journal IEEE Sensors (Appendix C).

Table 5.3: Range of ADC values obtained for different resistor values when measured from the 8×8 RSA and readout circuit assembly

Resistor Value (kΩ)	**Range of ADC Values**
1.5	69 – 74
2.4	2375 – 2381
3	2705 – 2709
6.5	3486 – 3492
9.1	3639 – 3643

A significant contrast was observed between 1.5 kΩ resistors and 2.4 kΩ resistors in the compound resistor arrangement. However, the distinction in colour change gradually decreases with the increase in the resistance such that the contrast between 6.5 kΩ resistors and 9.1 kΩ resistors were significantly low. The reason this non-linearity was because columns were sampled by inverting op-amps which does not yield a linear output. Nonetheless, this was a desired feature that was permitted intentionally to provide a linearity correction for the pedobarographic system input (Section 5.7.4).

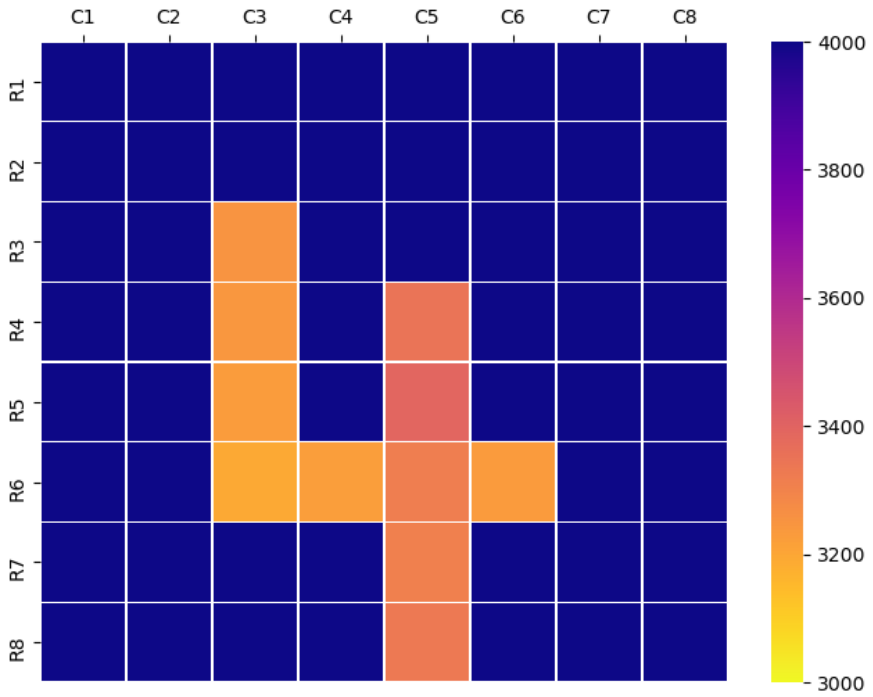


Figure 5.26: shape accuracy assessment via forming the shape of number 4 on the 8×8 RSA and scanning via the developed readout circuit

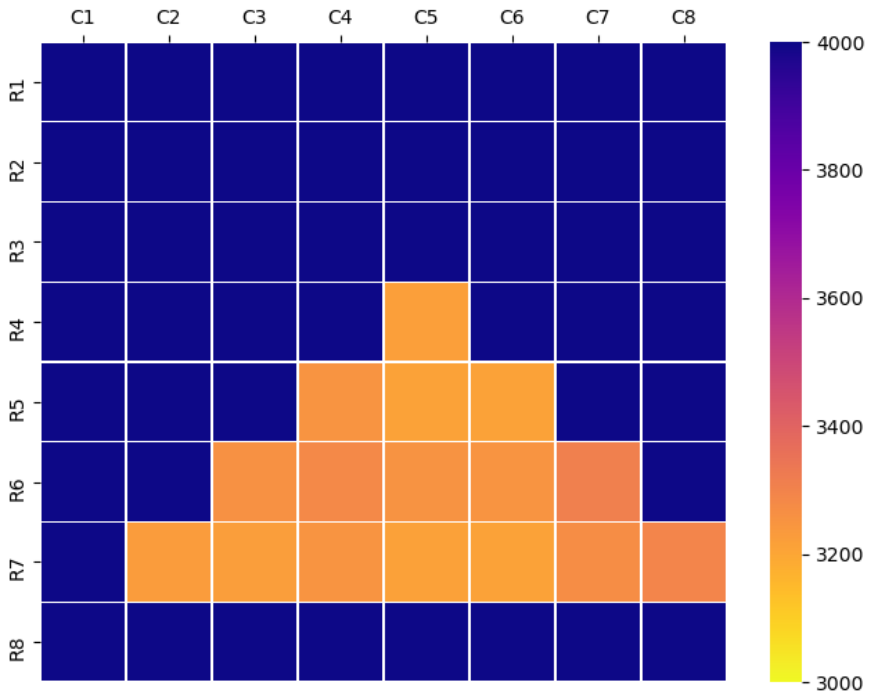


Figure 5.27: shape accuracy assessment via forming the shape of a triangular shape on the 8×8 RSA and scanning via the developed readout circuit

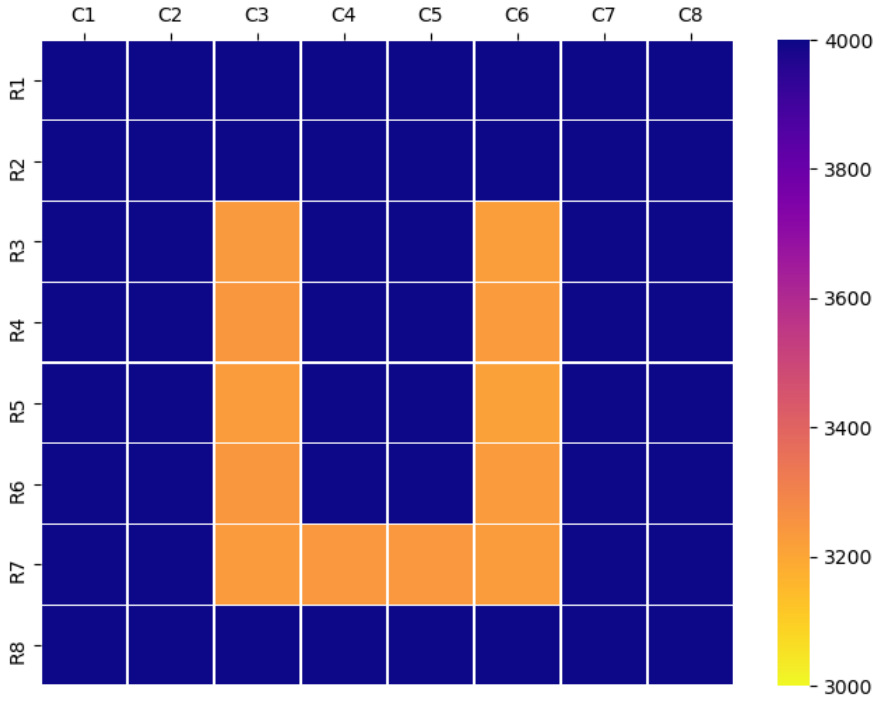


Figure 5.28: shape accuracy assessment via forming the shape of letter U 4 on the 8×8 RSA and scanning via the developed readout circuit

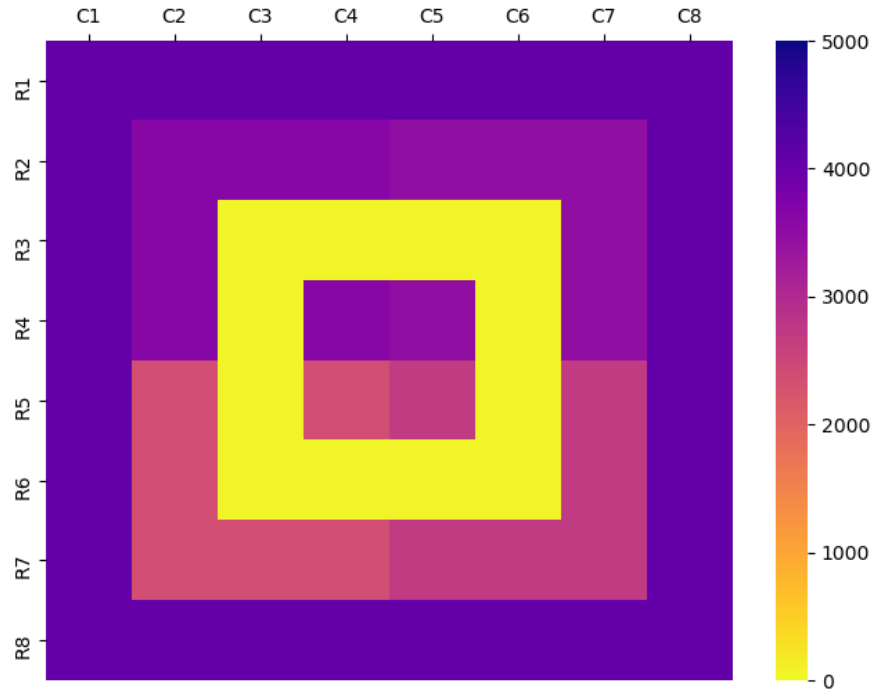


Figure 5.29: Shape accuracy assessment via forming a compounded shape on the 8×8 RSA using resistors of 1.5 kΩ, 2.4 kΩ, 3 kΩ, 6.5 kΩ and 9.1 kΩ

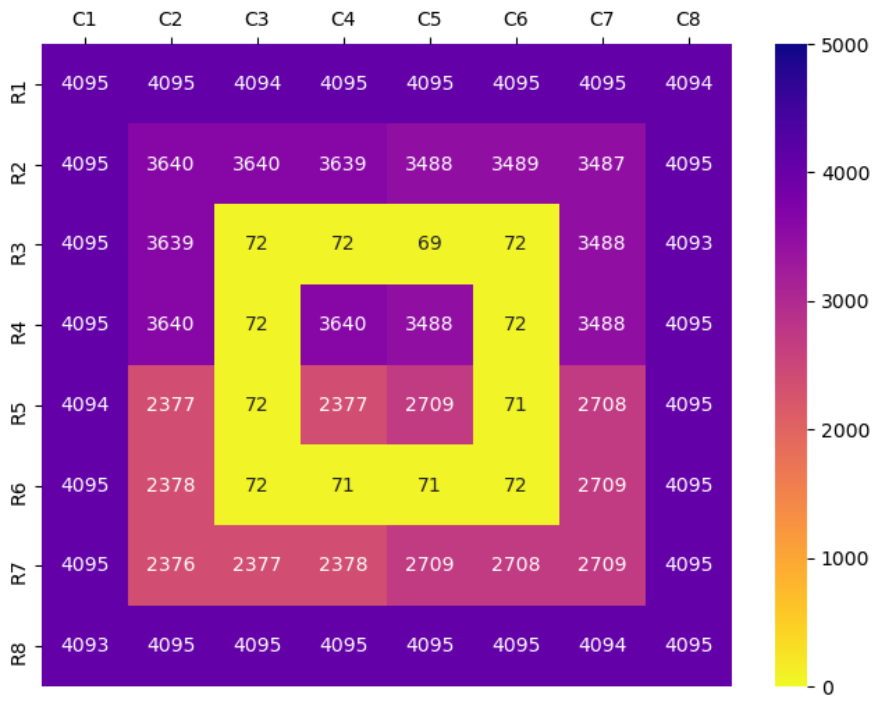


Figure 5.30: Assessment of both shape accuracy and measurement accuracy via the compounded shape formed on the 8×8 RSA using resistors of 1.5 kΩ, 2.4 kΩ, 3 kΩ, 6.5 kΩ and 9.1 kΩ

5.7.4 Linearity Correction to the Pedobarographic System

The input to the pedobarographic system is the pressure exerted by the foot plantar which is reflected as a change in resistance by the piezoresistive sensor array. The change in resistance and input pressure have a non-linear relationship [95, 107]. Nevertheless, the relationship between the input resistance and the ADC value of the readout circuit, which is essentially the pedobarographic system output, is also non-linear (Equation 1).

Therefore, if the readout circuit was carefully designed such that the non-linearity induced as a result of the pressure-resistance relationship is reverted back to linear as a result of the resistance-ADC value non-linear relationship, then the resultant input to the system and the resultant output from the system ultimately becomes linear. In

order to determine the degree of linearity correction rendered by the system the non-linear relationship between the input pressure and the corresponding resistance of the fabricated piezoresistive sensor array derived from the manufacturer provided data was plotted as shown in Figure 5.31.

For the resistance values obtained as the output for the input pressure values in Figure 5.31, the corresponding ADC values generated by the readout circuit were derived using the Equation 1 which is depicted in Figure 5.32. Accordingly, the relationship between the corresponding input of the pedobarographic system and the corresponding system output which were plotted is shown in Figure 5.33.

A simple linear regression analysis conducted using SPSS® revealed that the system input and the system output has a coefficient of determination (r_2) of –0.95. Hence, it is abundantly clear that the developed implementation provides a linearity correction effectively.

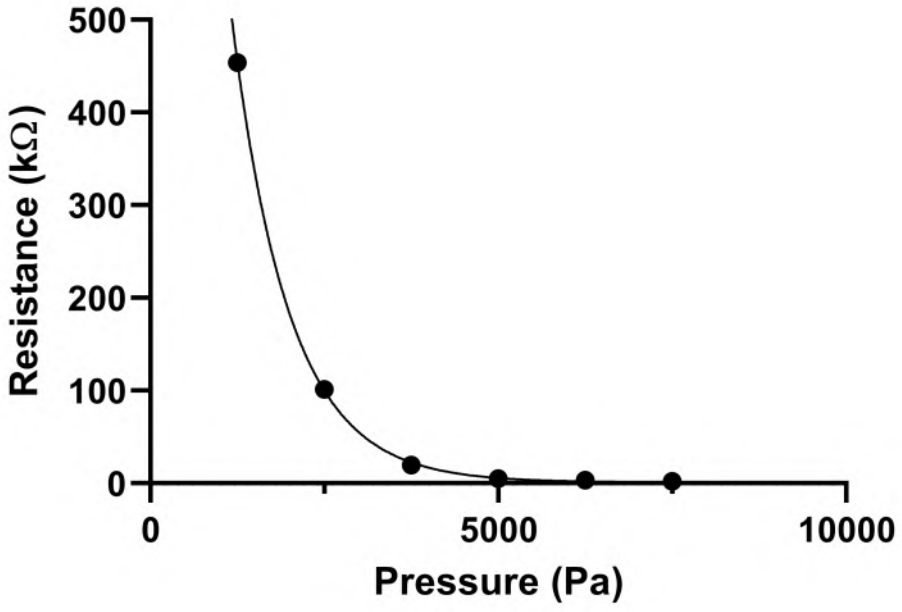


Figure 5.31: The input pressure vs resultant resistance for the piezoresistive sensor array based on the manufacturer provided data for the resistor range of 1 kΩ – 10 kΩ

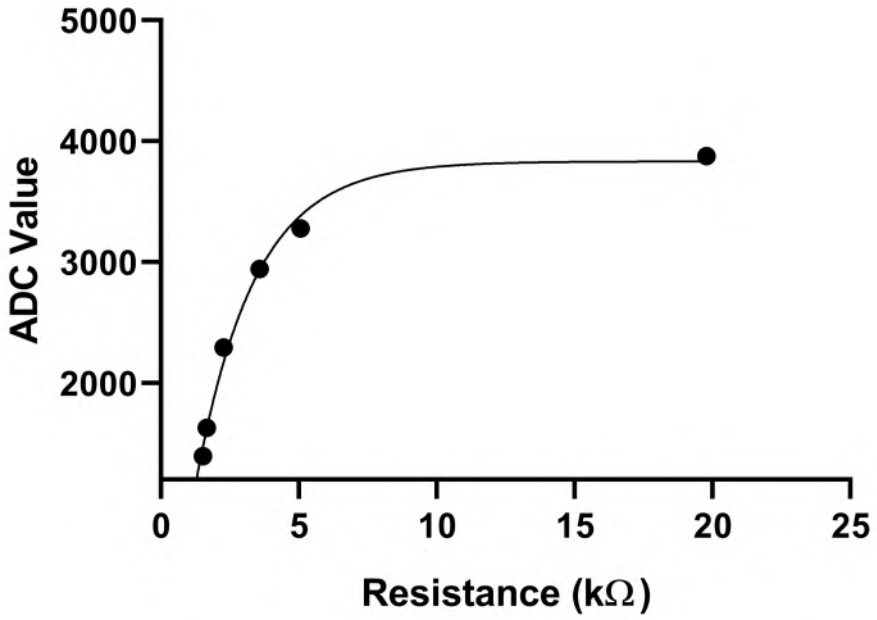


Figure 5.32: The resistance vs ADC value relationship for the resistance values derived from input pressure values provided by the manufacturer

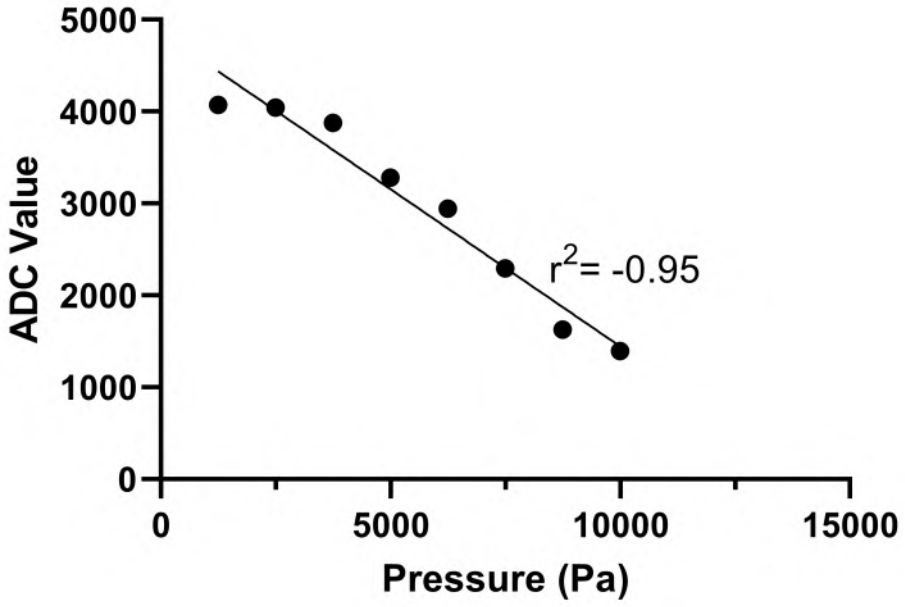


Figure 5.33: The relationship between pedobarographic system input (pressure) vs the output (ADC value)

5.8 APSoC Implementation

APSoC based implementations are gradually displacing microcontrollers, PSoCs and even FPGAs as they furnish the performance of hardware and the flexibility of software concurrently, while enabling parallel processing [178]. Therefore, APSoC based on Xilinx Zynq-7000 architecture for reasons cited in Section 3.10.5 was selected as the controller.

Implementation of the readout circuit with a novel scanning architecture meant that the controller had to be configured accordingly. The following are the main functions carried out by the APSoC device during the sensor array scanning.

1. Issue control signals components (chip select, enable signals)
2. Issue addresses values for the multiplexers and decoders to drive rows and sample columns
3. Acquire digitized data from ADCs
4. Package acquired data and store them temporarily
5. Transmit the acquired data to a computer

Upon establishing of the expected functionality from the APSoC system, necessary functional blocks to carry them out were identified. On that basis, several standard Intellectual Property (IP) blocks in the Xilinx Vivado IP library were selected for the final design implementation. Moreover, the functionality of the IPs which have to be custom designed for the end-application were also identified.

Using these existing and custom built IPs, high speed logic was implemented in the Programmable Logic (PL) whereas software routines such as handing interrupts, issuance of control signals and communication between computer was implemented in the Processing System (PS).

The only input to the APSoC was acquired from the PL side through the ten ADS7886 ADC chips which generates a 12-bit ADC output. However, the fixed data bus width of (Advanced eXtensible Interface) AXI which is used to form interconnections between PS and PL peripherals is 32 bits or 64 bits. Because the data bus width was selected to be 32 bits, the 12–bit ADC values received had to be aligned across the 32-bit data bus as shown in Figure 5.34 to minimize the waste and ensure optimum performance.

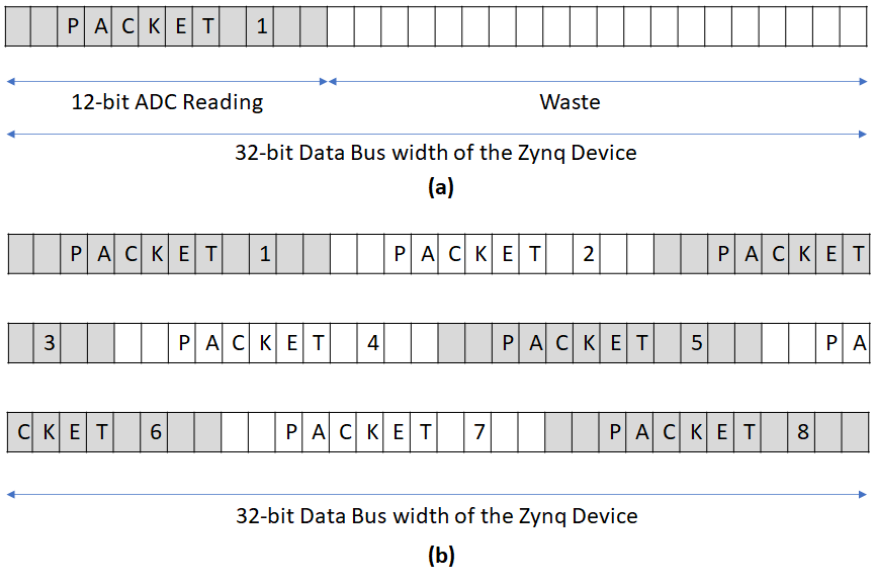


Figure 5.34: **(a)** Arranging 12-bit data from the ADC into 32-bit wide data bus of the Zynq waste the bus space and reduce the efficiency of data transmission. **(b)** Arranging 12-bit data from ADC into 8 data packets across three temporary registers to be transmitted to the DDR3 memory of the PS in 3 consecutive transactions was identified to be the best use of the AXI data bus while improving the efficiency

To eliminate any ambiguity with the architecture implemented in readout circuit being referred to as the "Scanning Architecture", the architecture implemented in the APSoC that sanction the data acquisition from the readout circuit, pre-processing and packaging of the acquired data and transmission of packaged data would hereon be referred to as the "data acquisition (DAQ) architecture".

5.8.1 Simulation of One Cluster in Xilinx Vivado

Before implementing the DAQ architecture in Vivado, a simulation study was conducted to identify the expected functionality and the type of behavior expected of the DAQ architecture. For this purpose, three distinct IP modules were designed as shown in the Figure 5.35.

The MemRam_0 module executed the role of the piezo resistive sensor array by generating 3000 unique values at every positive clock edge. sample_adc module assumed the role of the ADC chip on the readout circuit. Therefore, for input signals of chip select (cs) and serial clock (sclk), sample_adc generated corresponding ADC values in between 0 and 4096 (output range of a 12-bit ADC). adc_read_0 module was a module implemented to acquire the data into the APSoC, issue clock signals and cs signal for the sample_adc.

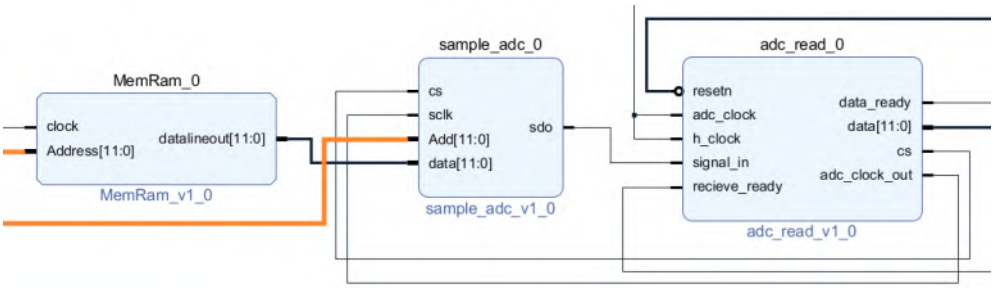


Figure 5.35: The module combination of the initial simulations for expected behaviour of one cluster

When MemRam_0 produced a unique output through datalineout[11:0] it should be acquired by the sample_adc and a corresponding output (sdo) should be generated if both cs is enabled and at positive edge of sclk. The sdo is the signal_in for the adc_read_0 module. When 12 bits of data are acquired, a data_ready signal is asserted and acquired data are dumped onto the data[11:0] output port on the adc_read_0. adc_read_0 module also provide a low speed clock (adc_clock) to the sample_adc as it requires a significantly low clock for its operation compared to hardware IP modules which require a high speed clock. After programming each and

every module in Verilog for the desired functionality, a behavioral simulation study was carried out to determine whether the expected functionality has could be achieved. The behavioral simulation data are presented in Figure 5.36.

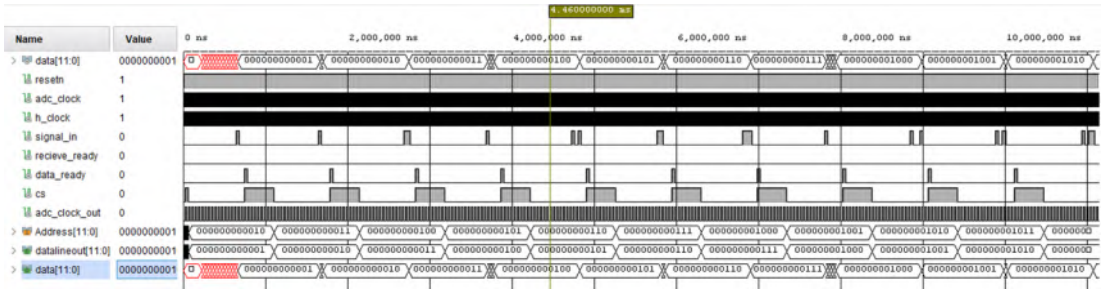


Figure 5.36: The behavioral simulation results for the simulation of one cluster in Xilinx Vivado

The behavioral simulation portrays that when cs and adc_clock are asserted, the MemRam_0 output is acquired by the sample_adc and given out as signal_in to the adc_read_0. Afterwards, data_ready is asserted and acquired 12-bit data are accurately copied onto the data[11:0] port, thus, confirming the optimum operation. Consequently, a DAQ architecture was implemented in the APSoC by removing both MemRam_0 and sample_adc from the design and keeping signal_in as the primary input to the DAQ architecture. Moreover, several improvements were made to the adc_read_0 module as discussed in Section 5.8.2

5.8.2 Modular Implementation in Xilinx Vivado

Upon identification of the expected functionality a suitable DAQ architecture was developed after several iterations. The final block diagram of the IP based modular implementation carried out in Xilinx Vivado is illustrated in Figure 5.37. The functionality of the implemented modules is discussed in the subsequent sections. All custom developed RTL modules were programmed with Hardware Description Language (HDL) Verilog. Seeing that Vivado does not facilitate simulation of the entire block diagrams, each and every module was subjected to behavioral simulation individually.

The following section disclose the implementation carried out in Vivado and the subsequent sections further elaborate on the obtained results and the .

Zynq Processing System

The Zynq processing system IP was the first standard IP included in the project. Although, the software programming of the processor was done separately in Xilinx SDK environment, in order to implement the interconnections between the PS and PL modules and generate the clock signals required by the PL, Zynq IP had to be utilized and configured.

High Performance Port HP0 (Section 3.10.5) was used to interface the PL and PS and the PL-PS interrupt port (IRQ_F2P) was used to generate an interrupt to the communication between the PL and PS through HP0. For harmonious operation, all modules implemented within PL required a system clock generated by PS. However, the ADC chip which sampled at 1 MSPS required a significantly low speed clock signal as discussed in Section 5.8.1 . Therefore, two clock signals of 20 MHz (for ADC IC) and 250 MHz (for all IP modules implemented in hardware) were generated for the PL by PS.

When eight ADC data packets are arranged into three 32-bit transactions as shown in Figure 5.34, an interrupt should be issued to the Zynq processing system (to IRQ_F2P port) by the axi_lite_slave_0 module to initiate data transfer to the DDR3 memory by the processor. As ten clusters transmit eight ADC packets simultaneously, 80 ADC data packets are transmitted and saved to DDR3 memory simultaneously. To relieve the processor of the burden of initiating and sustaining communication, a Direct Memory Access (DMA) module from the standard Xilinx IP Catalogue was used.

adc_0 module

This module is a custom designed RTL module which perform the function of issuing control signals to the ICs and other components in the readout circuit and acquiring two ADC readings from two clusters of the readout circuit. In addition, it provides two

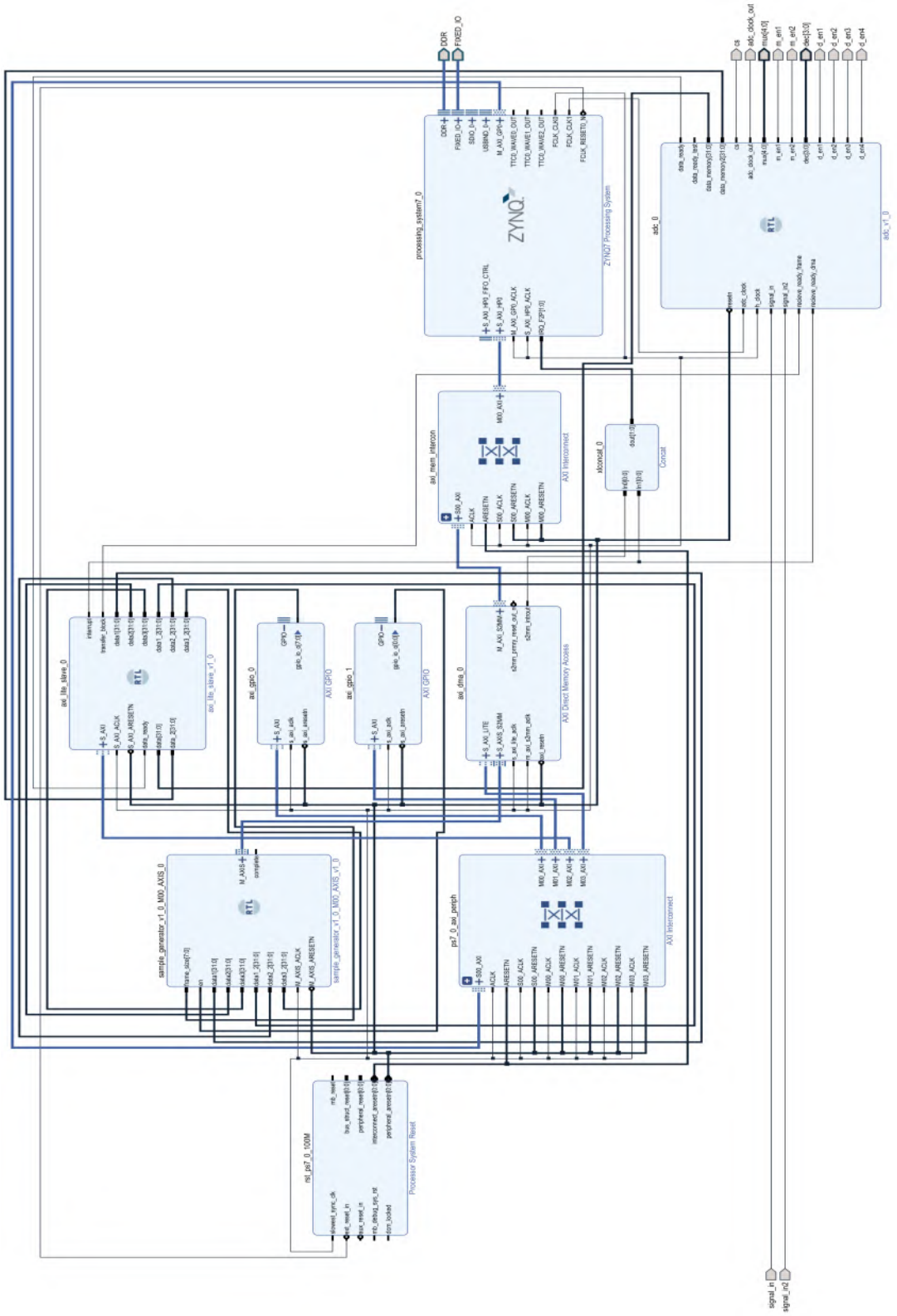


Figure 5.37: The IP based block design for the implemented DAQ architecture in Xilinx Vivado for scanning two clusters via one readout circuit

clock signals to the to the PL modules and IC components as illustrated in Table 5.4.

Table 5.4: Signals issued and acquired by the adc_0 module

Signal	**Function**
resetn	Active low reset signal from the processor system reset module
signal_in signal_in2	ADC values acquired from cluster 1 and 2
adc_clock	20 MHz clock for ADC chip on the readout circuit
h_clock	250 MHz clock for IP modules in PL
cs	Provide the chip select signal for both ADCs of the corresponding two clusters which are enabled simultaneously
adc_clock_out	Provide the clock signal for the ADC
mux[4:0]	The address signal of the multiplexer input channel to be switched to the output
m_en1, m_en2	Enable signals to activate either of the two multiplexers
dec[3:0]	The address signal of the decoder output channel to be switched to the input
d_en1, d_en2, d_en3, d_en4	Enable signals to activate one of four decoders of the shared row driving electrodes

The module is equipped with the capability to separately buffer (in two temporary 32-bit wide registers) the most recent 32 bits of the 12-bit ADC readings from two clusters (signal_in and signal_in2) as shown in Figure 5.34(b). Once both buffers fill completely with 32 bits, data_ready signal is issued to the axi_lite_slave_0 module to indicate that 32-bit data packet is ready to be transmitted. Then the buffered 32-bit data are unloaded onto two 32-bit wide data busses of adc_0, data_memory[31:0] and data_memory2[31:0] respectively which latches them on, so that ADC reading can be sustained without affecting the sampling at the axi_lite_slave_0.

Afterwards, 32-bit data on data_memory[31:0] and data_memory_2[31:0] ports of adc_0 are dumped on to data[31:0] and data_2[31:0] input ports of axi_lite_slave_0. Similarly, the next 32 bits from signal_in and signal_in2 are also transmitted to the

axi_lite_slave_0 module through its data[31:0] and data2_2[31:0] ports.

The control signals issued by this module are generated from a state machine which first traverse trough the sampling electrodes and then though the driving electrodes. However, there remains no hardware constrain on relationship between control signal and address of the value in the DDR3 memory. That mapping is completely handled by the firmware so that higher degree of flexibility remain to write software using this hardware.

As shown in Table 5.4, multiplexer address signals (mux[4:0]), multiplexer enable signals (m_en1 and m_en2), decoder address signals (dec[3:0]) and decoder enable signals (d_en1, d_en2, d_en3 and d_en4) were also issued by the adc_0 module. Therefore, decoder address is asserted to the shared decoder address bus and one decoder is enabled. Then, multiplexer address is asserted to the multiplexer address bus and one multiplexer is enabled. Multiplexer addresses then increment gradually until all the columns of the activated row is transversed. Subsequently, the decoder address is incremented by 1. This procedure is continued until all the addresses of the decoder output pins are transversed so that a cluster is scanned completely. The ability of the module to properly execute the described functionality was evaluated via behavioral simulations conducted in Xilinx Vivado.

axi_lite_slave_0

This module assumes the role of the main control unit in the PL of the APSoC, and it has an AXI Lite Slave interface with 96-bit addressable memory. It acquires three consecutive 32-bit data readings from each cluster via data_memory[31:0] and data_memory2[31:0] from adc_0 through its data[31:0] and data_2[31:0] input ports and arrange them in six 32-bit buffers, data1[31:0], data2[31:0], data3[31:0] (for cluster 1) and data1_2[31:0], data2_2[31:0], data3_2[31:0] (for cluster 2) until all six buffers acquire a total of 96 bits of data across three transactions. Once all six 32-bit buffers are filled and aligned, interrupt signal is issued to the PS as well as the adc_0 module. The adc_0 module pauses it's operation until PS clears the interrupt once it

acquires and save all 96 bits in its DDR3 memory. By buffering the three most recent data transfers in axi_lite_slave_0 it was ensured that no data loss from ADC chip happens during data transmission.

Sample Generator

Sample generator is a custom developed RTL module to streamline the acquired and stored 96-bit data from each cluster by the axi_lite_slave_0 to AXI stream data. The reason being the acquired data are written to the DDR3 memory of the PS via a DMA interface. Sample generator temporarily store the aligned data by axi_lite_slave_0 module. Therefore, the six input ports of sample generator data1[31:0], data2[31:0], data3[31:0] (for cluster 1) and data1_2[31:0], data2_2[31:0], data3_2[31:0] (for cluster 2) acquire and temporarily store the 32-bit data.

Although it was a redundant module, it was incorporated to ensure that provision for data corruption is minimal at axi_lite_slave_0 if both adc_0 and axi_dma are accessing the axi_lite_slave_0 module simultaneously. In order to transmit the acquired data to the DDR3 memory of the PS, and subsequently arrange the acquired data in a 2D plane, the transmitted data has to be memory mapped [142]. A transaction is said to be memory mapped if the source specifies a corresponding address in the address space of the target device during the transaction [142]. However, the data in sample generator are stream data (with no address values).

Direct Memory Access (DMA)

A DMA module is used to convert the stream data into memory mapped data while limiting the processor (in PS) intervention in data movement tasks, thereby, reducing the overhead of handshaking and complexity of data transmission. The stream data from M_AXIS port of sample generator was converted to memory mapped data by the S_AXIS_S2MM interface of the configured AXI Direct Memory Access IP-core used in the design. During data transmission, DMA assumes the role of the master and transmit data to the DDR3 memory of the PS processor through the AXI memory interconnect.

AXI Memory Interconnect

For the reason that AXI interfaces in PL and PS cannot interface directly an interconnect is required in between which acts as a switch which oversee the data transfers. AXI memory interconnect was used to interface between the DMA and the HP0 slave port of the PS which received the data and transmitted them to the DDR3 memory.

Other Standard Xilinx IP-cores used

Two AXI GPIO blocks were used to generate control signals for the sample generator to transmit data through DMA. axi_gpio_1 was used to provide the enable signal to the signal generator and 8-bit axi_gpio_0 was used communicate the number of transactions that the sample generator needs to perform.

The AXI peripheral interconnect was used to connect AXI slave interfaces to the PS. Since a single clock is used for all the AXI peripherals. Processor System Reset was auto-generated alongside Zynq processing system to provide reset signal to all modules. Concat module is used to concatenate interrupt signals to and from the processor.

Xilinx SDK implementation

Although, the functionality of the IP modules could be implemented through a HDL in hardware, the functionality of the PS could only be programmed using using software. As the PS is responsible for issuing control signals, clock signals, address signals, temporarily storing ADC values in DDR3 memory and transmitting data to the computer. These sequential processes were programmed into processor in the PS using built in Xilinx SDK software development environment in C.

When all the functionality is incorporated to both the PS and PL modules, debugging could be carried out by connecting the APSoC to the computer. UART data communication interface was used to transmit the acquired data to the computer. The

raw ADC data acquired by the DDR3, could be visualised through a terminal program such as Tera Term installed in the computer as shown in Figure 5.39.

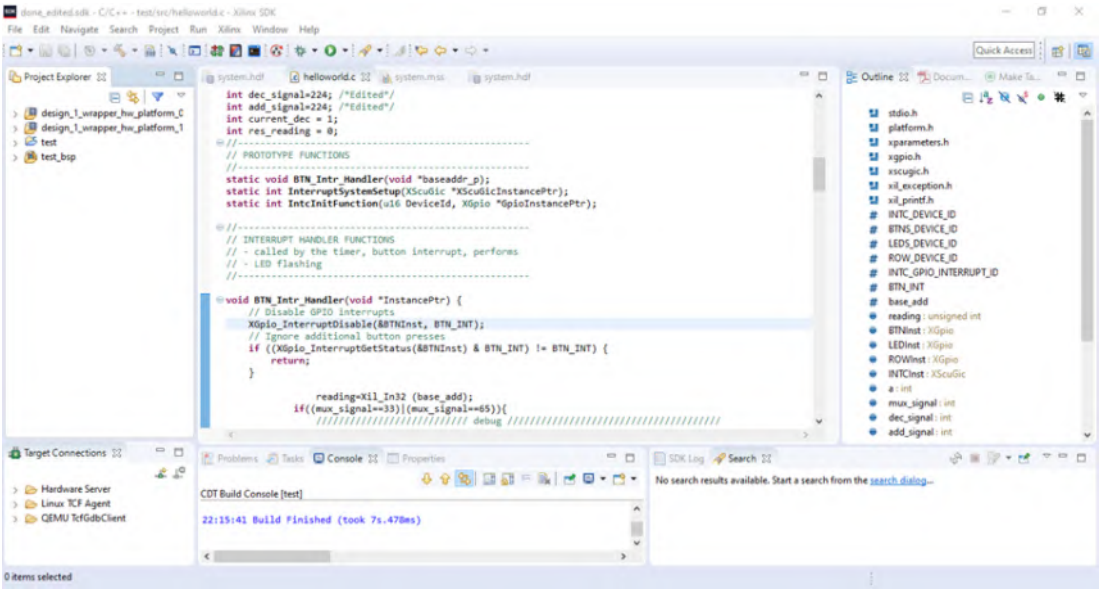


Figure 5.38: Programming the processor at the PS using Xilinx SDK

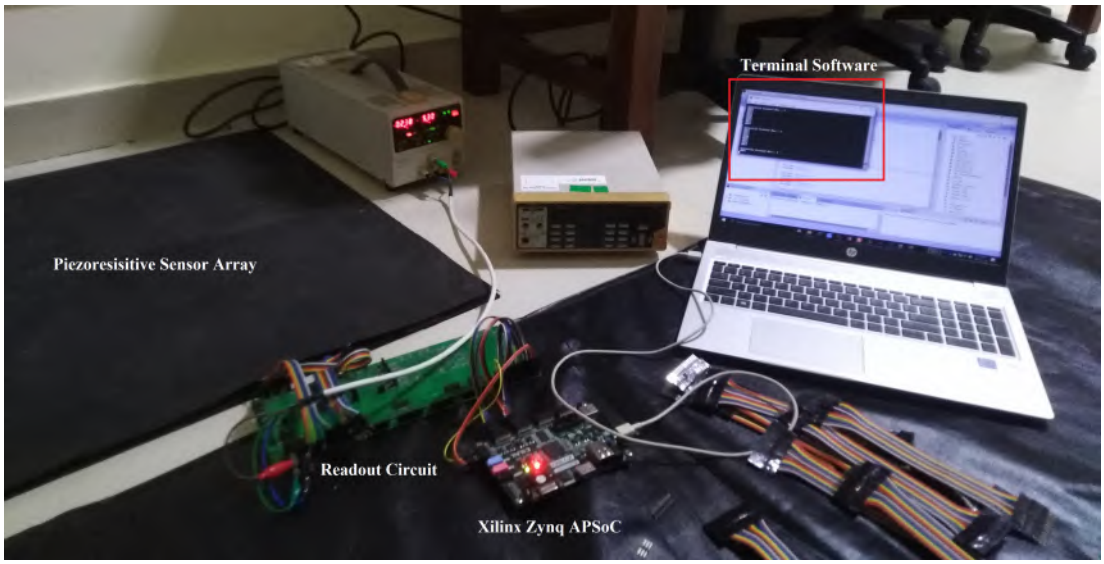


Figure 5.39: Visualising raw ADC values from the piezoresisitive sensor array via Tera term terminal software

5.8.3 Results and Discussion on APSoC Implementation

In an effort to verify the proper functionality of the developed data acquisition system on the Zynq device several simulation based studies were conducted. Separate test benches were written in Verilog HDL for the individual modules and their functional correctness was assessed by evaluating the output for a control set of inputs and comparing the obtained output with expected output.

Accordingly, the ability of the custom developed adc_0 RTL module to accurately issue control signals to the readout circuit was evaluated. Thus obtained simulation results of the control signals issued by the the adc_0 module are shown in the Figure 5.40, 5.41 , 5.42 and 5.43.

Figure 5.40 demonstrates that the adc_0 module receive the input ADC signals only after asserting the cs and adc_clock signals as expected. The adc_clock_out signal issued to the two ADC chips of the readout circuit was observed to be of the desired frequency of 20 MHz because from Figure 5.41,

$$\begin{aligned} Period\ (ns) &= 4,999,750\ ns - 4,999,700\ ns \\ &= 50\ ns \\ \therefore\ \ frequency &= \frac{1}{50}\ ns \\ &= 20\ Mz. \end{aligned}$$

Moreover 32 bits of data has been accurately loaded onto both data_memory[31:0] and data_memory2[31:0] busses.

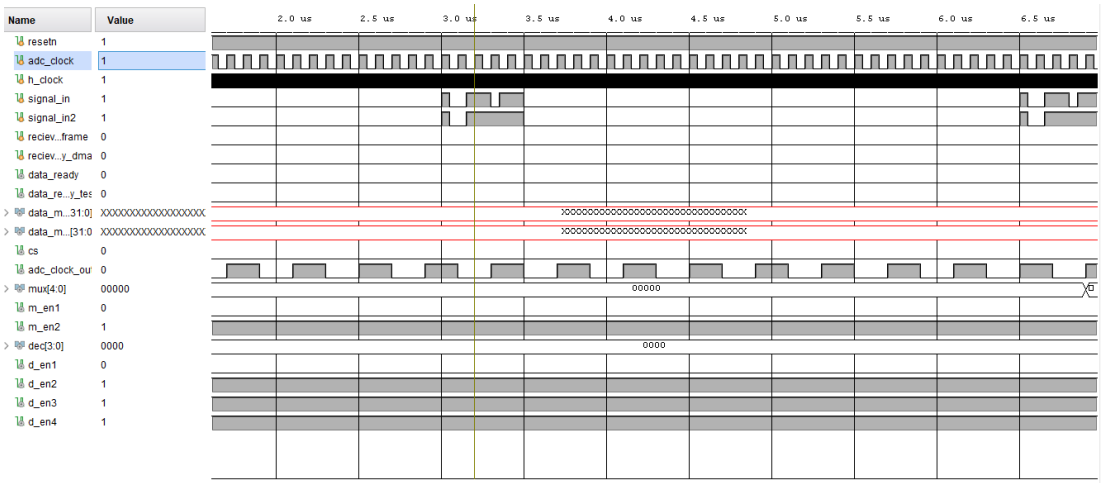


Figure 5.40: Simulation results for the adc_0 module

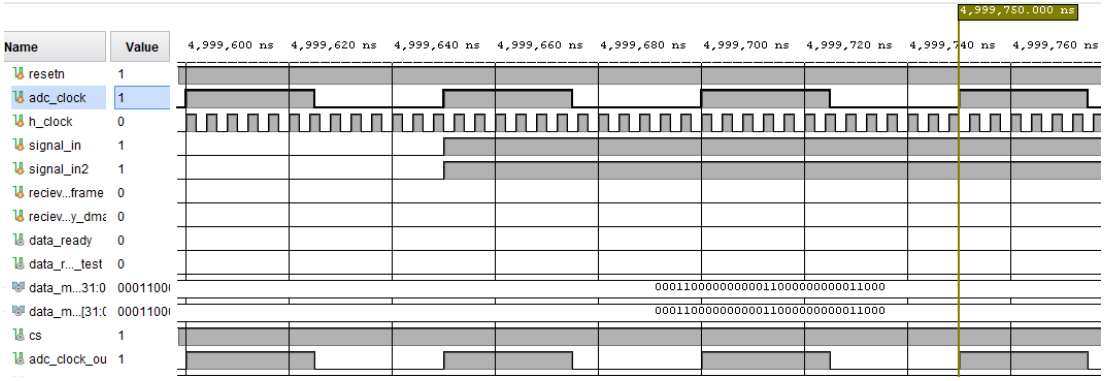


Figure 5.41: Simulation results for the clock signals generated from the adc_0 module

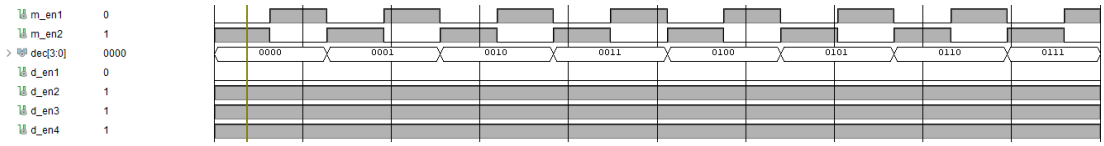


Figure 5.42: Simulation results of the multiplexer address signal mux[4:0] and multiplexer enable signals mux_en1 and mux_en2 issued by the the adc_0 module.

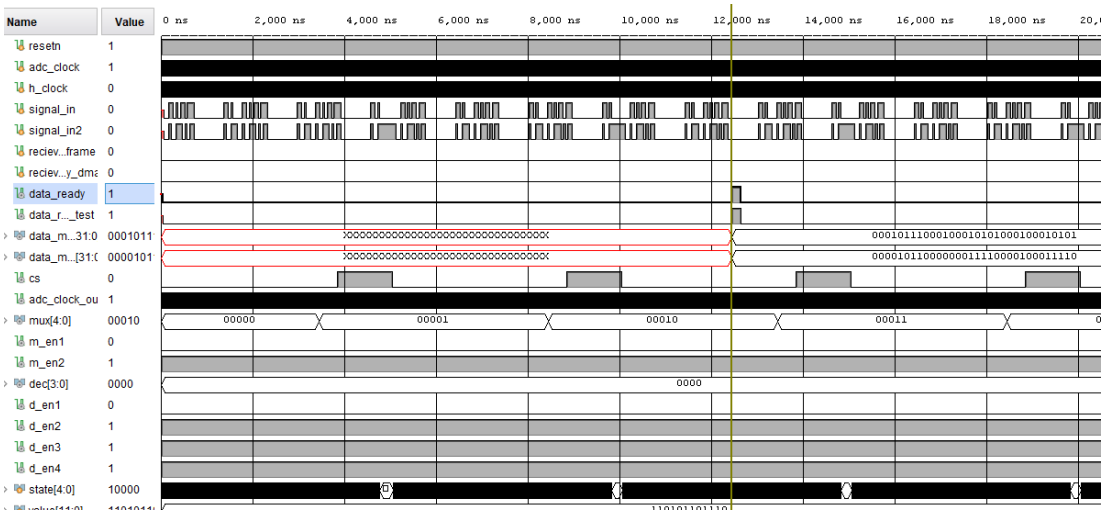


Figure 5.43: Simulation results for multiple ADC readings including all the input/output signals to and from the adc_0 module

Multiplexer enable signals (mux_en1 and mux_en2) accurately interchange between enable (1) and disable (0) states so that only one multiplexer samples 30 sampling electrodes at a given time. Thus multiplexer address signal (mux[4:0]) should gradually increment from 5'b00000 to 5'b11110 (0 to 30). Once mux[4:0] reaches 5'b11110, multiplexer enable signals should toggle and the multiplexer addresses should reset to 5b'00000 and gradually increment upto 5'b11110. This cyclic process should continue indefinitely. This functionality can be clearly observed in the adc_0 module as depicted in the Fig. 5.42.

Meanwhile, decoder address signal (dec[3:0]) should increment from 4'b0000 to 4'b1111 (0 to 15) as a decoder has 16 output pins connected to 15 row driving electrodes. One increment in the decoder signal should occur only after an entire row has been scanned by all the 60 sampling electrodes. Hence, decoder signal increment should take place only when the the mux_en signals are toggled twice. As the dec[3:0] is a shared address bus among four decoders, dec_enX (where X=1,2,3,4) signals should be selected to enable a given decoder. This process is illustrated in the Fig. 5.42 In the present simulation, decoder one was enabled by driving dec_en1 signal to low state and retaining dec_en2, dec_en3, and dec_en4) at high state.

Afterwards, the capability of the developed adc_0 module to effectively buffer the most recent 32 bits of 12-bit ADC readings (signal_in and signal_in2), issue the data_ready signal (to the axi_lite_slave_0) once 32-bits of data are acquired and load the content on to both data_memory [31:0] and data_memory2 [31:0] ports for respective clusters was evaluated. Once, 32 bits are acquired by the internal buffers of the adc_0, they are loaded onto data_memory and data_memory2 ports and data_ready signal is asserted accurately.

Moreover, it was noted that, as long as 32 bits are buffered by the adc_0 module, the data_memory and data_memory2 ports are not occupied. As soon as 32 bits are acquired and data_ready signal is raised, all 32 bits are dumped onto the two ports and latched on until the next 32 bits are loaded onto them. This functionality is profoundly distinguishable in Fig. 5.43. At the start, it was apparent that the data_memory and data_memory2 ports are at undefined (X) state. Once, 32 bits are acquired, data_ready is asserted and cs is raised, the ports are updated with the acquired values. However, during the first ADC reading, it was observed that initial transients result in the loss of first two ADC readings. Given that it could easily be addressed at the software level, not measurements were taken to rectify that in the APSoC implementation.

5.9 Python Graphical User Interface Implementation

For visualization of the acquired data from the piezoresistive sensor array a Graphical User Interface (GUI) program called Pressure Data Visualization" was developed using tkinter and Python as shown in Figure 5.44. In addition, matplotlib.pyplot library was used to map the adc values in the 2D space. Matplotlib.animation library was used to update the plot in real-time. Python serial library was used to implement serial connectivity between the computer and the APSoC and Python time library was used to generate timing delays. Seaborn library was used to generate a heatmap and numpy library was used to store the data into a temporary buffer once received.

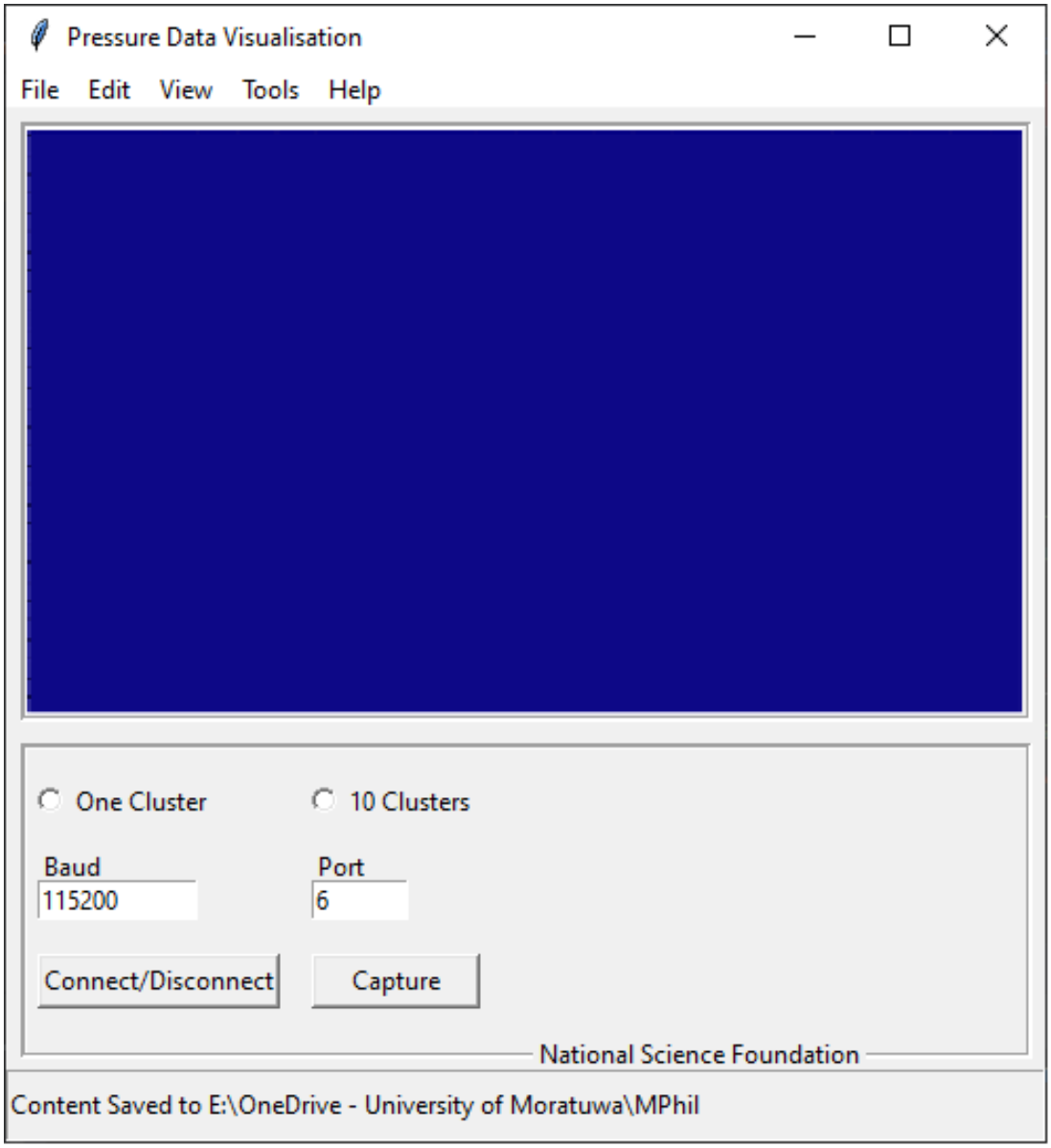


Figure 5.44: The GUI developed using tkinter and Python to visualise data acquired from the piezoresistive sensor array

A heatmap is a two dimensional data visualization technique comprising of rectangular tiling arranged into rows and columns such that colour in each tile represents a value within a given data range [179]. In this instance, a tile in the heatmap represents the position of the sensel in X and Y planes of the piezoresisitive sensor array and the colour gradient represents the intensity of pressure. Reverse plasma colour color palette was used for the present design. Therefore, when no load is applied on the

sensor array the ADC reading is will be around 4096 (2^{12}) which is mapped to blue colour and lowest resistance measurable (1 kΩ correspond to an ADC reading around 70) will be mapped to yellow colour.

The serial port to which the APSoC is connected should first be opened to initial communication between the two devices. The incoming ADC data are then temporarily stored in a numpy array of $rows \times columns$ size. Using a special function, the one dimensional numpy array was converted to a two dimensional array which was converted into a heatmap by the seaborn library. The heatmap was updated once all the adc readings of the corresponding array size are acquired.

Using the controllers on the GUI window, it was possible select whether one cluster or entire 10 clusters are being measured and the output screen (blue) will be adjusted accordingly. The desired baud rate and the serial port to which the APSoC device is connected could be configured. Connect/Disconnect button allowed establishing and interrupting serial communication between the APSoC and the computer. Capture button will take a snapshot of the current output screen and save it in the default directory shown at the bottom of the window as a PNG image. The "Pressure Data Visualization" program interface can be configured using the tools accessible through menu bar.

The GUI development, debugging and verification was done using the 8×8 RSA (Section 5.3.3) as it was easier to map 64 sensels in 2D space and debug than 3000 sensels. However, the program was developed in such a way that number of rows and number of columns are defined initially along with baud rate and serial port so that these parameters could be changed at will before executing the program. Upon verification of the Python program via the 8×8 RSA model as shown in Figure 5.45 GUI was tested on one cluster of the piezoresisitive sensor array.

Figure 5.46 demonstrates an instance where a book was placed on one cluster of the piezoresistive sensor array to visualize its pressure distribution via the Python GUI. Book was pressed from center to create a pressure gradient across the surface of the

Figure 5.45: Development of the Python GUI program by debugging it with the 8×8 RSA model

book. Figure 5.47 denotes the visualization made for the arrangement shown in Figure 5.46.

It is evident from Figure 5.47 that the developed Python GUI has been able to map the corresponding ADC values to their respective positions in the 2D space predicting an accurate shape of the object. Moreover, the shape accuracy assessment discussed in Section 5.7.3 was conducted following the verification of the GUI functionality.

Figure 5.46: Book is placed on the piezoresisitve sensor array and pressed against the sensor array from center to generate an image in Python GUI

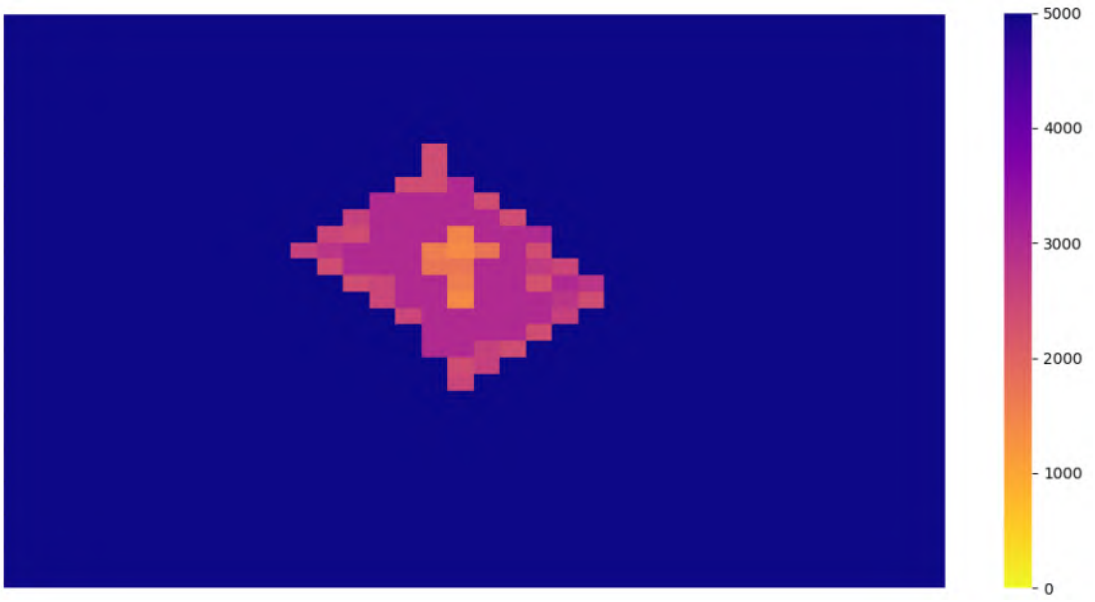


Figure 5.47: The GUI visualization when a book is placed on the piezoresisitve sensor array and pressed against the sensor array from center

5.10 Calibration of the Pedobarographic System

5.10.1 Exisiting Calibration Techniques

Calibration of sensors is of critical importance in any engineering application, as it ensures that the measurements are reliable, precise and reproducible [180, 181]. Although several sensor array calibration techniques have been utilized in reported literature, all these techniques can be categorized as static and dynamic calibration techniques as outlined below.

1. Static calibration
    (a) Calibrating individual sensels under different loading conditions using a Force Sensitive Resistor (FSR)
    (b) Placing individual weights (discs) of increasing mass
2. Dynamic calibration
    (a) Increasing continuous load from a linear actuator
    (b) Using a manometer wrapped around the sensor array

Static calibration techniques involve the application of discrete pressure on a single or a group of sensors and monitoring the output [181–183]. Force Sensitive Resistor (FSR) (Figure 5.48(a)) and standard weight discs (Figure 5.48(b)) have been employed to calibrate sensor arrays under static conditions [181]. The FSR technique has been used on sensor arrays with smaller sensor dimensions as it involves testing of individual sensors [181, 182]. Considering the limitations of FSR calibration method and the availability of resources, the technique involving the placement of weight discs on the piezoresistive sensor array to record the corresponding output was the most viable static calibration technique for our large piezoresistive sensor array.

Figure 5.48: Static calibration techniques for pedobarographic systems with piezoresistive sensor arrays. **(a)** Calibrating individual sensels under different loading conditions using a Force Sensitive Resistor (FSR). **(b)** Placing individual weights discs of increasing mass

Dynamic calibration quantifies the effect of hysteresis, drift and settling time of the sensels through a continuous loading mechanism [181, 182, 184]. Linear actuator based Instron machines and Minishaker machines used for material testing purposes are often used in calibration of individual sensors and manometer based techniques are often used in calibration of group of sensors under dynamic conditions.

Due to the limitations in availability of necessary hardware resources, only a static calibration was conducted on the pedobarographic system. Hence, the behaviour of the sensels during dynamic loading conditions have not been evaluated and the behaviour of the sensels in the presence of hysteresis, settling time and drift etc. were not identified during the current investigation.

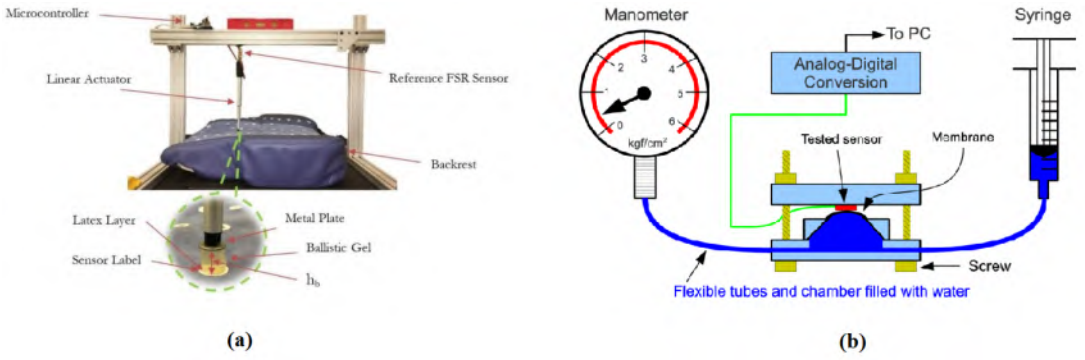


Figure 5.49: Dynamic calibration techniques for pedobarographic systems with piezoresistive sensor arrays. **(a)** Calibrating individual sensels under different loading conditions using a linear actuator. **(b)** Calibrating group of sensels under different loading conditions using a manometer

5.10.2 Static Calibration of the Piezoresistive Sensor Array

Static calibration of the implemented pedobarographic system was conducted using standard weight discs of 5 kg, 10 kg, 15 kg and 20 kg. Initially, the actual weight of all the disc was measured using a laboratory scale. Then, the selected weight discs were placed on the piezoresistive sensor array while recording the pressure distribution through the custom developed data visualization GUI (Section 5.9). Weights were stacked on top of each other as shown in Figure 5.50, such that their center of masses align at the center with 5 kg increments until a total maximum of 100 kg.

The python program used in the GUI was modified such that it records the ADC values of all the loaded sensels of a given image frame for a given combination of weight discs. The image frame captured for a combination of 65 kg is shown in Figure 5.51. One average ADC value was then calculated from all the ADC values pertaining to loaded sensels. The primary assumption during this calibration process was that a the composition of the weight discs are homogeneous and the weight distribution of each disc is uniform. The calculated average ADC value was then plotted against the measured weight from the laboratory scale as shown in the Figure 5.52.

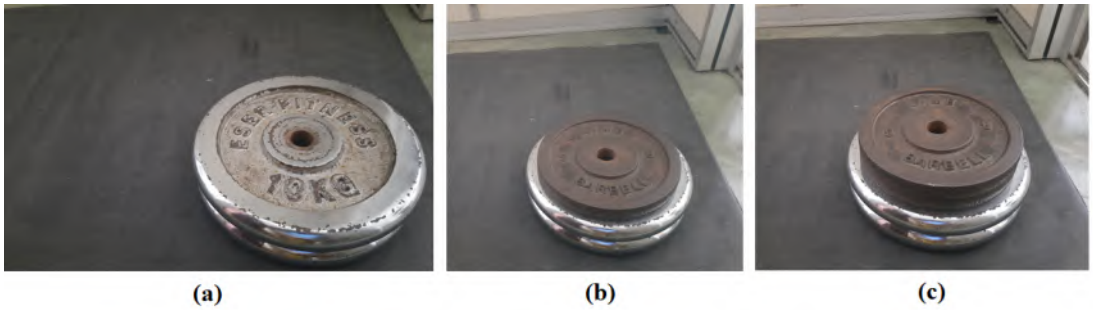


Figure 5.50: Calibration of the pedobarographic system by placing weights. Weight combinations of **(a)** 20 kg, **(b)** 25 kg and **(c)** 30 kg are shown here.

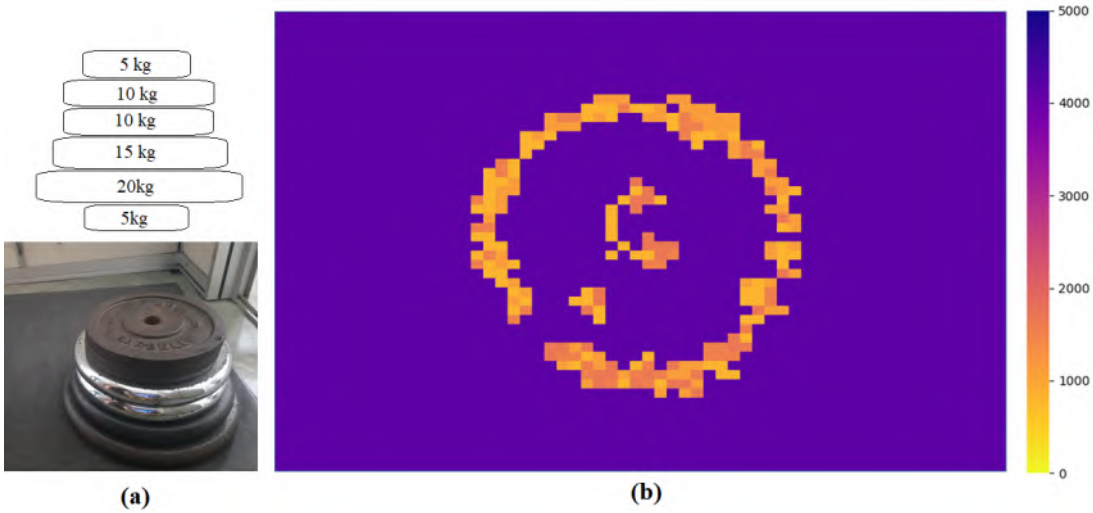


Figure 5.51: The visualization made **(b)** for a tack of 65 kg of weight discs **(a)** through the python GUI

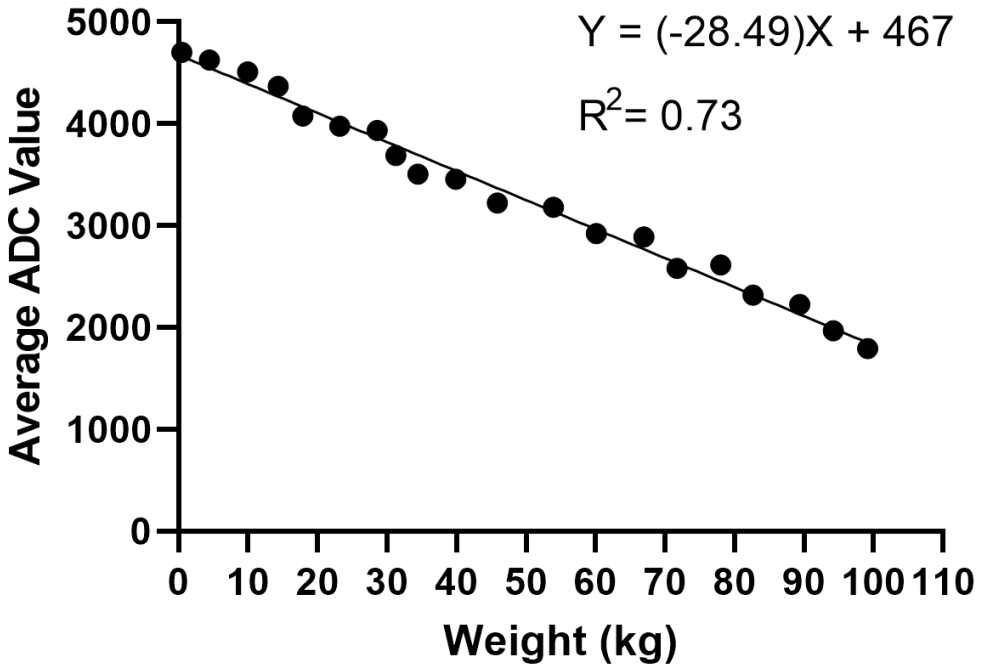


Figure 5.52: The calibration curve of average ADC value against measured weight of the disc.

A regression analysis was conducted for the averaged ADC value from the python GUI against its corresponding weight combination (in kg) which yielded the Equation 3 with a coefficient of determination of $R^2 = 0.73$ as indicated in Figure 5.52. The linear relationship of the piezoresistive sensor array is slightly less than the linear relationship exhibited by the readout circuit and the 8×8 RSA model ($R^2 = 0.95$) demonstrated in Figure 5.33. This can be due to manufacturing variations and material irregularities of the piezoresistive sensor array 5.7. The existing mismatch between sensels could be mitigated through normalization of the sensels by calculating a gain factor and multiplying each sensel reading with the gain factor as demonstrated by Campos et al. [181]. However, normalization of sensels was not performed during the present implementation.

$$Y = (-28.49)X + 467 \tag{3}$$

5.11 Validation of the Pedobarographic Device

The next objective was to compare the developed system against a commercially available plantar pressure measurement system to validate and evaluate the performance of the implemented system in terms of measurement accuracy and the shape accuracy. Therefore, a commercial platform sensor array system, RSscan®, owned by the FeetCare Singapore (Pvt) Ltd. located at the Asiri Surgical (Pvt) Ltd. (refer Figure 5.53)was used to compare and validate the developed system.

Figure 5.53: The RSscan® platform sensor array system which was used to compare and validate the developed pedobarographic system

The primary approach towards validation was to obtain measurements from the RSscan® system and the developed pedobarographic system separately using the same combination of weights (standard weight discs and feet) and evaluate the results in terms of measurement accuracy and shape accuracy to determine the overall accuracy of the systems against known weights and shapes. First, both the platform sensor arrays were laid on an even surface. Then, weight discs were placed on top of the sensor arrays. Then a cross comparison was conducted for the measurements

obtained from each system under the same combination of weight discs. Figure 5.54 shows the measurement obtained from the RSscan® system for the same combination of 65 kg weight discs used during the calibration of the implemented system which was shown in Figure 5.51). Figure 5.55 demonstrates a side-by-side comparison of the measurements from both systems shown separately in Figure 5.51 and Figure 5.55. Similarly, Figure 5.57 and Figure 5.56 shows the measurements across both systems when weights of 35 kg and 25 kg had been arranged.

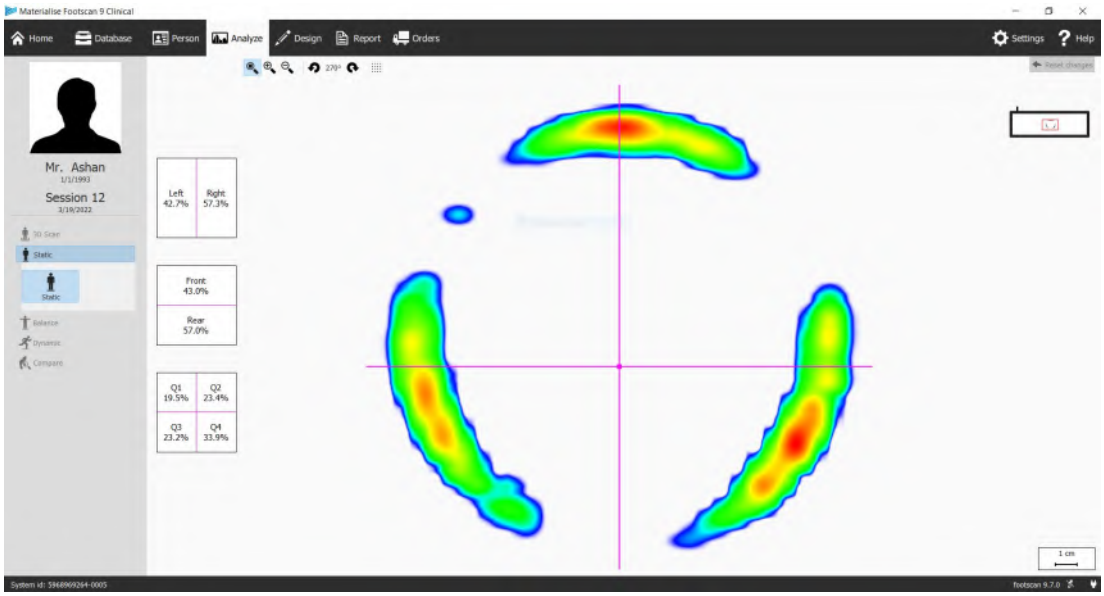


Figure 5.54: The visualization and readings obtained from the RSScan® platform sensor array system for the same arrangement of 65 kg weight discs obtained from the developed pedobarographic system as shown in Figure 5.51.

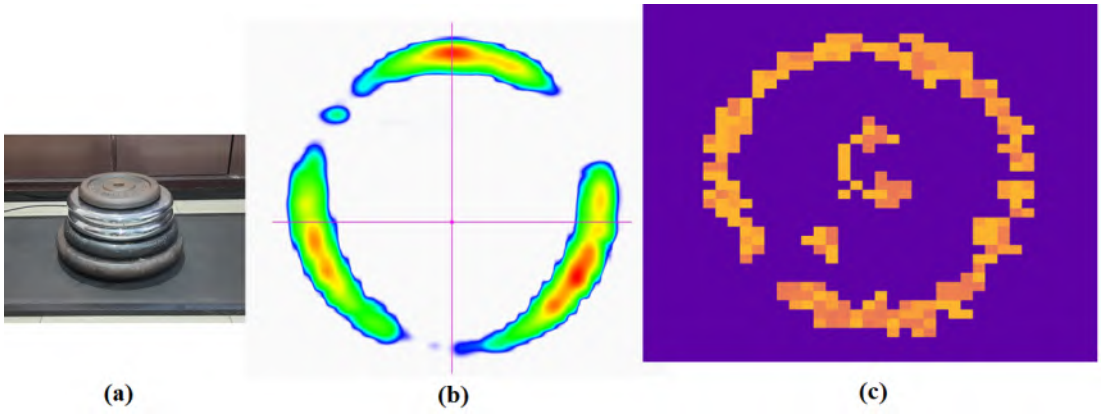


Figure 5.55: A side by side comparison of the same**(a)** weight discs arrangement visualized by the RSscan® and the developed pedobarographic system for the same weight weight discs arrangement.

Measurements from the RSscan® system did not generate absolute values, rather weight distribution was mapped as a percentage for the four quartiles (Q1,Q2,Q3 and Q4) as shown in Figure 5.56, 5.57 and 5.58. In addition to the four quartiles, the percentage weight distribution was calculated for the front side (Q1,Q2), rear side (Q3,Q4) left side (Q2,Q3) and right side (Q1,Q4) .

As a parameter, percentage weight distribution had no significant bearing in the cross comparison between the two systems. In an effort to conduct an appropriate comparison, readings obtained from the implemented system was also demarcated as a percentage weight distribution. Since there was no algorithm developed to estimate the center of mass and the separation of quartiles, the center of mass was determined manually from the probable center of the measurement and four quartiles were generated extending from the center of mass as shown in Figure 5.56, 5.57 and 5.58. The weight concentration in each quartile was calculated indirectly by calculating percentage from the ratio of total ADC values in each quartile to the total ADC values of the measurement. However, given the negative linear association between ADC value and weight in the implemented system (Figure 5.52), high ADC value in a given quartile meant lower weight distribution. Hence, the inverse percentage weight distribution (IPWD) was calculated according to Equation 4.

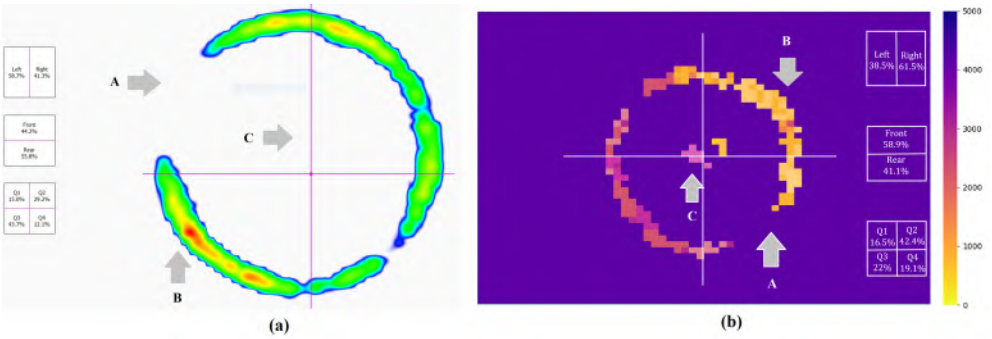


Figure 5.56: A side by side percentage weight distribution comparison of 25 kg of weight discs arrangement measured by the **(a)** RSscan® and **(b)** the developed pedobarographic system

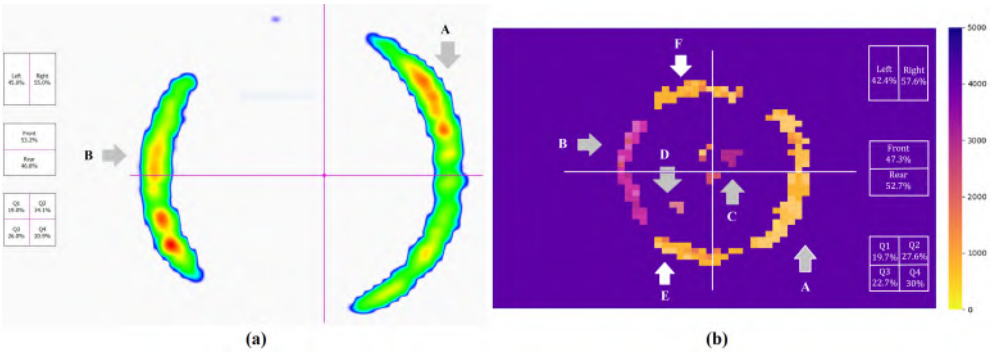


Figure 5.57: A side by side percentage weight distribution comparison of 35 kg of weight discs arrangement measured by the **(a)** RSscan® and **(b)** the developed pedobarographic system

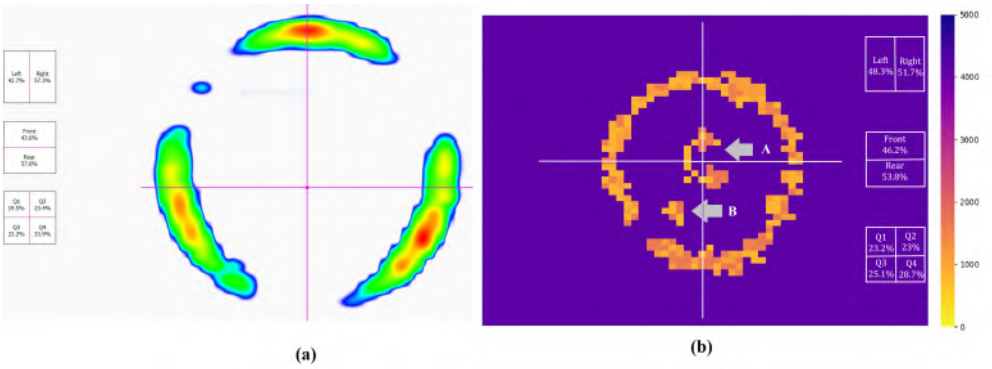


Figure 5.58: A side by side percentage weight distribution comparison of 65 kg of weight discs arrangement measured by the **(a)** RSscan® and **(b)** the developed pedobarographic system

$$IPWD(\%) = 1 - \frac{\text{ADC Value of quartile}}{\text{Total ADC values of all four quatiles}} \times 100\% \quad (4)$$

In the cross validation between the systems during 25 kg loading condition (Figure 5.56), it can be observed that the more weight is concentrated on the right side of the measurement (61.5%) from the implemented system in contrast to that of the RSscan® system (58.7%) which has a prevalence towards the left side. Similarly, more weight concentration is observed at the front side of the developed system (58.9%) in contrast to the RSscan® system which shows a bias towards the rear side (55.8%). However, it is comprehensible that the orientation of the weight disc which has no clear front, rear, left or right side is key to the discrepancy that was observed. Nonetheless, we could clearly see a similarity between the weight distribution towards the left/right sides (61.5% versus 58.7%) and front/rear sides (58.9% versus 55.8%).

A similar comparison involving front and rear, left and right, was performed for weight distributions of the 35 kg measurement from both systems as denoted in Figure 5.57. Both systems had a bias towards the right side of 35 kg with 55% percentage weight distribution observed from the RSscan® system and 57.6% observed from the developed system. Moreover, the front measurement from the implemented system (47.3%) corresponded with the rear measurement of the RSscan® system (46.8%).

However, in the case of 65 kg measurements, both implemented system and the RSscan® system showed similar percentage weight distributions in front side with 51.7% and 57.3% respectively. Meanwhile, both rear sides experienced more percentage weight distribution which were 53.8% and 57% respectively. Although, the orientation of the weight discs plays a pivotal role in the percentage weight distribution, with more weight the discrepancies were observed to diminish which could be a result of the weight disc getting firmly in contact with the piezoresistive sensor array.

Although, the measurement accuracy could not be quantified precisely due to the percentage distribution analysis, shape accuracy analysis through visual inspection made it clear that the shape estimation by the impelemented pedobarographic system was slightly superior to the RSscan® system during the analysis with standard weight discs as observed from Figure 5.56, 5.57 and 5.58.

In Figure 5.56, a similar weight distribution in regions denoted by A and B is observed. An unloaded region A is visible in Q2 and Q4 in both systems as shown in Figure 5.56 **(a)** and 5.56 **(b)** respectively. Similarly, more weight concentration can be observed in region B in both systems. However, the inner ridge of the weight disc (region C), is not indicated in the RSscan® system (Figure 5.56 **(a)**) in contrast to the implemented system. Moreover, in Figure 5.57, a similar high (region A) and low (region B) weight distribution can be observed. Although, absent of region C is prominent across all measurement shown in Figure 5.56, 5.57 and 5.58, absence of regions D,E and F (in Figure 5.57 **(b)**) is remarkable. However, at higher weights such as 65 kg (Figure 5.58), it can be observed that an almost uniform weight distribution in both systems with regions B and C (inner ridge of the weight disc) absent. The region D in (Figure 5.57 **(a)**) and (Figure 5.58 **(a)**) could be a result of the surface of the weight disc coming into contact with the piezoresistive sensor array due to an unevenness or deterioration of the surface. The reason for the absence of certain regions in the measurements across weights 25 kg, 35 kg and 65 kg in the RSscan® system remains ambiguous.

However, it can be presumed that the system disregard weights beyond a predefined loading threshold although no evidence was found on the pedobarogram obtained from the RSscan® system in published literature. If Convoluted Neural Network (CNN) algorithms are deployed in the estimation of the shape of the object of concern from the RSscan® system (which is always a foot), it may be a result of the system attempting to estimate the shape from a predefined shape contour of the foot resulting in an alteration of the shape of the object. However, there is no evidence to justify this assumption.

The stated assumption of disregarding the weights beyond a predefined threshold

seems plausible when readings of a foot is measured from both the systems as shown in Figure 5.59. It is evident that both the systems has similar estimation of the shape and weight distribution. The heel (region A in Figure 5.59 **(a)** and **(b)**) metatarsal (region B in Figure 5.59 **(a)** and **(b)**) regions of the foot are bearing a higher load in both the systems and the shape of the foot has been accurately determined by both the systems.

However, it is worthy to note that the image from the developed pedobarographic system appear to be pixelated. The reason being, the python GUI displays the raw measurements as a 2D array of pixels corresponding to the intensity of measured pressure from each sensel without conducting any image processing, pixel normalization, interpolation or smoothing. Nonetheless, through the effective use of interpolation algorithms (eg. 2D spline interpolation) and smoothing algorithms (eg. Gaussian smoothing) a similar image as of the RSscan® system could be obtained. By changing the python colour map from "Plasma" to "Summer" the measurements from the implemented system would map between green and yellow spectrum rather than blue and yellow spectrum of "Plasma". However, image processing and extraction of clinically significant features were beyond the scope of the present research.

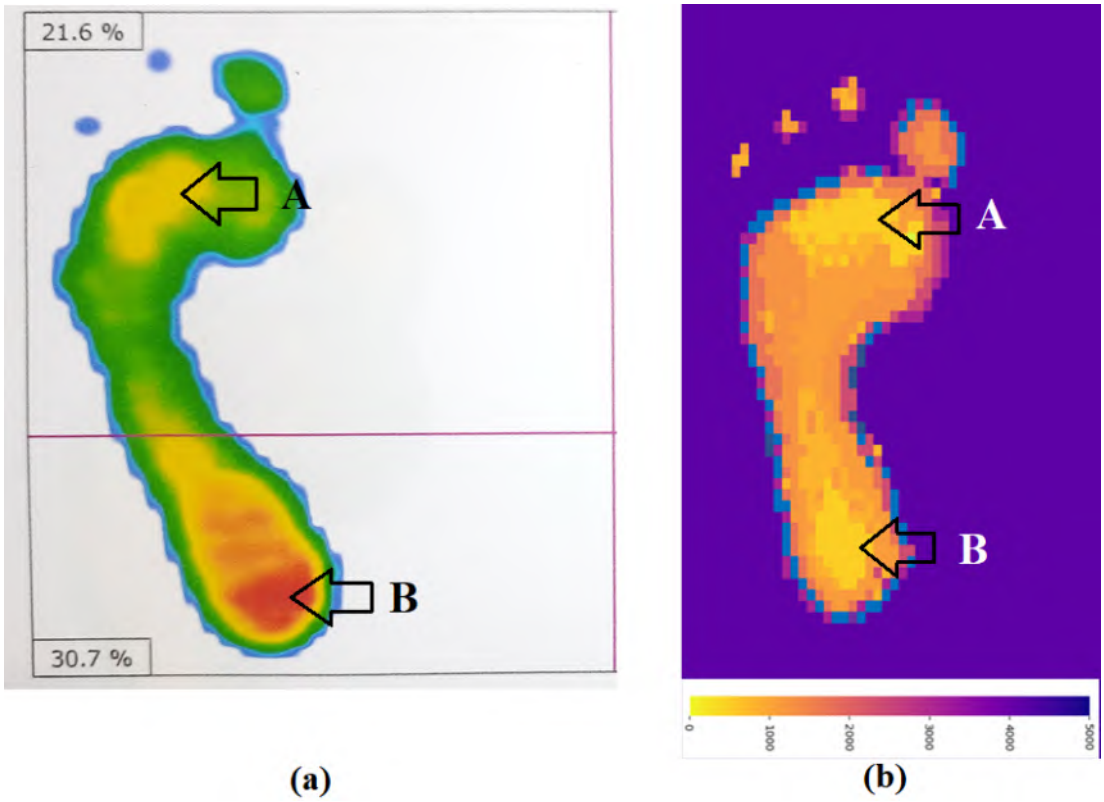


Figure 5.59: A side-by-side comparison of the same foot from the **(a)** RSscan® system and the **(b)** Implemented Pedobarographic System

Moreover, a cross validation between the percentage weight distribution of a foot from the two systems were initially planned. Anyhow, it appeared that the percentage weight distribution of both feet are taken into consideration by the RSscan® system when determining the four quartiles as shown in Figure 5.60. However, given that only one cluster was realized in the implemented pedobarographic system, only one foot could be scanned at a time. Hence, conducting a cross comparison between the percentage weight distribution of a single foot was not feasible.

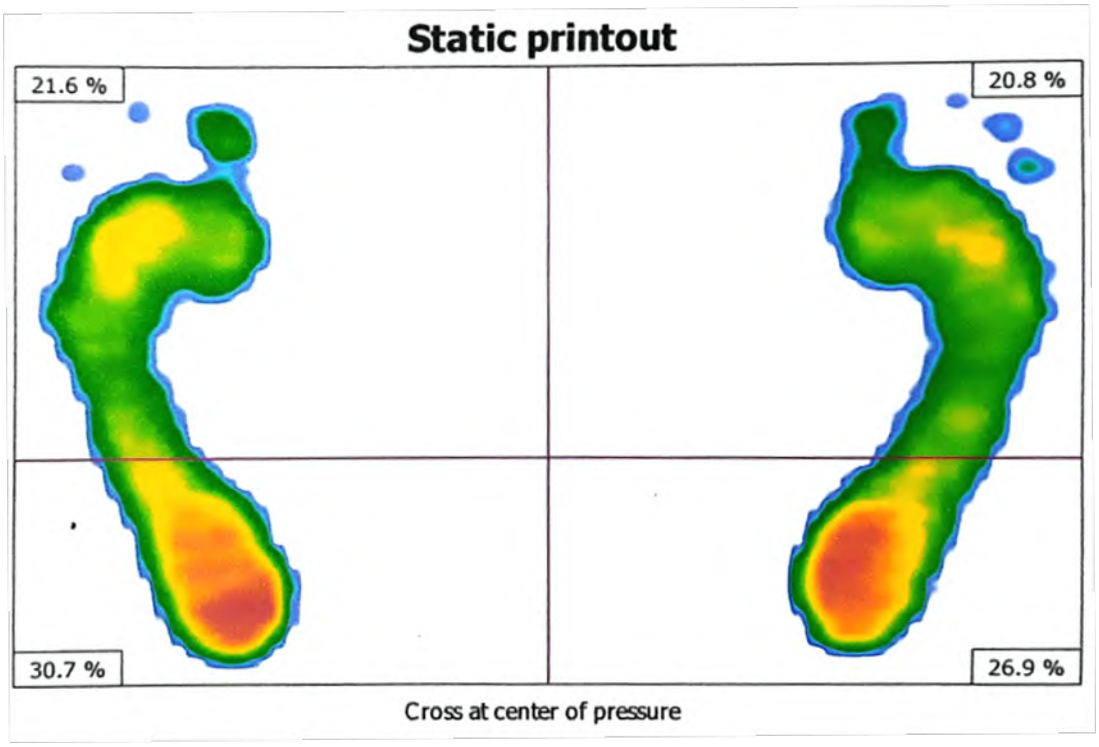


Figure 5.60: Measurement obtained from both feet from the RSscan® system. Percentage weight distribution of the two feet in four quartiles are indicated at top right/left corner

5.12 Limitations of the Implemented Scanning Mechanism

5.12.1 Data Synchronization

During the debugging process of the implemented Python GUI, it was observed that the overall data are shifted by two bits as shown in Figure 5.61 (a). In addition the first two bits were represented in yellow color indicating a very low resistance. This alteration was observed only during the opening frame and the data shift caused by this phenomenon propagated throughout.

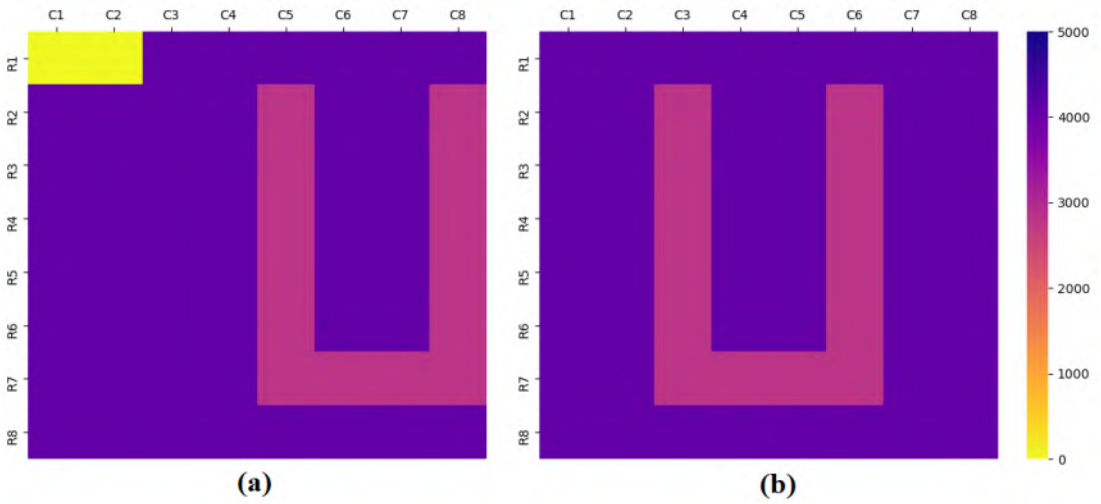


Figure 5.61: The data synchronization issue observed when implementing the GUI for data visualization. **(a)** The obtained visualisation through Python GUI when the letter U was formed on the 8×8 RSA. **(b)** The expected visualization through Python GUI for the shape formed on the 8×8 RSA

It was initially though that this error was due to the presence of harmonics or low settling time of the ADC during the opening frame which proved not to be the case upon logic analysis of the ADC. After careful investigations and observations it was noted that the reason for the initial shift of two bits were due to the structure of the data packet of the selected ADC as shown in Figure 5.62.

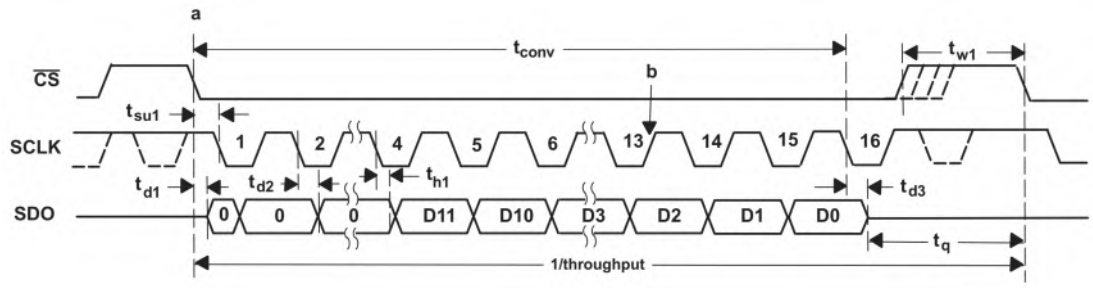


Figure 5.62: The timing diagram of the selected ADS7886 ADC durring normal operation

The serial ADC transmitted two leading zeros until the fourth clock cycle after which it started transmitting 12-bits of data (D11, D10, ... D0 from Figure 5.62) and our

Verilog HDL program was equipped to cater this functionality as shown in the Verilog code snippet below. However, All the subsequent frames except the opening frame responded accurately to the Verilog code. As the opening frame did not respond to any of the modifications at the Verilog side it was decided compensate for this bit shift at the software side in the Python GUI.

```
case(state)
    0:begin                     // start of new reading
        state<=state+1;         // no reading
    end
    1:begin
        state<=state+1;         // no reading
    end
    2:begin
        state<=state+1;         // no reading
    end
    3:begin
        state<=state+1;         // reading of D11
        data[31]<=signal_in;
        data2[31]<=signal_in2;
    end
    4:begin
        state<=state+1;          // reading of D10
        data[30]<=signal_in;
        data2[30]<=signal_in2;
    end
```

In the Python GUI development, a separate function was defined to acquire data such that if it is the opening frame (determined by a counter), the first two bits of the acquired serial data stored in a numpy array are ignored and used to generate the heatmap. However, if it is a subsequent data frame, then all the acquired bits will be considered. The described functionality by the defined matRead() function is given below. After these implementations, it was observed that the data synchronization issue had been resolved and the spatial data arrangement in the heatmap corresponded to the spacial object placement in the sensor array as shown in Figure 5.61 (b) where letter U formed at the center of the 8×8 RSA was visualized accurately.

```
def matRead():
```

```
    global count
    startTime = time.time()
    if count == 0:
        for j in range(0, numPoints_ini):
            dataList_ini[j] = int(getValues())
        oneCluster = np.array(dataList_ini[2:])
            .reshape(NR, NC)
        count += 1
    else:
        for j in range(0, numPoints):
            dataList[j] = int(getValues())
        oneCluster = np.array(dataList).reshape(NR, NC)
    print(oneCluster)
    print("\n Execution time = %.3f seconds\n"
        % float((time.time() - startTime)))

    return oneCluster

##Notes: NR = Number of Rows, NC = Number of Columns
```

5.12.2 Timing Delays

So as to guarantee optimum performance, the speed of operation is also critical apart from the accuracy. Although, our main focus was on improving the accuracy of the pedobrographic implementation, measures were taken to generate sufficiently high data rates. However, the readout circuit, APSoC and one cluster of piezoresistive sensor array could initially deliver a frame rate of only 1 Hz.

The timing response of all major components along the signal pathway were separately monitored to determine any bottlenecks in the readout circuit design. However, the output characteristics of all the individual components coincided with the expected requirements, suggesting that the transmission delay was not a consequence of readout circuit implementation. Next, it was decided to conducted a timing analysis of the implemented DAQ architecture in APSoC to determine whether source of timing delays are in the DAQ architecture. Anyhow, the DAQ architecture seemed to adhere to all the timing constraints related to design guidelines as shown in

the Figure 5.63 which is extracted from the timing report generated by Xilinx Vivado after conducting a timing analysis of the implemented modules (Section 5.8.3). The setup and hold times were observed to be in order, including a positive Worst Negative Slack (WNS) and a positive Worst Hold Slack (WHS) without any failing endpoints.

Design Timing Summary

Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	1.870 ns	Worst Hold Slack (WHS):	0.013 ns	Worst Pulse Width Slack (WPWS):	3.750 ns
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	8401	Total Number of Endpoints:	8401	Total Number of Endpoints:	3446

All user specified timing constraints are met.

Figure 5.63: The summary of the APSoC design timing constraints implemented via Xilinx Vivado

Hence, it became abundantly clear that the timing delays were persistent in data transmission between the APSoC and the computer. Further investigations revealed that there existed a delay in transmission of data from DDR3 memory of APSoC to computer. The reason being, when the APSoC is connected to the computer, the DDR3 memory of the APSoC which temporarily stores the ADC readings are being treated as an external storage connected to computer. Generally, when a typical storage device such as flash drive is connected, computer does not expect a change of the data in the memory without an intervening from the computer. However, in the APSoC, DDR3 memory is updated in real time. As a result, upon the completion of the initial data transmission to the computer, re-transmission is blocked by the computer due to cache invalidation at the computer side resulting in transmission time-out. After that, the next transmission starts as a new transmission which also persists until transmission time-out, resulting in drastic reduction in the communication speed. However, through several optimizations and improvements, the frame rate was improved to 40 Hz. Although, this attained frame rate is sufficient for static data acquisition, it is not applicable for dynamic data acquisition.

Although, the USB 2.0 port has a rated maximum data rate of 480 Mbps (Mega-bits per second) [185] only a data rate of 30 Mbps was attainable under practical circumstances. This was because USB communication protocol is a half-duplex protocol, so that data flows only in one direction at a given time. Therefore, the theoretical maximum could be achieved only during high speed data transmission in only one direction [185, 186]. However, significant improvement of the data rate could be attained if data transmission is conducted via a USB 3.0 (5 Gbps), USB 3.1 (10 Gbps) or Ethernet (10 Gbps). However, the selected Xilinx APSoC device did not incorporate a USB 3.0 or 3.1 port but an Ethernet port. Therefore, even higher data rate could be attained if data were transmitted via Ethernet. Nevertheless, the reason for selecting the USB interface for data in the present implementation was because our main focus was on improving accuracy rather than data rate. Transmission through USB could easily be monitored via a terminal software which proved to be significantly important in debugging and implementation of data communication protocol.

5.12.3 Implementation of all Ten Clusters of the Pedobarographic System

The pedobraographic system was originally intended to be implemented with ten clusters as described in Section 3.7 such that two clusters share one readout circuit. The conceptualized design is shown in Figure 5.64. By utilizing the parallel data acqusition and processing capabilities of the PL of the APSoC, each cluster transmits data to the APSoC parallelly through separate ports, which are processed parallelly and transmitted to the computer. Had the data rates attainable are inadequate, the transmission protocol could easily be upgraded to Ethernet to facilitate more data transmission at a higher rate.

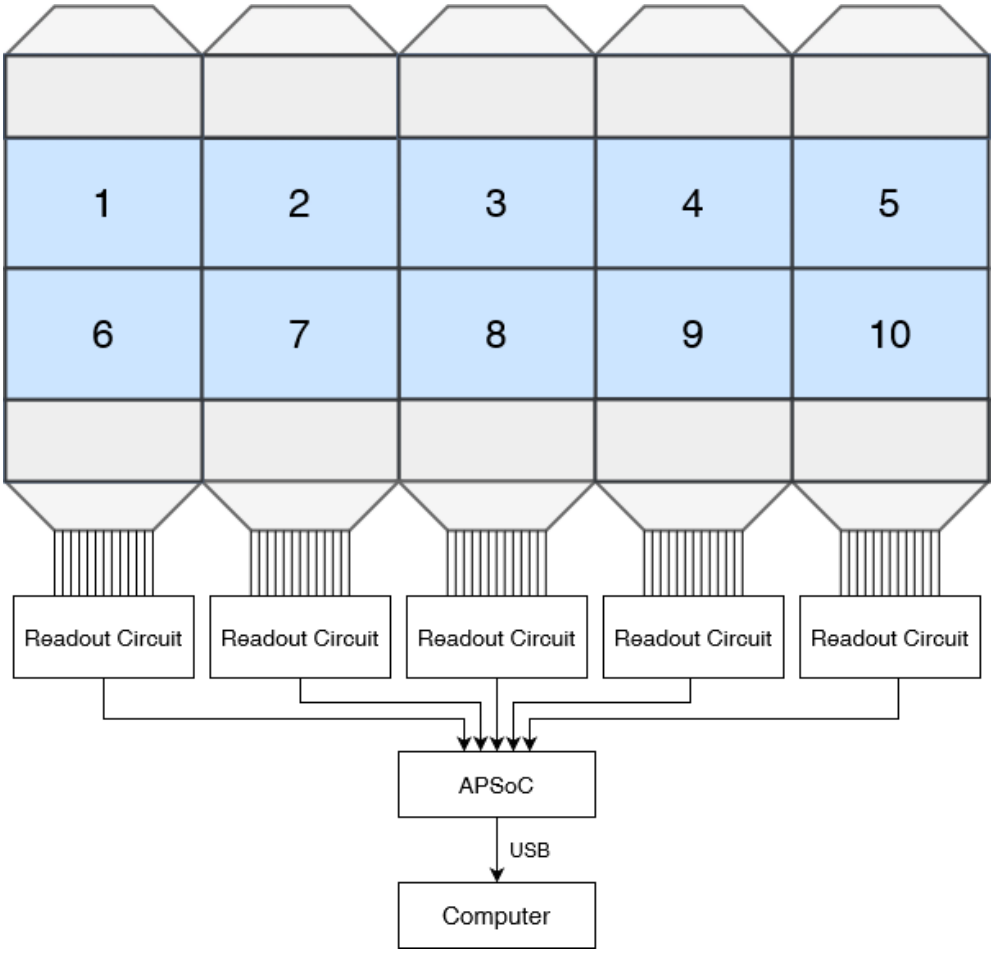


Figure 5.64: The overview of the whole pedobarographic system. A given readout circuit access two clusters (1,6), (2,7)...(5,10)

Nonetheless, only one readout circuit was physically realized during the initial phase of the research so that validation of the readout circuit, identification of any design flaws and required improvements followed by developing the DAQ architecture and implementing the data transmission mechanism could be identified and tested before implementing the whole system. If the designed readout circuit meets all the design, power and timing criteria, then, the rest of the four readout circuits could easily be implemented. Since these readout circuits operate in parallel to the realized readout circuit, it was just a matter of scaling up the design to accommodate four additional readout circuits with repeated IPs that operate parallely to ultimately generate 8 separate ADC values. Besides, all the rows in all the ten clusters are accessed using

the same shared signal bus, while all other control signals such as multiplexer enable signals, address signals and decoder enable signals and address signals are shared among all the readout circuits.

However, the funding for the project was terminated in the midst of the research unfortunately (NSF Research Grant ID: RPHS 2016 DTM 02). The cost of implementation of a single readout circuit amounted to nearly Rs. 423,000 at the time of calculation. Therefore, it was impossible to implement the remaining readout circuits entirely due to financial restrictions. It was later decided during progress evaluations to interface the developed readout circuit with one cluster and show that the implementation is accurate in terms of crosstalk suppression and through a a simulation study for the entire system as discussed in Section 5.7 and Section 5.8.1 respectively. The basis of the alternative approach was that, by implementing and validating the accuracy at hardware level in both readout circuit and APSoC it was reasonable to argue that the functionality of the rest of the readout circuits also demonstrate same degree of accuracy due to the parallel operation established. The only bottleneck that could arise would in serial data transmission via USB 2.0 which could be overloaded due to the high amount of data. However, this could be addressed simply by upgrading the data transmission protocol to Ethernet.

The APSoC resource utilization provides an overview of the the internal utilization of logic, (input/output) I/O and memory resources for the implemented design. A comparison between the on chip resource utilization for one readout circuit and all five readout circuits in the pedobarographic system is illustrated in Figure 5.65 (a) and (b) respectively. Although, the resource utilization have increased when scaling the design from one readout circuit to five, it is worthy of note that the percentage of increase in resource utilization has not increased proportionally. Table 5.5 summarizes the total number of resources utilized when implementing the DAQ architecture for all ten clusters.

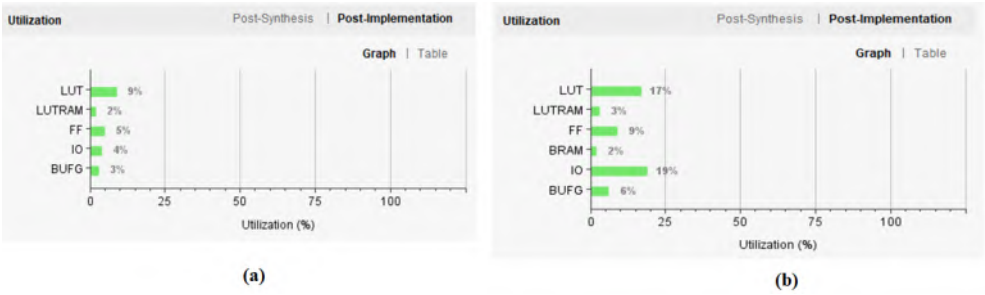


Figure 5.65: **(a)** On chip resource utilization for the implemented DAQ architecture for one cluster. **(b)** On chip resource utilization for the implemented DAQ architecture for all ten clusters simulated via Xilinx Vivado

Note: LUT: Look Up Tables, FF: Flip-Flops, BRAM: block-RAM, DSP slices, input/outputs (IO), and BUFG: Buffer Global Clock

Table 5.5: On chip resource utilization for all ten clusters of the pedobarographic system in the APSoC

Resource	**Utilization**	**Available**	**Utilization %**
LUT	3006	17600	17.08%
LUTRAM	154	6000	2.57%
FF	3225	35200	9.16%
BRAM	1	60	1.67%
IO	19	100	19%
BUFG	2	32	6.25%

The comparison of power consumption when implementing one cluster in APSoC and all ten clusters is shown in Figure 5.66 (a) and (b) respectively. Owing to the parallel processing capabilities, the power consumption in data acquisition from all ten readout circuits via APSoC DAQ architecture is only slight higher than the from one readout circuit. This further ascertain the significance of implementing the proposed pedobarographic system using an APSoC.

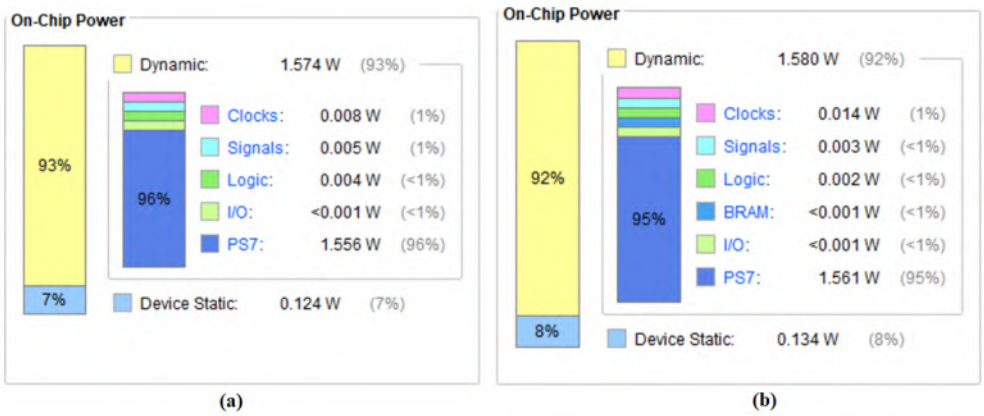


Figure 5.66: **(a)** Power dissipation of the implemented DAQ architecture for one cluster. **(b)** Power dissipation of the implemented DAQ architecture for all ten clusters simulated via Xilinx Vivado

CHAPTER 6

Pedothermographic Assessment Tool

6.1 Introduction

This chapter outlines the development process of the proposed pedothermographic assessment tool which can be used to determine the point and regional temperature of the foot plantar of patients exhibiting initial signs of PAD complications. The key elements covered in this chapter are listed below.

1. The structural overview of the implemented system
2. Implementation of the enclosed feet scanning unit
3. Implementation of the data acquisition and the processing system
4. Implementation of the image visualization and the analysis tool

Note that, the implementation and subsequent analysis of the pedothermographic assessment tool was a peripheral objective of the present research. Therefore, I only focused on the implementation of a fully functional pedothermographic assessment tool.

6.2 Overview of the Pedothermographic Assessment

The pedothermographic assessment tool was implemented with three main units, namely, the enclosed feet scanning unit, the data acquisition and processing unit, and the image visualization system as shown in Figure 6.1. The present work was inspired by the systems developed by Madarasinghe et al. [187] and Van Netten et al. [36, 151].

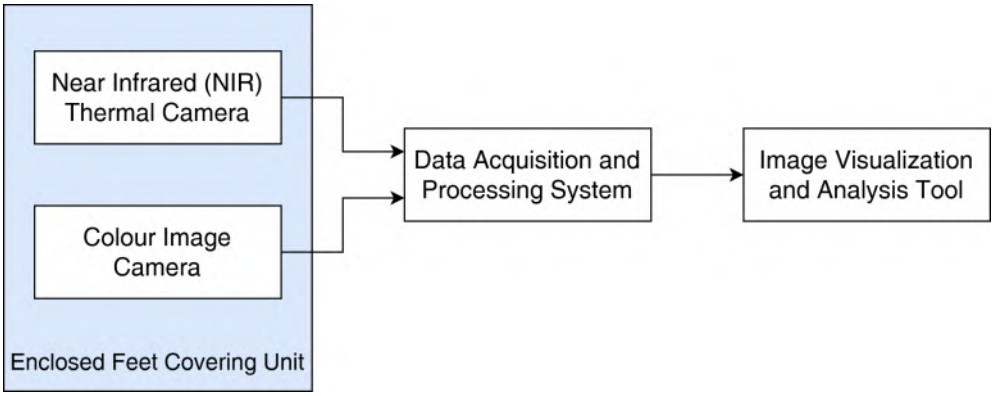


Figure 6.1: The structural overview of the implemented pedothermographic assessment tool consisting of the the enclosed feet covering unit, the data acquisition and processing unit and the image visualization system

The enclosed feet scanning unit in Figure 6.1 is the hardware especially developed to facilitate routine diabetic feet scanning at a diabetic clinic (refer Section 6.3 for the description and the Figure 6.6 for the final device). A Raspberry pi 3B+ singe board computer (SBC) was used as the data acquisition and processing system (Section 6.4) and provisions were made to visualize the images obtained from the system either with an external display monitor or a laptop computer (Section 6.5).

6.3 The Enclosed Feet Covering Unit

The enclosed feet scanning unit comprised of two sensors, mounted on a movable rod and a cushioned structure on which the patients' feet can be rested. A thermal camera, which is the main sensor of the implemented system, was responsible for recording the temperature distribution of the foot plantar. A colour image camera was also used to obtain a color image of the foot plantar to identify the foot contours, regions of interest and a capture any visual anomalies on the foot plantar.

Moreover, a special enclosing door that opens upwards (Figure 6.6 (a)) and closes downwards (Figure 6.6 (b)) after resting patient feet was built using wooden panel wrapped in cushion (for patient comfort).

6.3.1 Component Selection

Selection of components was critical since the accuracy of the implemented system relied heavily on the accuracy of the used sensors. To implement the system using infrared thermography which is gaining recognition as a high accuracy and high efficiency pedothermographic assessment tool (Section 4.4, robust, contactless, high resolution infrared theromographic sensor was required. Based on the recommendation of Madarasinghe et al. [187], a FLIR Lepton 3B+ thermal camera (Figure 6.2 (a)) and a Raspberry pi camera module v2 (Figure 6.3) were used for thermal and colour image acquisition respectively. A list of important specifications of the two imaging sensors are given in Table 6.1.

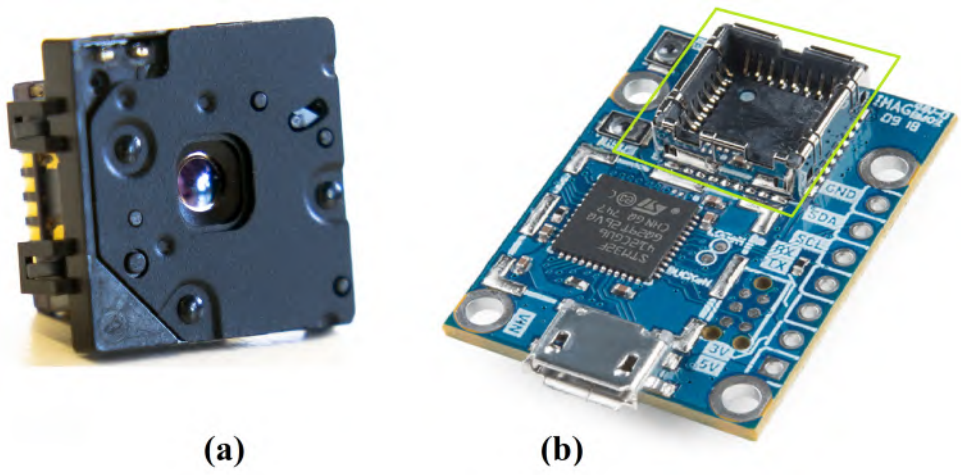


Figure 6.2: **(a)** The Lepton 3B+ thermal imaging sensor and **(b)** Purethermal 2.0 breakout board which houses it and interfaces it with the DAQ system. The Lepton 3B+ is fixed onto the socket highlighted with the green quadrilateral

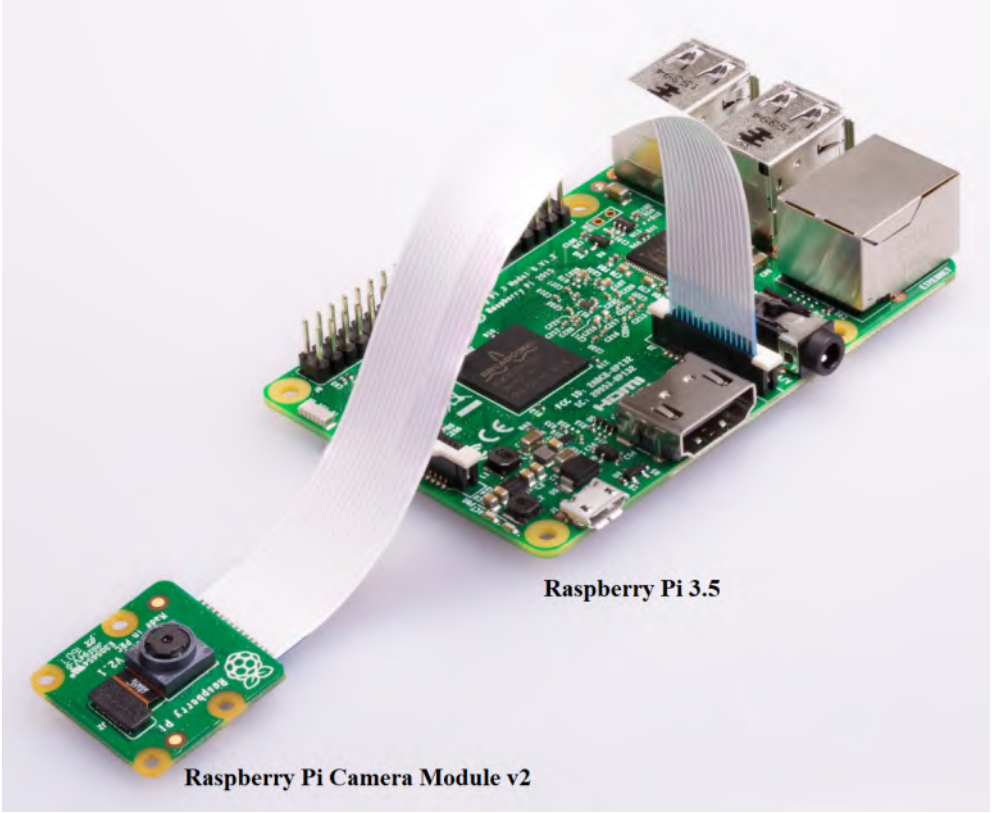


Figure 6.3: The Raspberry pi camera module v2 and the Raspberry pi 3B+ SBC which functions as the DAQ and processing system

Table 6.1: Specifications of the selected sensors for thermal image acquisition and colour image acquisition

Characteristic	**Thermal camera**	**Colour Image Camera**
Sensor	Microbolometer	Sony IMX219 CMOS
Pixel Resolution	160×120	8MP (3280×2464)
Thermal Sensitivity	0.050°C	–
Thermal Accuracy	$\pm$ 2°C	–
Frame Rate	9 fps	30 fps
Aperture size	f/1.1	f/4
Field of View	56°	42°
Communication Interface	I_2C and SPI	2-wire

6.3.2 Model Development using Solidworks®

After the sensor selection, model for the pedothermographic assessment tool was developed in Solidworks® 2018 SP4. The feet scanning unit was designed first. Dimensions of the enclosed feet scanning unit was determined based on the average distance between two feet when resting and the minimum distance required from the imaging sensor to the feet based on its field of view [187]. Thus, 75 cm$\times$ 57cm$\times$40 cm box was designed using stainless steel to mount the cameras and rest the feet for scanning as shown in Figure 6.4.

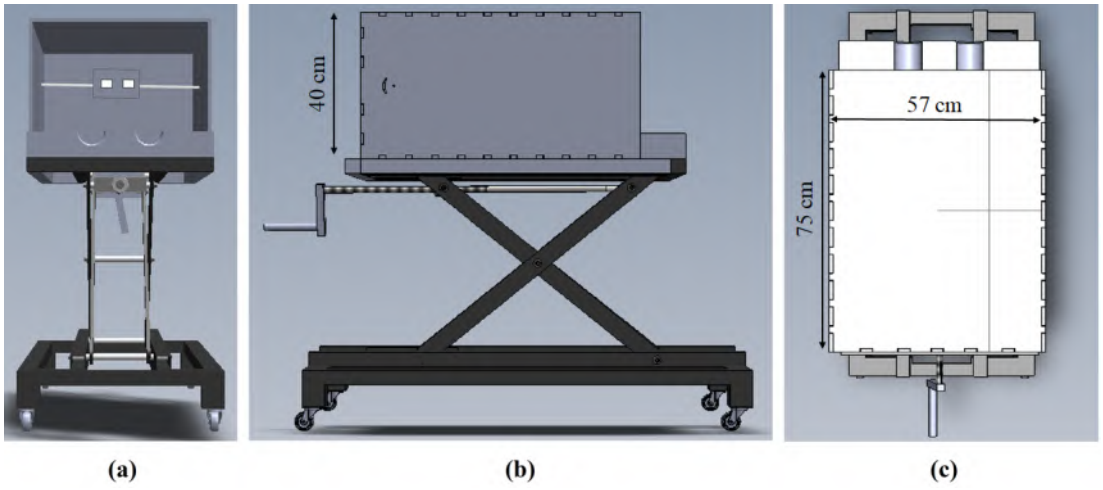


Figure 6.4: The **(a)** Frontal view **(b)** Section view and **(c)** Top view of the designed feet scanning unit in Solidworks® 2018 SP4

6.3.3 The Camera Mount

A separate camera mount was also designed using Solidworks®, and realized in polycarbonate sheets by laser cutting. The laser cut parts were later assembled into a unit as shown in the Figure 6.5. The colour image camera was mounted 2.7 cm behind the Lepton 3B+ camera as shown in Figure 6.5 to compensate for its smaller field of view. Purethermal 2 breakout board mounted with the Lepton 3B+ was interfaced to the Raspberry pi 3B+ SBC via USB 2.0. A flex cable was used to interface the Raspberry pi camera module v2 to the Raspberry pi 3B+ SBC. The Raspberry pi 3B+ SBC was also placed inside the camera mount to reduce the distance between the imaging sensors and the data acquisition and processing unit.

The microbolometer imaging sensor in the Lepton 3B+, measures the intensity of the infrared radiation emitted by a given object placed in front of it. However, presence of surrounding objects which emits infrared radiation distorts the image and segmentation of the image becomes overly complicated. That is the reason why the thermal measurements are taken inside an enclosed space. Inside of the feet scanning unit was painted black to minimize the reflection of infrared radiation from the object

through the stainless steel surface.

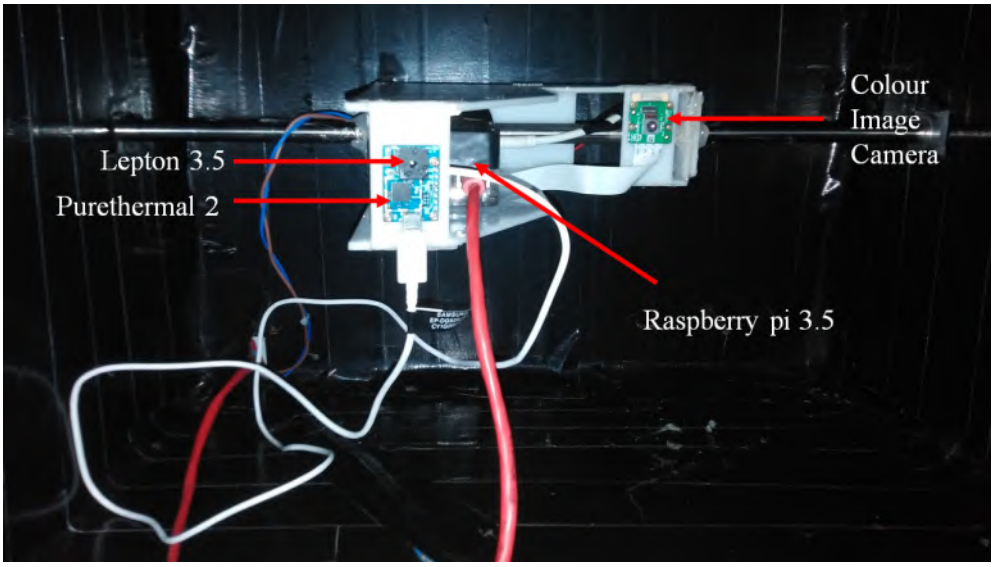


Figure 6.5: The camera mount designed to house the two imaging sensors (thermal and colour) and fix the Raspberry pi 3B+ SBC

The Lepton 3B+ thermal imaging sensor has been black body calibrated under special laboratory conditions, hence, it requires no further calibration before use [188]. Thus, two black bodies with known temperatures have been measured using the Lepton 3B+ under various laboratory and conditions using a proprietary software that communicate over I_2C [188]. Accordingly, the manufacture declares that the calibration highly accurate and re-calibration is not required. However, a calibration process using two black bodies is outlined in the FLIR Radiometery quickstart guide [188] if the user wishes to perform re-calibration. Despite the reassurance by the manufacturer, it is impossible to guarantee optimum performance of the thermal sensor without manual calibration to see whether the temperature measured by the sensor is the same as the actual temperature of the object. However, no secondary calibrations were conducted for the Lepton 3B+ camera in the present study.

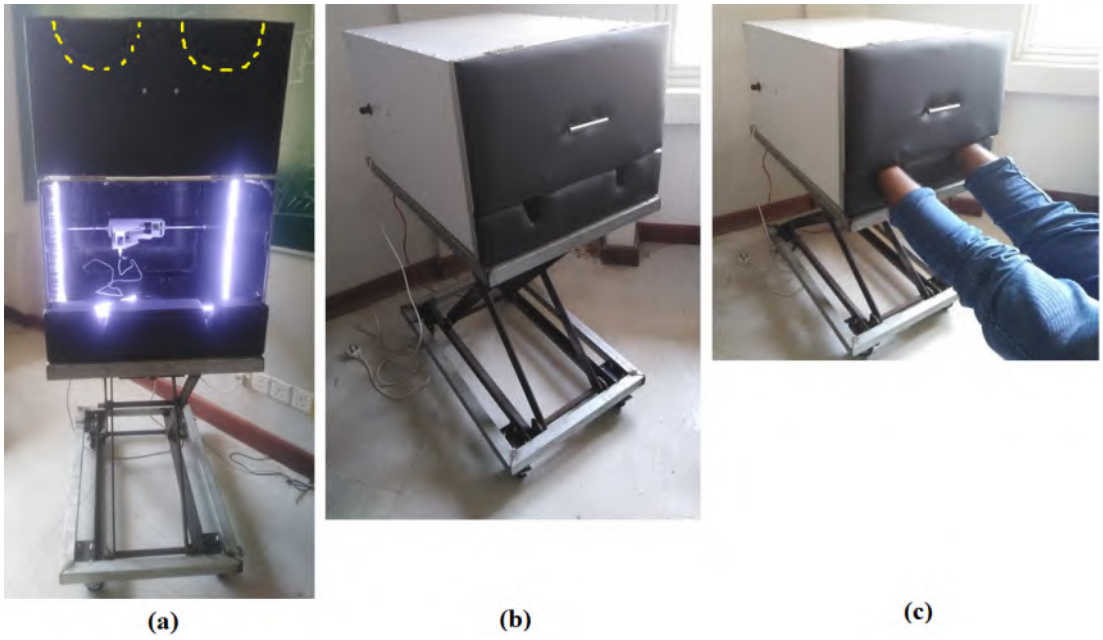


Figure 6.6: The physically realized pedothermographic assessement tool. **(a)** Inside of the the pedothermographic assessement tool demonstrating the LED light strip and the Camera mount inside the feet scanning unit. The yellow coloured arcs represents two structures made entirely of cushion that get tightly fixed around the perimeter of the patient legs. **(b)** Front view of the final pedothermographic assessement tool with enclosing door to prevent light entering the assessement tool from the open front end. **(c)** How the patient feet rests on the feet resting unit when the enclosing door has been closed and the device is ready for image acquisition

The colour image camera can not capture an image of the patient foot plantar without reflected light. Hence, a strip of LEDs were mounted inside the feet scanning unit as shown in the Figure 6.6 (a), which could be turned ON when the colour image is captured and then turned OFF for the thermal image acquisition.

6.3.4 The Scissor System

One of the major limitations of the systems implemented by Madarasinghe et al. [187] and Van Netten et al. [36, 151] was the inability to vertically move the feet scanning unit to the same level as the patient feet. A strong and a wide base to rest the feet

scanning unit was designed and a scissor system was designed to facilitate the vertical movement of the system as shown in Figure 6.7. The scissor system consist of a handle which can be rotated in clockwise or anti-clockwise directions. The handle is internally connected to an axel (Figure 6.4 (b)) which undergoes horizontal linear motion towards or away from the device causing the x-shaped scissor structures to undergo vertical linear motion either upwards or downwards. The structures were made of steel and and were able to withstand the high torque generated when a patient rest their feet on the feet resting unit without any tilting or instability.

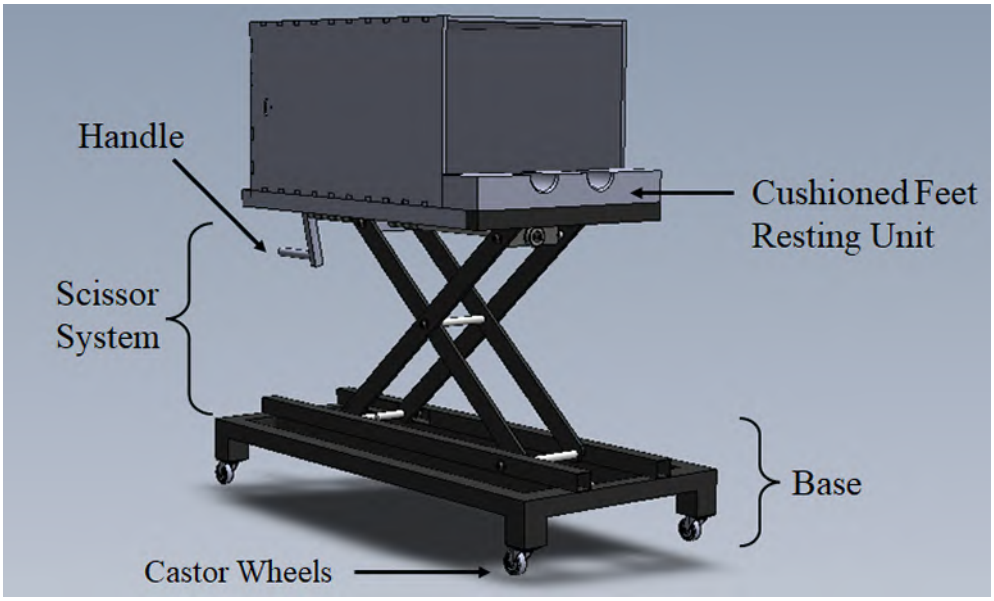


Figure 6.7: The base and the scissor system of the pedothermographic assessment tool

6.4 Data Acquisition and Thermogram Visualization

Acquisition and processing of high resolution image data from two imaging sensors in real-time could not be delivered by a microcontroller based embedded system due to the limitations in internal memory and CPU resources [189]. Therefore, single board computers such as Raspberry pi 3B+ (Figure 6.3) which was the latest model at the time, was selected for such implementations where Linux based standalone operating systems could also be installed.

Linux Raspbian operating system was flashed onto a 32 GB microSD card. First the Raspberry pi camera module v2 was connected to the custom camera port on the Raspberry pi device via the flex cable and the camera module was enabled from the Raspberry pi configuration settings. The camera was initially tested using the command line using "raspistill" and "raspivid" default commands. After successful integration, a python code was written using openCV to obtain a live stream from the camera module v2 and capture still images when necessary.

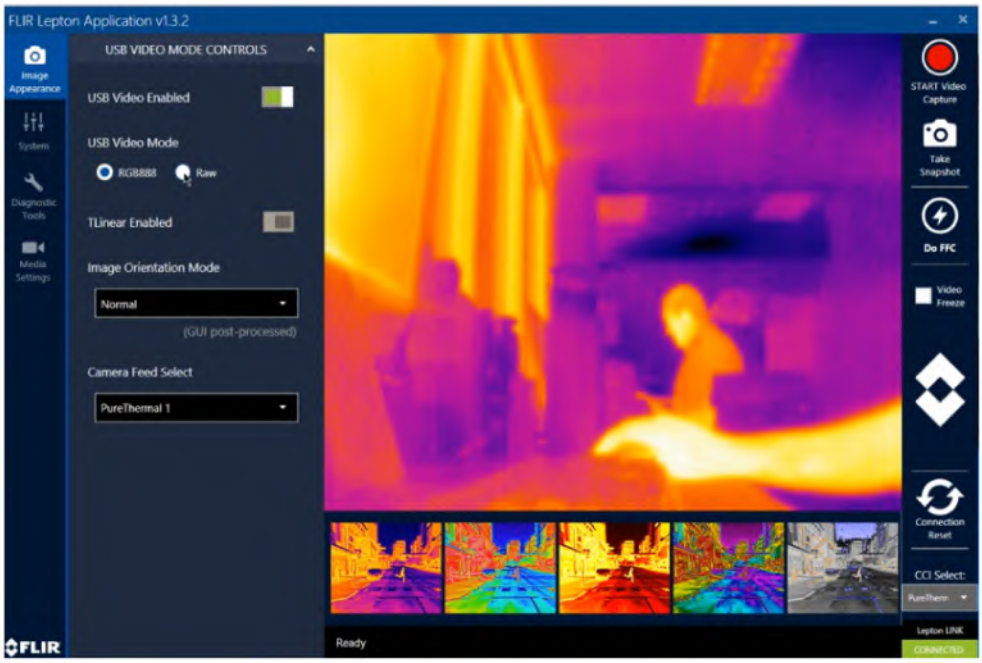


Figure 6.8: Initial testing of the Lepton 3.5 and Purethermal assembly using a Windows 10 computer using the Lepton User App software

A default software to interface the Lepton 3.5 and a computer running Windows 7 or above was available from the manufacturer as shown in Figure 6.8. It was used to verify the functionality of the thermal camera and purethermal 2 prototype board which was connected via a micro-USB cable to the Raspberry pi.

However, there existed no such application to visualize the thermal images in real-time in Raspberry Pi. Therefore, using the open-source purethermal-uvc-capture library in GitHub [190], and QT GUI framework a custom application was developed

for Raspbian (Linux OS) as shown in Figure 6.9. The image viewer could deliver a thermogram and a point temperatures of the feet indicated by the position of the cursor (+). The application can provide temperatures in both Celsius or Fahrenheit as desired.

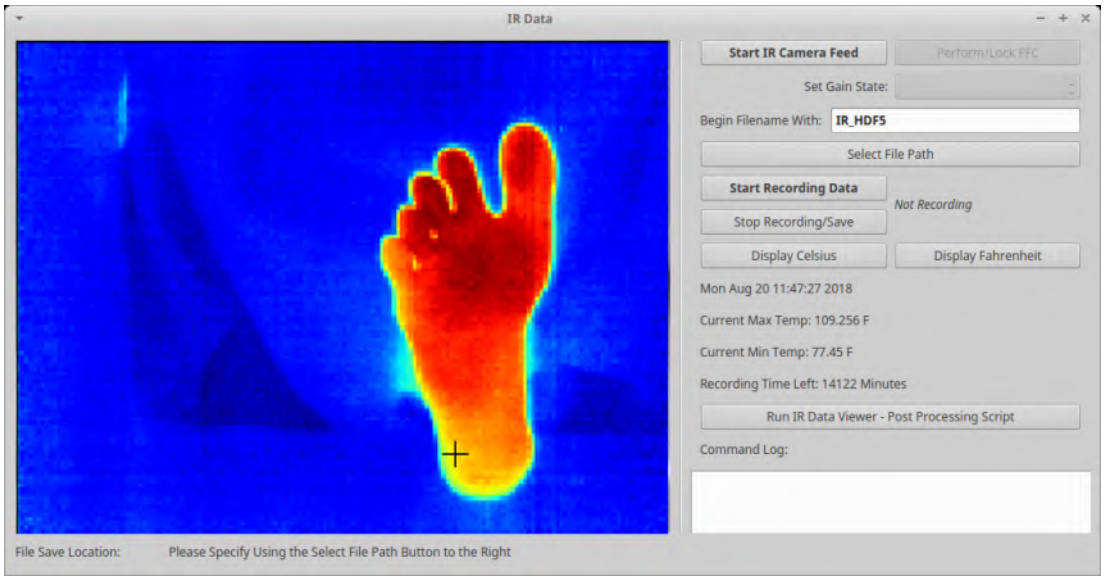


Figure 6.9: The thermal image acquisition tool developed using purethermal uvc capture library and QT GUI framework

A web application was developed in html so that thermograms could be remotely shared among physicians to improve and assist diagnosis. The developed tool shown in Figure 6.10 can compare two thermograms at a given instance. By clicking on the "Browse" button, a thermogram can be loaded to either side of the application and by clicking on the "Load Selected File" button, each thermogram can be uploaded to be viewed.

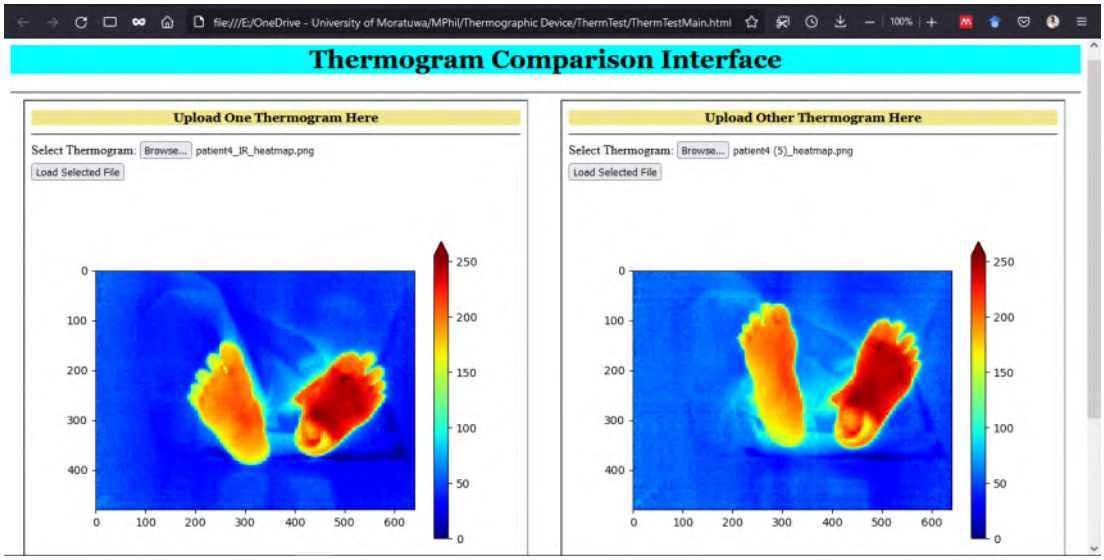


Figure 6.10: The web application developed using html to compare two thermograms obtained

For the visualization of thermograms generated by the Raspberry Pi SBC using the applications shown in Figure 6.9 and 6.10, a display device such as a HDMI monitor is required. However, it may sometimes be easier to use the Raspberry pi SBC without a monitor rather than a laptop computer during routine clinical assessments. It allows the operator to conduct the assessment at a convenient location via WIFI. It was implemented by installing VNC viewer and PuTTY applications in the laptop. PuTTY is a windows application that allows secure communication between two computers through encryption using SSH (Secure Socket Shell) protocol [191]. SSH incorporates a client/server architecture so that the raspberry pi SBC assumes the role of the client while the PuTTY installed laptop functions as the server.

After switching ON, the raspberry pi SBC is automatically connected to a WIFI router. Then, PuTTY could be launched from the laptop and the IP address and the port number of the Raspberry pi should be entered as shown in Figure 6.11. Then, the raspberry pi will be connected to the laptop computer. In order to log in to the raspberry pi, the username and the password of the raspberry pi SBC has to be entered. However, PuTTY establishes connection between the raspberry pi and the

laptop via the command line interface. VNC Viewer which can be launched in the laptop could then show the output display of the Raspberry pi, so that the GUI application that could easily be launched from it. Therefore, the raspberry pi can essentially be controlled from the laptop (similar to a virtual machine) without the need for extra hardware peripherals such as a mouse, keyboard and a display monitor as shown in Figure 6.12.

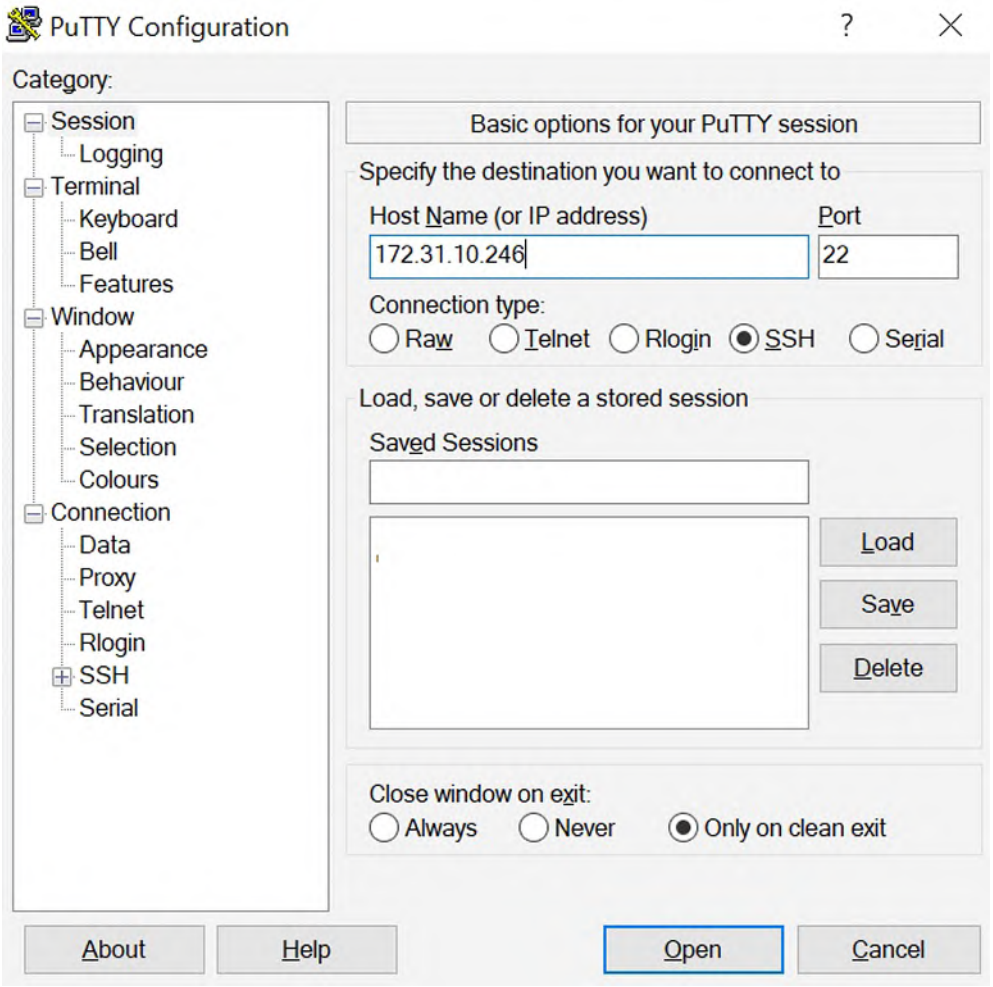


Figure 6.11: PuTTY application used to connect the raspberry pi to a laptop via SSH

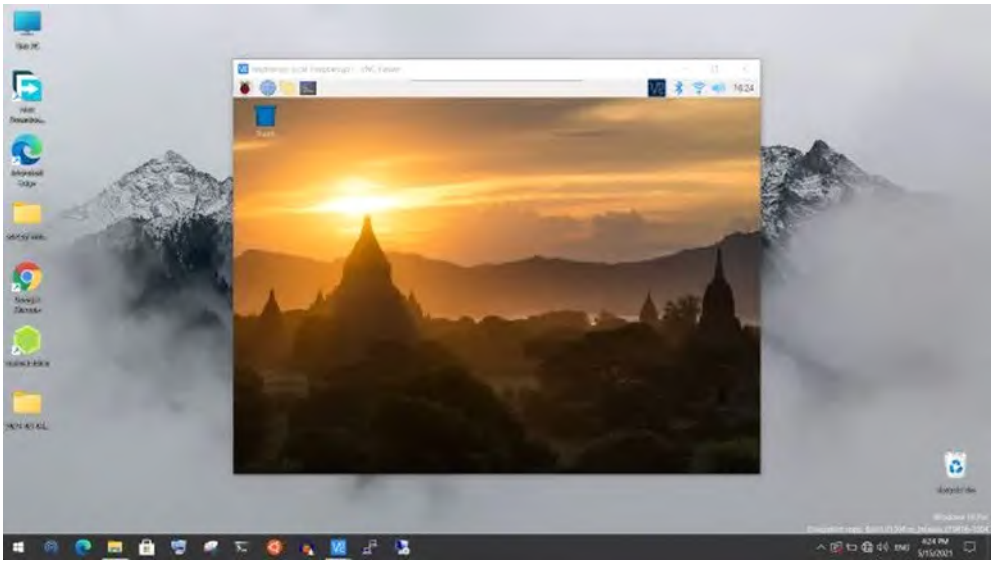


Figure 6.12: VNC Viewer application which launches Raspberry Pi SBC output display

6.5 Thermogram Generation

The purethermal breakout board which is connected to the USB port of the Raspberry pi SBC, is turned ON as soon as the raspberry pi is powered ON. However, to acquire thermal images, the python software has to be launched. The intensity of infrared photons that strike the microbolometer sensor array of 160×120 pixel array of Lepton 3.5 are converted to a 16-bit ADC value and stored temporarily in a look up table as shown in Figure 6.13.

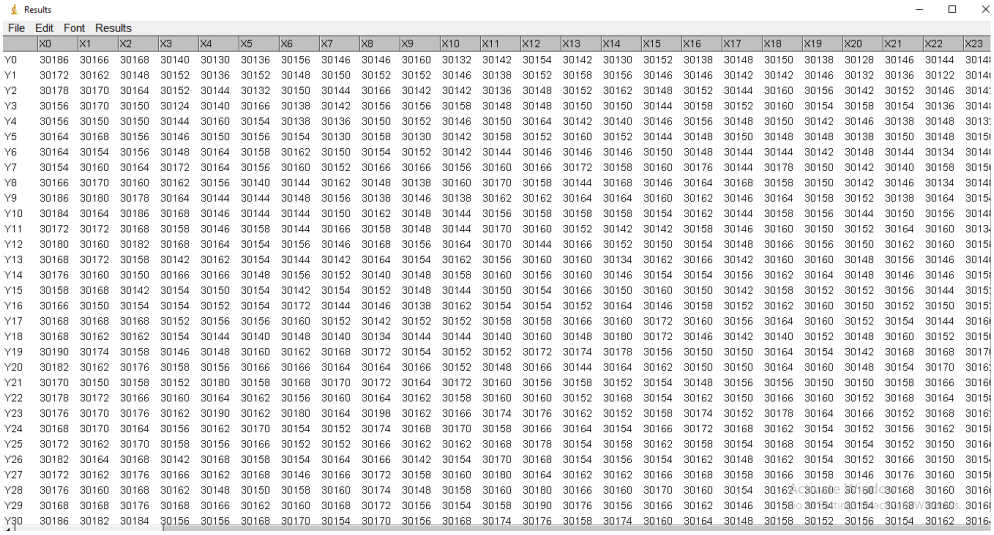
Each pixel value represents the temperature value measured in centiKelvin (T_{cK}). The Equation 5 is used in order to convert the pixel values to temperature in Celsius.

$$Temperature(°C) = \frac{T_{cK}}{100} - 273.15 \tag{5}$$

For example, the temperature (°C) of X1,Y1 pixel (pixel value = 30162) of Figure 6.13

can be calculated as shown below.

$$Temperature(°C) = \frac{30162}{100} - 273.15$$
$$= 28.47\ °C$$



	X0	X1	X2	X3	X4	X5	X6	X7	X8	X9	X10	X11	X12	X13	X14	X15	X16	X17	X18	X19	X20	X21	X22	X23
Y0	30186	30166	30168	30140	30130	30136	30156	30146	30146	30160	30132	30142	30154	30142	30130	30152	30138	30148	30150	30138	30128	30146	30144	30140
Y1	30172	30162	30148	30152	30136	30152	30148	30150	30152	30152	30146	30138	30152	30158	30156	30146	30146	30142	30142	30146	30132	30136	30122	30140
Y2	30178	30170	30164	30152	30144	30132	30150	30144	30166	30142	30142	30136	30148	30152	30162	30148	30152	30144	30160	30156	30142	30152	30146	30142
Y3	30156	30170	30150	30124	30140	30166	30138	30142	30156	30156	30158	30148	30148	30150	30150	30144	30158	30152	30160	30154	30158	30154	30136	30148
Y4	30156	30150	30150	30144	30160	30154	30138	30136	30150	30152	30146	30150	30164	30142	30140	30146	30156	30148	30150	30142	30146	30138	30148	30132
Y5	30164	30168	30156	30146	30150	30156	30154	30130	30158	30130	30142	30158	30152	30160	30152	30144	30148	30150	30148	30148	30138	30150	30148	30150
Y6	30164	30154	30156	30148	30164	30158	30162	30150	30154	30152	30142	30144	30146	30146	30146	30150	30148	30144	30144	30142	30148	30144	30134	30140
Y7	30154	30160	30164	30172	30164	30156	30160	30152	30166	30166	30156	30160	30166	30172	30158	30160	30176	30144	30178	30150	30142	30140	30158	30150
Y8	30166	30170	30160	30162	30156	30140	30144	30162	30148	30138	30160	30170	30158	30144	30168	30146	30164	30168	30158	30150	30142	30146	30134	30148
Y9	30186	30180	30178	30164	30144	30144	30148	30156	30138	30146	30138	30162	30162	30164	30164	30160	30162	30146	30164	30158	30152	30138	30164	30154
Y10	30184	30164	30186	30168	30146	30144	30144	30150	30162	30148	30144	30156	30158	30158	30158	30154	30162	30144	30158	30156	30144	30150	30156	30148
Y11	30172	30172	30168	30158	30146	30158	30144	30166	30158	30148	30144	30170	30160	30152	30142	30142	30158	30146	30160	30150	30152	30164	30160	30134
Y12	30180	30160	30182	30168	30164	30154	30156	30146	30168	30156	30164	30170	30144	30166	30152	30150	30154	30148	30166	30156	30150	30162	30160	30150
Y13	30168	30172	30158	30142	30162	30154	30144	30142	30164	30154	30162	30156	30160	30160	30134	30162	30166	30142	30160	30160	30148	30156	30146	30140
Y14	30176	30160	30150	30166	30166	30148	30156	30152	30140	30148	30158	30160	30156	30160	30146	30154	30154	30156	30162	30164	30148	30146	30146	30150
Y15	30158	30168	30142	30154	30150	30154	30142	30154	30152	30148	30144	30150	30154	30166	30150	30160	30150	30142	30158	30152	30152	30156	30144	30152
Y16	30166	30150	30154	30154	30152	30154	30172	30144	30146	30138	30162	30154	30154	30152	30164	30146	30158	30152	30162	30160	30150	30152	30150	30152
Y17	30168	30168	30168	30152	30156	30156	30160	30152	30142	30152	30152	30158	30158	30166	30160	30172	30160	30156	30164	30160	30152	30154	30144	30160
Y18	30168	30162	30162	30154	30144	30140	30148	30140	30134	30144	30144	30140	30160	30148	30180	30172	30146	30142	30140	30152	30148	30160	30152	30150
Y19	30190	30174	30158	30146	30148	30160	30162	30168	30172	30154	30152	30152	30172	30174	30178	30156	30150	30150	30164	30154	30142	30168	30168	30170
Y20	30182	30162	30176	30158	30156	30166	30166	30164	30164	30166	30152	30148	30166	30144	30164	30162	30150	30150	30164	30160	30148	30154	30170	30162
Y21	30170	30150	30158	30152	30180	30158	30168	30170	30172	30164	30172	30160	30156	30158	30152	30154	30148	30156	30156	30150	30150	30158	30166	30160
Y22	30178	30172	30166	30160	30164	30162	30156	30160	30164	30162	30158	30160	30160	30152	30168	30154	30162	30150	30166	30160	30152	30168	30164	30150
Y23	30176	30170	30176	30162	30190	30162	30180	30164	30198	30162	30166	30174	30176	30162	30152	30158	30174	30152	30178	30164	30166	30152	30168	30162
Y24	30168	30170	30164	30156	30162	30170	30154	30152	30174	30168	30170	30158	30166	30164	30154	30166	30172	30168	30162	30154	30152	30156	30162	30150
Y25	30172	30162	30170	30158	30156	30166	30152	30152	30166	30162	30162	30168	30178	30154	30158	30162	30158	30154	30168	30154	30154	30152	30150	30160
Y26	30182	30164	30168	30142	30168	30158	30154	30164	30166	30142	30154	30170	30168	30154	30156	30154	30162	30148	30162	30154	30152	30166	30150	30154
Y27	30172	30162	30176	30166	30162	30168	30146	30166	30172	30158	30160	30180	30164	30162	30162	30166	30168	30158	30166	30158	30146	30176	30160	30150
Y28	30176	30160	30168	30162	30148	30150	30158	30160	30174	30148	30158	30160	30180	30166	30160	30170	30160	30154	30162	30160	30160	30168	30160	30160
Y29	30168	30168	30176	30168	30166	30162	30160	30168	30172	30156	30154	30158	30190	30176	30156	30166	30162	30146	30158	30154	30154	30168	30160	30160
Y30	30186	30182	30184	30156	30156	30168	30170	30154	30170	30156	30168	30174	30176	30158	30174	30160	30164	30148	30158	30152	30156	30154	30162	30160

Figure 6.13: Part of the temperature values recorded in each pixel of the 160×120 microbolometer sensor array

Therefore, using the Equation 5, all the pixel values could be converted to temperature values in Celsius to generate a raw image with temperature values. However, visualizing the generated raw image is challenging with the naked eye. This is because, the captured scene has a limited range of temperature values which do not generate sufficient contrast to visualize it as an image (Figure 6.14 (a)).

As a result, these raw images had to be normalized within the smallest and greatest temperature value in the raw image using Automatic Gain Control (AGC) algorithms which generate an image with sufficient contrast to be visualized with the naked eye (Figure 6.14 (b)). Afterwards, a suitable colourmap could be applied to the raw image such that the lowest temperature in the image is assigned the lowest intensity value of the colour pallet and highest temperature value within the image is assigned the highest intensity value of the colourmap (or vise versa) to generate a thermogram.

The diverging colourmap "coolwarm" was used here which is a builtin colourmap in Matplotlib library in python which extends from blue to red which is the customary range of colours in a thermogram. [36, 151]. As implied by the name, cool surfaces are assigned blue colours while warm surfaces are mapped with red colour. The intensity of temperature determines the colour intensity of blue and red.

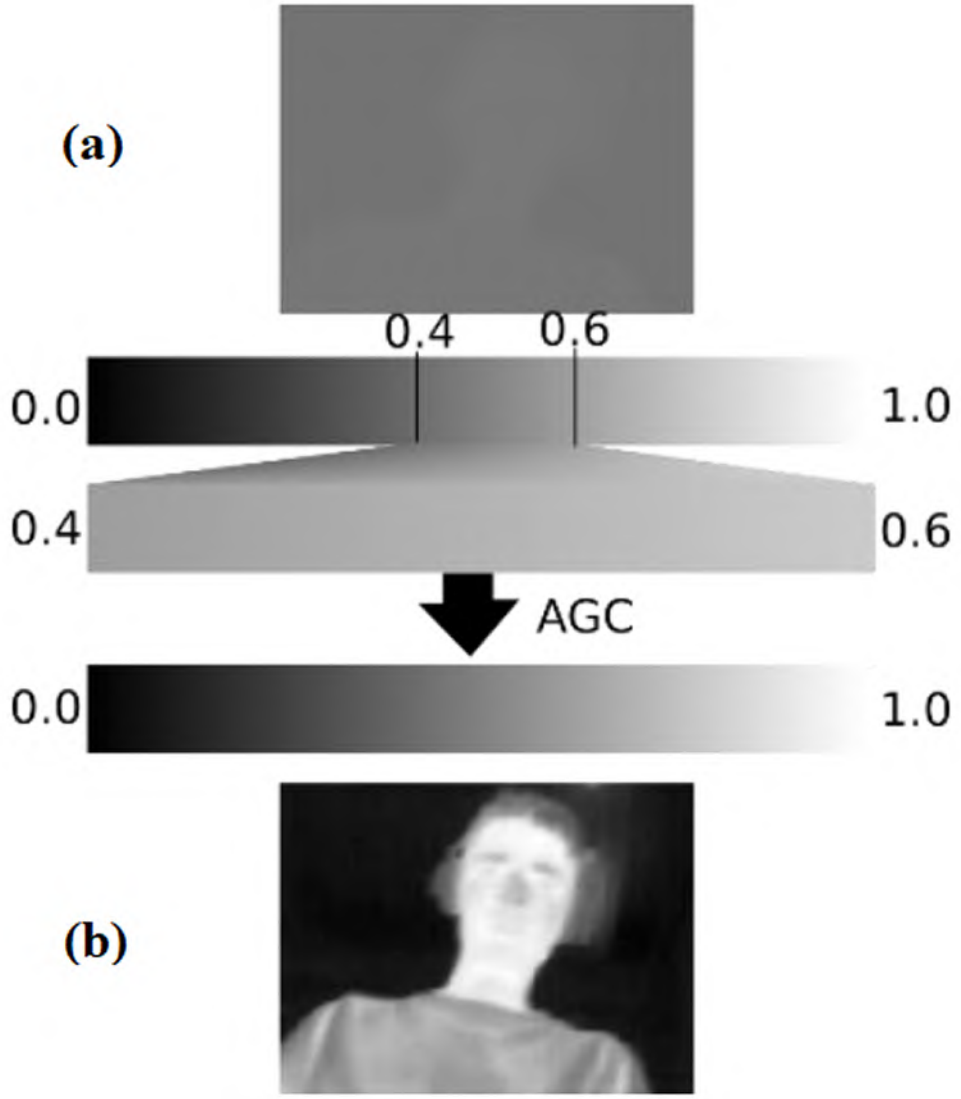


Figure 6.14: Process of normalizing the obtained raw temperature image using AGC algorithms. **(a)** The raw temperature image. **(b)** The normalized image using AGC algorithms

CHAPTER 7

Conclusion

7.1 Overview

This chapter presents the conclusions derived from this dissertation. It portrays how the research findings correlate with the aims and objectives of the research and the primary research problem, limitations identified from the study and the recommendations for conducting future research.

7.2 Objectives and Research Outcomes

Plantar pressure measurement (pedobarography) platform systems which have an edge over in-sole measurements systems due to high spatial resolution and increased sensing area, inherently suffer from crosstalk interference among sensels as a result of the shared-row column architecture. However, one of the main limitations in plantar pressure assessment with commercial platform systems is the mitigation of crosstalk through proprietary algorithms at software level which have proven to emphasise either measurement accuracy or shape accuracy, but not both simultaneously. However, simultaneous measurement accuracy and shape accuracy are the major determinants of effective crosstalk suppression. Therefore, in the present study we mainly investigated the possibility of implementing a large pedobarographic system

with effective crosstalk suppression utilizing a zero potential hardware compensation technique on a custom built piezoresistive sensor array with newly developed readout mechanism.

The initial thought process was to build the pedobarographic system around a FPGA centered system architecture to provide hardware acceleration due to the increased number of sensels (30,000) present in the piezoresistive sensor array. Therefore, upon a thorough investigation we implemented the the system with an APSoC device which encompasses both a FPGA and a dual core processor in the same fabric.

Inspired by the type-III scanning architecture proposed by Kim et al. [116], we implemented an improved novel decoder-transistor scanning architecture that is well-suited for implementing a large sensor array scanning mechanism employing the S-NSSE-ZP technique for effective crosstalk suppression. The realized readout circuit which has a shared 50 row-driving electrodes and separate set of column sampling electrodes for two clusters (60 each) in a single PCB, delivered a measurement accuracy which was quantified to be $< 1\%$ and a significant shape accuracy which could be evaluated qualitatively. The attained measurement accuracy was par with those attained through other scanning mechanisms that are listed in literature to be fairly accurate.

A separate data acquisition architecture was implemented in the APSoC using Xilinx Vivado and SDK, using existing and custom developed set of IPs, which surpassed all the timing, power consumption, synchronization and delay tests at the software level for a cluster as well as the entire system consisting of ten clusters. Using a hybrid validation technique using both simulation results and readings from a test model we also validated the proper functionality of the implemented system which were published in the IEEE Sensors Q1 journal [127]. Thereby, the main objectives of our study to realize a high accuracy piezoresistive scanning mechanism for a large sensor array using a FPGA centered architecture was successfully realized.

The APSoC was able to transmit data at a rate of 30 Mbps through a USB 2.0

interface. The implemented GUI using Python offered a platform to visualize the pedobarograms in a computer with any operating system due to the cross-platform portability in Python.

A secondary objective of the study was to conduct validation of the developed implemented system. Due to the pandemic situation at the time of this research study and the termination of the research grant, we were not able to realize all ten clusters of the pedobarographic system due to financial and resource constraints. However, we completely implemented one cluster through a readout circuit and demonstrated that the implemented readout circuit and the scanning architecture deliver significantly high crosstalk suppression by validating it through measurement accuracy and shape accuracy. Given that APSoC allows parallel processing, data acquisition and processing was done in parallel from all ten clusters simultaneously. Thus, validation of one cluster at hardware level essentially ensures proper functionality of the rest of the readout circuits. Moreover, a separate validation was carried out as a series of simulation studies for an individual cluster as well as all ten clusters which demonstrated that the design meets all the criteria to deliver optimum performance.

Although, not listed as an objective, we took the liberty of implementing a pedothermographic system as an extension to the work undertaken by Mararasinghe et al. [187]. The improved implementation could scan both feet of a patient at an enclosed space using a NIR thermal camera and a colour image camera in a Raspberry pi SBC based system that could generate an output in a separate HDMI display monitor or through a laptop screen connected over WIFI via SSH through PuTTY and VNC Viewer. A custom application was developed in Linux to visualize the thermograms in real-time and/or capture still images, measure and record point and regional temperature variations. In addition, an html based cross-platform interface was developed to visualize and analyze several thermograms remotely. However, analysis of thermograms and the calibration of the thermographic system was beyond the scope of the present study.

7.3 Present Limitations and Future Recommendations

7.3.1 Pedobarographic Assessment Tool

The main limitation of the present study can be identified as the non-implementation of the pedobarographic system in full due to several restrictions beyond the control of the author. However, the full implementation is just a repetition of the same process implemented on one cluster using one readout circuit, on ten different clusters that are operating in parallel. This implementation is bound to deliver the same results in terms of effective crosstalk suppression and operational speed. Although, a through analysis could have been conducted for the whole piezoresistive sensor array in terms of the spatial resolution delivered by the sensing platform. A detailed analysis of the synchronization of data generated from different clusters to form a single image of 300×150 pixels could also have been studied. Therefore, a complete implementation of the pedobarographic system in as a future development would enable a complete hardware analysis of the pedobarographic system.

In addition, the readout circuit was implemented with S-NSSE-ZP technique. Although, practical implementation and comparisons were made under similar conditions for the basic types of voltage feedback and zero potential methods, VF-NSE method and S-NSE-ZP method, no comparisons were made when selecting the appropriate type of zero potential technique among the three existing methods (S-NSE-ZP, S-NSSE-ZP and S-NSDE-ZP methods). The selection was done primarily on the available literature and considering the cost of implementation. Therefore, a similar comparison among the three types of zero potential techniques could effectively deduce the most reliable crosstalk suppression mechanism under similar conditions.

Another limitation was the comparatively low speeds of data transmission between the APSoC and the computer which was expected when the implementation was done

using the USB 2.0 interface. This is justifiable as our main focus was on improving the accuracy of the acquired data rather than the speed of transmission. Given that the current Xilinx Zynq APSoC does not incorporate a USB 3.0 interfaces or higher (speeds over 10 Gbps [185]), updating the implementation to transmit data via Ethernet would be the most plausible solution. Utilizing the standard lightweight IP (LWIP)-Raw and lightweight IP (LWIP)-Socket, data transmission can be implemented with speeds over 13.5 Gbps. When the full implementation is complete in a future study, data transmission must be upgraded to Ethernet protocol to accommodate for large volume of data transmission.

Moreover, the present implementation of the pedobarographic system is centered around an APSoC which has an abundance of unutilized hardware resources even when ten clusters are realized in it. If the present pedobarogrphic system is to be manufactured in large scale as a commercial product, a more formidable custom made APSoC without excess hardware resources could be fabricated.

7.3.2 Pedothermographic Assessment Tool

The thermal imaging sensor was not calibrated in the present study as the only focus was on implementation of the pedothermographic assessment tool. Despite the fact that Lepton 3.5 was black body calibrated under factory conditions, calibration of the thermal sensor by mapping the measured temperature with the actual temperature of an object could prove vital for thermogram assessment and subsequent diagnosis. Therefore, it is recommended to calibration of the Lepton 3.5 is recommended for future studies.

Using SSH/PuTTY and VNC Viewer implementation to use a laptop screen as the display device of the thermographic system has a limitation. That is, when logging into the Raspberry pi the IP address has to be entered. However, connections via WiFi often allocates dynamic IPs to different peripherals connected to it. Therefore, router configuration tool has to be accessed from the browser to identify the IP of the

Raspberry Pi every time a connection has to made. This would be a noticeable limitation in that implementation. However, an institution like a hospital where the implemented pedothermographic assessment tool would be used generally has dedicated bandwidth in the WiFi. Hence, devices are generally assigned with static IPs. In such cases, the burden of dynamically varying IPs would not arise.

7.3.3 Final Comments

When both pedobarographic system and pedothermographic assessment tools are implemented in full and validated, evaluation has to be carried out on live subjects to test the efficacy of the system under actual conditions where it would be used. Therefore, a clinical observational study must be conducted on patients using both assessment tools in tandem, such that both a thermogram and a pedobarogram has to be obtained from both foot plantars of the same patient.

In conclusion, when realized in full, both these assessment tools together could play a vital role in early detection of foot related complications in diabetic patients, by detecting DPN and PAD complications early, so that proper clinical intervention could be deployed before they progress to ulceration and subsequent amputation. In addition, these deveices could also play a significant role in a multitude of biomechanical studies related to the foot plantar and analysis of gait.

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APPENDIX A

ZPM and VFM Readout Test Circuit Schematic

Schematic diagrams can be drawn with either physical connectivity or logical connectivity between components [192]. Physical connectivity involves the use of physical nets connected between corresponding pins of the components. Logical connectivity involves net labels placed on pins of components that display no physical nets between component pins. ZPM readout test circuit was drawn using logical connections between components as shown in Figure A.1 while VFM readout test circuit was drawn using physical connections between components as shown in Figure A.2.

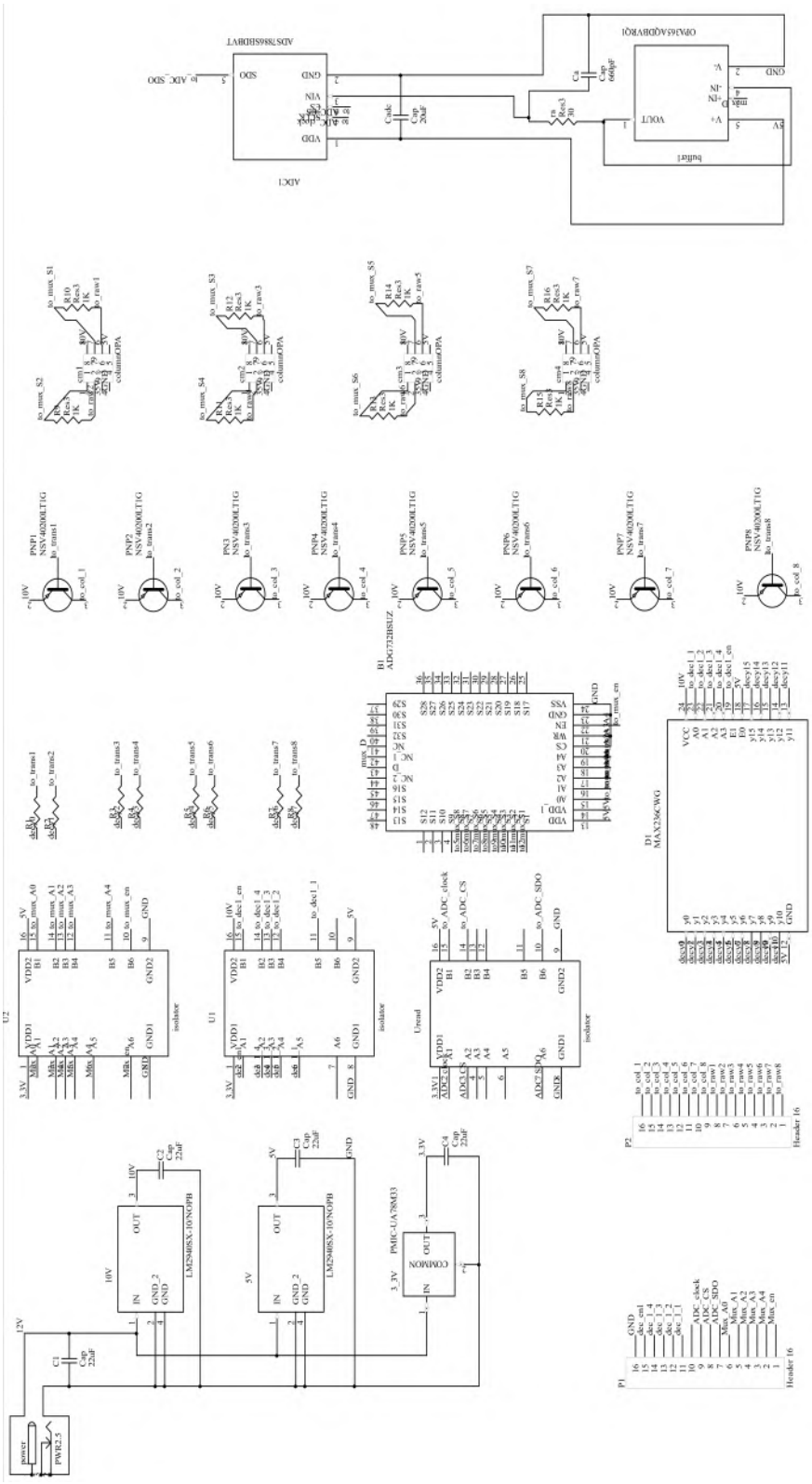

Figure A.1: ZPM Readout Test Circuit Schematic

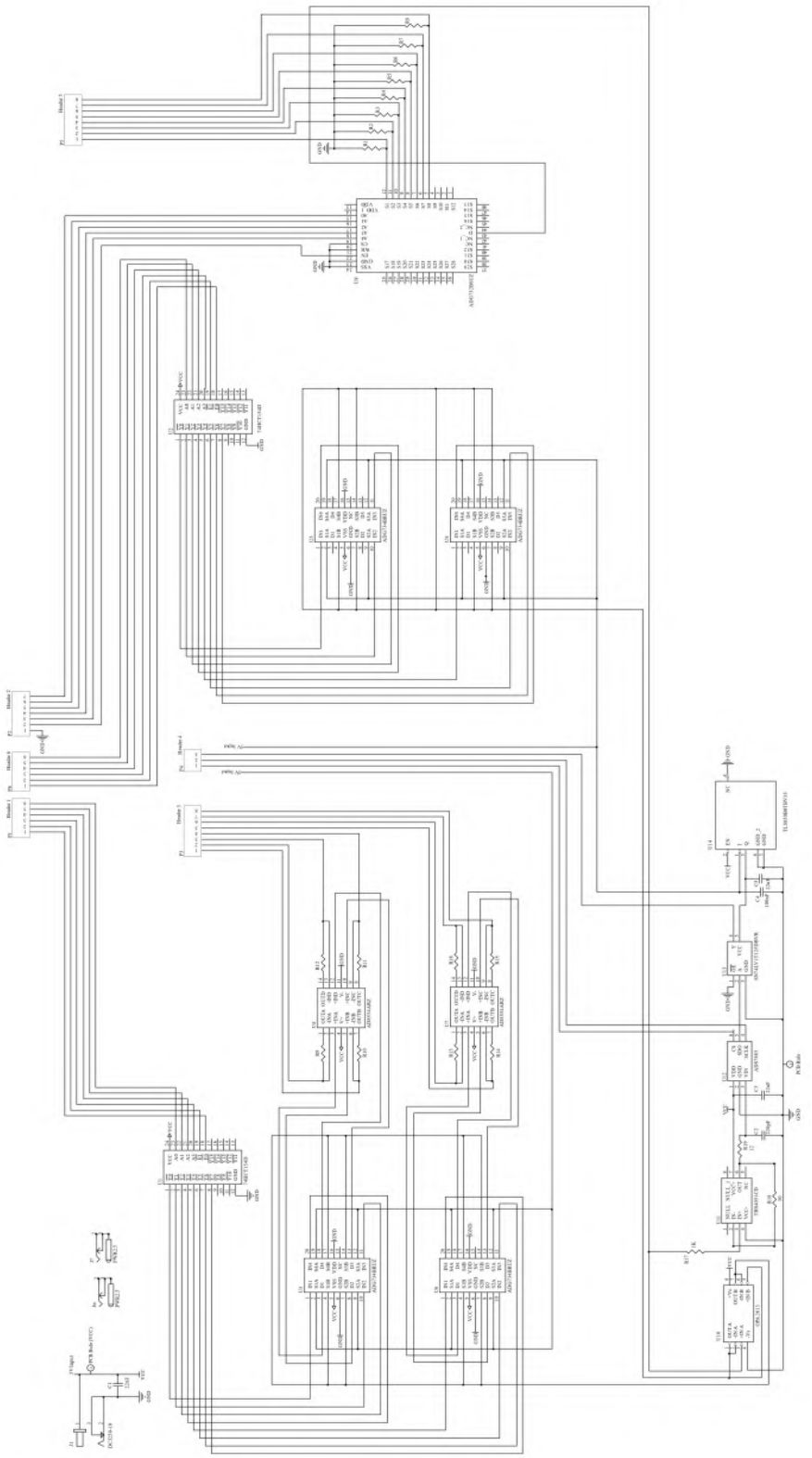

Figure A.2: VFM Readout Test Circuit Schematic

APPENDIX B

Python Program to Serially Acquire Data from APSoC

```
# ------------------------------------------------- #
# Program to Read Piezoresistive Sensor Array/RSA using
Xilinx Zynq Zybo
# Author : A.S. Warnakulasuriya
# ------------------------------------------------- #
import matplotlib.animation as animation
import matplotlib.pyplot as plt
import numpy as np
import seaborn as sns
import serial
import time
# ------------------------------------
# Variables of the Pressure Sensor Array
# ------------------------------------
NR = 8        # No. of rows
NC = 8        # No. of columns
v1 = 0        # ADC Lowest
v2 = 5000     # ADC Highest
COM = "COM4"
baudR = 115200
numPoints_ini = ((NR*NC)+2)
numPoints = (NR*NC)
dataList_ini = [0]*numPoints_ini
dataList = [0]*numPoints
count = 0

rows = ["R{}".format(i) for i in range(1, NR+1)]
columns = ["C{}".format(i) for i in range(1, NC+1)]
```

```
# ------------------------------------
# Initiate Serial Communication
# ------------------------------------
ser = serial.Serial(COM, baudrate=baudR)
# ser.set_buffer_size(rx_size = 12800, tx_size = 12800)
# time.sleep(1)
# fixed time delay before the user can request

print("FPGA Connected")
time.sleep(0.1)
print("Connected to: " + ser.portstr)
time.sleep(0.1)
print("Initializing Data Acquisition...\n")

def getValues():
    ''' #Requesting, Reading and Returning serial data
    from the zynq '''

    # ser.write(b'K')
    # b signifies that we are writing a byte to the serial bus
    zynqData = ser.readline().decode().split('\r\n')
    # readline() reads until end of line character \n
    return zynqData[0]

def hmap(data):
    """ Generate heatmap from seaborn library"""

    ax = sns.heatmap(data, vmin=v1, vmax=v2, cmap="plasma_r",
    xticklabels=columns, yticklabels=rows, linewidths=0)
    ax.tick_params(top=True, bottom=False, labeltop=True,
    labelbottom=False)

    return ax

def matRead():

    global count
    startTime = time.time()
    if count == 0:
        for j in range(0, numPoints_ini):
            dataList_ini[j] = int(getValues())
        oneCluster = np.array(dataList_ini[2:]).reshape(NR, NC)
        count += 1
    else:
```

```
        for j in range(0, numPoints):
            dataList[j] = int(getValues())
        oneCluster = np.array(dataList).reshape(NR, NC)
    print(oneCluster)
    print("\n Execution time = %.3f seconds\n"
    % float((time.time() - startTime)))

    return oneCluster

def animate_heat_map():

    fig = plt.figure(figsize=(8, 6))
    fig.canvas.set_window_title('GUI Interface')
    fig.tight_layout()

    # data = np.zeros((nx, ny))
    data = np.full((NR, NC), 4095, dtype=int)
    # ax = sns.heatmap(data, vmin=v1, vmax=v2)
    ax = hmap(data)

    def init():
        plt.clf()
        # ax = sns.heatmap(data, vmin=v1, vmax=v2)
        ax = hmap(data)

    def animate(i):
        plt.clf()

        data = matRead()
        # ax = sns.heatmap(data, vmin=v1, vmax=v2)
        ax = hmap(data)

    anim = animation.FuncAnimation(fig, animate,
    init_func=init, interval=5000)

    plt.show()
    # plt.pause(10)

if __name__ == "__main__":
    animate_heat_map()
```

APPENDIX C

Publication made in the Q1 Journal IEEE Sensors

The results readout circuit validation conducted as an analysis of shape accuracy and measurement accuracy, was presented in a Q1 journal publication made in the IEEE Sensors journal. Details of the publication are listed below.

Journal	: IEEE Sensors Journal
Publication Date	: AUGUST 1, 2021
Volume	: 21
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A Readout Circuit Based on Zero Potential Crosstalk Suppression for a Large Piezoresistive Sensor Array: Case Study Based on a Resistor Model

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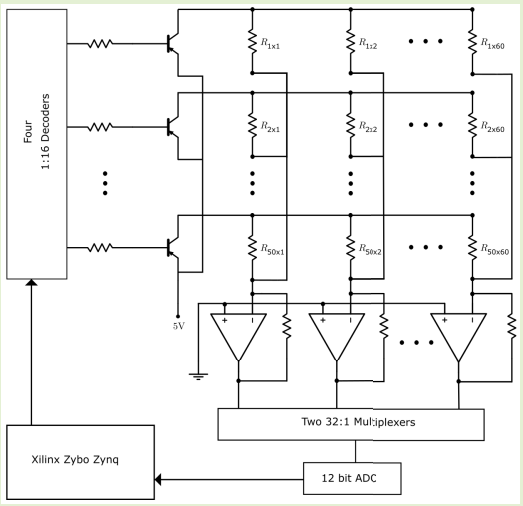
***Abstract*—Although large piezoresistive sensor arrays are vital in obtaining 2D pressure distributions in many applications, they suffer from crosstalk forming parasitic parallel paths as a result of their generic shared row-column architecture. Existing software based algorithms and post processing is the industrially utilized crosstalk suppression mechanism which is below par in meeting the desired measurement accuracy and shape accuracy requirements. However, several hardware based implementations based on the zero potential method have been proposed in literature to mitigate crosstalk and deliver reasonable measurements with repressed crosstalk. Nevertheless, they are often confined to smaller sensor array sizes meeting the requirements of low density applications like robotics where power consumption, design complexity, magnitude of external dimensions, cost of implementation and higher scanning rates are not the governing constraints during the design process. Adopting existing mechanisms directly into scanning large sensor arrays violate the aforementioned design constraints, thus, a novel approach is required. Here, we have proposed and implemented a readout circuit based on zero potential crosstalk suppression, with an improved decoder-transistor based scanning architecture, for a large piezoresistive sensor array containing 30000 sensels meeting the design constraints. The developed circuit was validated using a miniaturized resistor model in conjunction with circuit simulations in PSPICE to determine the propensity of the readout circuit to deliver a measurement accuracy (error less than 1%) while maintaining shape accuracy at the hardware level.**



***Index Terms*—Crosstalk suppression, readout circuit, resistive sensor array, zero potential feedback.**

I. Introduction

TWO dimensional (2D) arrays of force sensors based on piezoresistive principles are often used in static and dynamic load monitoring and damage detection applications in biomedical (minimum invasive surgery, diabetic feet scanning etc.) and robotics [1]–[3] as they offer several technological and economical benefits including low complexity of implementation, durability, robustness and low cost [4], [5].

In order to reduce interconnect complexity/overloading and improve scanning rates of a piezoresistive sensor array with $M \times N$ elements, shared row-column architecture is often adopted [5], [7], [8]. Although, a reduction in interconnections to $M + N$ and higher scanning rates could be achieved by addressing sensels as rows and columns [4]–[7], occurrence of crosstalk due to the formation of parasitic parallel paths is inevitable [1]–[11] resulting in the spread of information between sensels [4], [20]. Hence, sensor arrays expanding a formidable scanning area, with faster signal conditioning which facilitate realtime operation while effectively mitigating

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undesirable crosstalk are the most vital constraints for new generation of piezoresistive sensor arrays.

A. Crosstalk Suppression

Several scanning approaches that mitigate crosstalk have been proposed and implemented using either software modifications after data acquisition or hardware modifications to local electronics. Almost all commercialized piezoresistive sensor array systems utilize software modifications to mitigate crosstalk by employing various proprietary algorithms to compensate for the induced error of measurement [12]–[14]. However, when deploying these algorithms, measurement accuracy (ability to record measurements with minimum errors) and shape accuracy (ability to correctly replicate the shape of the measurand) cannot be obtained simultaneously. In literature, several hardware compensation techniques for crosstalk exist for smaller sensor arrays, of which voltage feedback method (VFM) [4], [9], [10] and zero potential method (ZPM) [15]–[18] are the most widely adopted. The underlying mechanism of crosstalk suppression in both these methods is by momentarily forming a virtual short-circuit around the non-scanned sensels of the array that contribute in parasitic path formation by retaining both ends at an equipotential voltage when scanning a particular sensel [4], [9], [10].

However, both VFMs and ZPMs are susceptible to characteristics of the piezoresistive sensor array and the parameters of the readout circuit such as multiplexer ON resistances, sampling resistances, non-ideal characteristics of operational amplifiers (op-amps), wire resistances and contact resistances of the feedback circuit [4], [9], [10]. Comparatively, ZPMs are associated with high scanning rates, greater linearity between input vs output characteristics, lesser measurement errors with increased sensor array dimensions, high cost and complexity [4], [10], [19]. Thus, ZPMs are preferred for scanning large piezoresistive sensor arrays with many sensels.

B. Local Electronics Used for Array Readout Circuits

Apart from the local electronics of the readout circuit, manufacturing technology and the number of senels present in the shared row-column architecture of the sensor array also governs the scanning approach. Castellanos-Ramoset *et al.* [1] has identified that conductive ink based polymer sheets result in the most efficient, reliable and robust sensor arrays. Nonetheless, almost all the reported cases in literature for conductive polymer sheets with ZPM based scanning approaches have generally been not greater than 16×16 sensels, as they have all been implemented for applications involving robotics. However, as a structural health monitoring tool, for example pedobarographic assessment of diabetic feet, the technology nor the scanning approaches have met the requirement. In fact, most of the commercial pedobarographic tools which are based on piezoresistive principles are either smaller in dimensions. Those which meet the required spatial dimensions are based on capacitive principles with complications in signal conditioning together with subsequent parasitic capacitances having only software compensations for crosstalk [1], [3]. With increasing spatial dimensions (larger sensor arrays), constraints such as high speed signal conditioning, data transmission, faster data processing of huge amounts of data, reduced wiring complexity and lower power consumption must be considered.

When considering the existing scanning approaches, microcontrollers, Programmable System on Chips (PSoC) and Field Programmable Gate Arrays (FPGA) based systems exist for smaller arrays. However, the above constraints pertaining to larger sensor arrays could be addressed with a FPGA based system [1], [3]. Therefore, there exist a requirement to develop a readout circuit and a scanning approach for larger piezoresistive sensor arrays by modifying existing scanning approaches for smaller arrays incorporating hardware compensation for crosstalk that also meet the above design constrains.

TABLE I
SPECIFICATIONS OF THE PIEZORESISTIVE SENSOR ARRAY MANUFACTURED USING CONDUCTIVE POLYMER SHEET FABRICATION TECHNOLOGY TO SERVE AS A STRUCTURAL HEALTH MONITORING TOOL

Characteristic	Value
Number of sensors	30,000
Number of rows $\times$ columns	100×300
Number of clusters	10
Rows $\times$ columns of a cluster	50×60
Sensor area	5×1.5 m^2
Individual sensor size	6.25 mm^2
Pitch	5 mm
Spatial resolution	4 sensels per cm^2
Response time (90% of the output)	< 3 ms
Measurement Range	1 kΩ - 1 MΩ

C. Proposed Implementation

In this paper, we present a readout circuit with a scanning approach based on ZPM (Section II B, C) controlled by a FPGA system for a specific conductive polymer sheet type piezoresisitive sensor array specially developed as a structural health monitoring tool with specifications given in Table I. Here, 30,000 sensels with a total sensing area of $0.5 \times 1.5\ m^2$ are assembled into 10 identical clusters of 50×60 such that 5 identical readout circuits could scan all 10 clusters (one readout circuit scans two clusters) simultaneously through the FPGA achieving parallelism, thus ensuring real time operation.

We verified the proper functionality of the readout circuit using a fixed resistor array model (Section IV A) so that manufacturing defects and mismatching between sensels [1], [3] in the array do not interfere the verification of the readout circuit. Ultimately, we have shown that using the proposed readout circuit, both measurement accuracy (Section IV B)and shape accuracy (Section IV C) could be obtained simultaneously without compromising either as opposed to existing techniques.

II. ARCHITECTURE OF THE READOUT CIRCUIT

A. Existing Architectures

A readout circuit generally consist of driving electrodes (row driver), sampling electrodes (column scanning) and analog to digital conversion unit as main components and other accessories. Based on the mechanism by which non-scanned

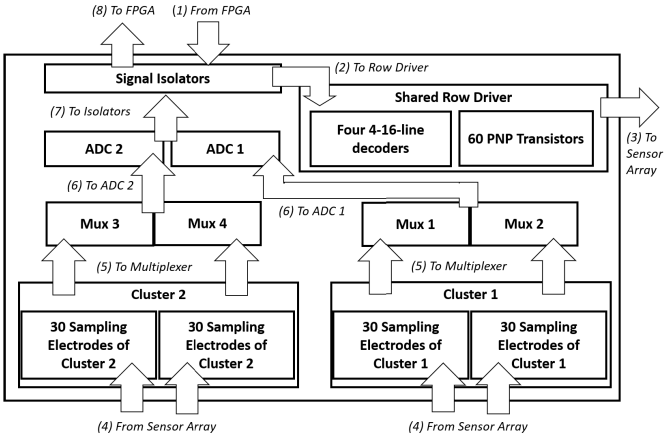

Fig. 1. Proposed architecture of the readout circuit for scanning two clusters of a large piezoresistive sensor array of 30,000 sensors arranged into 10 clusters of 3,000 sensels as 50 × 60. The FPGA board issues controls signals to the shared driving electrodes (shared between 2 clusters) through isolators to activate each row sequentially until all rows are activated and scanned. The sampling electrodes scan each column sequentially also upon receiving FPGA control signals. Two multiplexers are placed to sequentially scan each sampling electrode of a cluster (each multiplexer scan 60 sampling electrodes each). Both Mux 1 and Mux 3 works in tandem while Mux 2 and Mux 4 works in tandem for two clusters to transmit analog data to a dedicated ADC for each cluster which digitise them and transmit to the FPGA board via isolators for further signal conditioning. Please note that only the main components of the readout circuit are illustrated here by excluding filter circuits, buffer circuits and other passive components. Anti-aliasing filter exist between the sampling electrodes and multiplexers. An ADC buffer and a low pass filter has been placed between the multiplexers and ADC. A detailed representation of the signal path is shown in Fig. 3.

electrodes of the readout circuit retained at zero voltage, ZPMs have been sub-categorized by Liu *et al.* [10] as, setting-non-scanned-electrode-zero-potential (S-NSE-ZP) method, setting-non-scanned-sampling-electrode-zero-potential (S-NSSE-ZP) and setting-non-scanned-driving-electrode-zero-potential (S-NSDE-ZP) method. In S-NSE-ZP method, both ends of the non-scanned sensels are virtually grounded by switching respective shared rows and columns. On the other hand, in S-NSSE-ZP and S-NSDE-ZP methods either driving electrodes or else sampling electrodes of the non-scanned sensels are grounded while retaining other set of electrodes at high impedance. Further, Kim *et al*, [15] categorized driving electrodes of ZPMs as digital buffer systems (Type I) and operational amplifier systems (Type II). In Type I systems, multiplexers toggle the rows between power up voltage (Vcc) and feedback voltage. Therefore, these systems demand low multiplexer switch-on resistance to ensure accurate switching and also high current driving capability. This is because, large RSAs draw comparatively high currents, in the case when all the non-scanned elements in the row are at their lowest resistance value, leading to an inherent inaccuracy problem [3], [15]. In contrast, Type II systems are regarded as the most efficient row driving mechanism because the op-amps are connected with a feedback such that they provide accurate electrode voltages, even with non-ideal operation. However, this technique requires $M + N$ op-amps, which increases power consumption, system complexity and cost of implementation for larger RSAs [9], [10], [19].

As a solution, Kim *et al*, [15] has proposed a ZPM scanning technique using only a single op-amp and $2N$ switches and has effectively realized this for a 4×4 sensor array. Although, this novel architecture is commendable for applications involving smaller array sizes, it fails to cater for larger RSAs demanding higher scanning rates and spatial resolution due to the resultant scanning delay associated with higher number of sensels. Besides, higher driving currents and susceptibility to high frequency switching noise and electromagnetic interference [19] when the sensor array is driven by a single op-amp is clearly not feasible for our application.

Since the accuracy of the existing scanning approaches used in readout circuits depends primarily on the offset voltages of the op-amp and the switch-on resistance of the driving electrodes, increased use of op-amps consumes more silicon area and power if directly adopted for larger RSA systems, thus imposing several practical inefficiencies theoretically. In terms of crosstalk suppression, the S-NSE-ZP method is the most suitable method to implement ZPM as it involves $M + N$ dedicated op-amps for each row and column of the sensor array. However, practically, the power consumption and silicon area of the readout circuit increases significantly. The S-NSSE-ZP method on the other hand, reduces op-amp requirement generally from $M + N$ to N by eliminating the need for op-amps at driving electrodes but accommodating a dedicated op-amp forming the sampling electrodes at each column. Incorporating a dedicated op-amp for each column serves a dual functionality such that it provides a virtual ground for all non-scanned columns when it is not addressed and scan the column when addressed by the controller. The output voltage of the sampling electrode op-amp becomes the signal of interest to measure the sensor resistance. Therefore, S-NSSE-ZP would be the most appropriate crosstalk suppression technique to adopt for large array scanning. Nevertheless, placing an Analog to Digital Converter (ADC) at the output of each sampling electrode would generate a fast readout as demonstrated by Liu *et al.* [10], yet, a dedicated ADC for each column in a large sensor array would increase the cost significantly. Hence, we propose to trade off the need to couple an ADC for each sampling electrode by multiplexing each sampling electrode at a higher frequency and feeding into a single ADC with a higher sampling rate.

B. Proposed Driving Electrode Architecture

We propose to implement the scanning architecture for the driving electrodes of the readout circuit using a decoder-transistor system as depicted in Fig. 1 which reduces overall power consumption, cost of components and complexity while generating fast readout rates with minimum crosstalk interference. An active-low decoder would be issued with control signals corresponding to a specific row number to activate, by the FPGA. This will result in switching a row on, through a PNP transistor which acts as a high side switch that toggles rows between active and inactive states upon the active low signal of the decoder (Fig. 2). This, eliminate any switch-ON resistances that may be present directly across the decoder. Although, a switch-ON resistance exist even for a transistor, it is in the range of mΩ which is negligible in

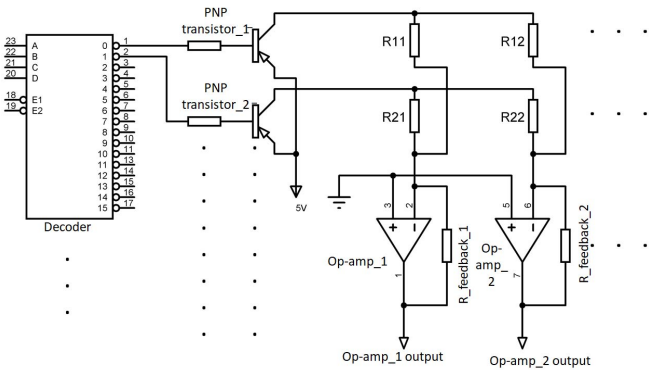

Fig. 2. The layout of the proposed readout circuit decoder-transistor based row-driver and op-amp based sampling electrodes using ZPM suppression technique. One decoder can address 16 distinct rows, hence 4 decoders are sufficient to scan an entire cluster of 50 rows. Since two clusters share the same driving electrodes, in fact, 4 decoders and 50 transistors can address 100 rows with the proposed architecture. Op-amps at sampling electrodes serves 2 distinct purposes. During idling(not scanning) they toggle the non-scanned columns to virtual grounding and act as an inverting amplifier which converts the sensor resistance to a voltage signal when scanning. It is important to note that the sensel being scanned is a part of the op-amp's feedback loop.

comparison to the switch-ON resistance through a decoder. Since the proposed driving electrodes does not switch directly through digital buffers (multiplexers, decoders etc.) or op-amps, inaccuracies discussed by Liu et al [10] will not be associated with measurements, while inadvertently reducing the power consumption and high switching noise.

When a driving electrode needs to be scanned, an active low signal is provided at the base of the corresponding transistor forceing it to the saturation mode. This connects the driving electrode to the power up voltage enabling a flow of current through the desired sensel which can be read through the inverting op-amp based sampling electrode in unity gain configuration as shown in Fig. 2.

Meanwhile, the remaining I/O pins of the decoder which are connected to corresponding transistors receive a high voltage signal. This drives the PNP transistors to the cutoff mode which forces the driving electrode into a high impedance floating state. This technique, ensures that the rows are maintained at power up voltages when scanned but falls onto a high impedance state when they are not scanned, thus, establishing the S-NSSE-ZP condition while maintaining a low susceptibility to noise [9], [10], [19].

Besides, one decoder we have used can address 16 independent rows, requiring only 4 decoders to address all the rows (50) in a cluster, saving both silicon area and power requirement. Moreover, as one readout circuit of our application scan two columns in tandem as shown in Fig. 1, we have optimized it in such a way to have shared driving electrodes for two clusters and separate sampling electrodes for each cluster, again reducing cost and complexity of implementation, silicon area of readout circuit and the power requirement.

C. Proposed Sampling Electrode Architecture

All the sampling electrode op-amps are scanned sequentially via two 32:1 multiplexers which can accommodate all columns (60) in a single cluster. The local electronics we propose to implement in the readout circuit along the pathway from each sampling electrode to an I/O port of the FPGA is illustrated in Fig. 3.

D. High Frequency Noise Filtration

Upon, scanning the array, signal conditioning should be performed to ensure the accuracy of the obtained data for further processing. To remove noise generated due to high frequency switching between sampling electrodes, a low pass anti-aliasing filter was added at the multiplexer output. But this induced transients at the multiplexer output increasing its settling time. Therefore, placing the filter at the multiplexer output is undesirable for large sensor array readout due to the resultant measurement errors arising of limited settling time. Otherwise, the scanning frequency of sampling electrodes must be compromised.

Alternatively, a low pass anti-aliasing low pass filter implemented to band limit the signal before the input of the multiplexer based on proper component selection, discussed in section III, proved to deliver the desired filtration. The low pass anti-aliasing filter could be further optimised by incorporating it directly into the feedback loop of the op-amp of the sampling electrode of the op-amp. However, it is important to note that the sensel resistance(R_EBT) is a part of the op-amp's feedback loop, while the feedback resistor $R\_feedback$ should always be configured to the lowest sensel resistance, which vary based on the measurement range of the piezoresistive sensor array. In the context of our application, the lowest sensel resistance was configured to be of 1kΩ thus, requiring a larger capacitance for the filter capacitor if coupled directly to the feedback loop.

E. Analog to Digital Conversion

In order to avoid the ADC from unnecessary loading, an ADC buffer was implemented at the ADC input as recommended by the manufacturer. Moreover, adding a low pass filter (ADC input filter Fig. 3) in between the ADC input and the ADC buffer seemed to further reduce noise and high frequency components due to switching by further smoothing the ADC input signal. Employing the Successive Approximation Register (SAR) technique, the ADC digitized the input signal and transverse it to the I/O ports of the FPGA board.

III. Design of the Readout Circuit

A. Decoder-Transistor Driving Electrode System

Component selection plays a major role in realizing the proposed readout circuit architecture. In order to implement the proposed driving electrodes in Section II B, we opted to use a 4-to-16 line, active low decoder 74HC154 which decode four binary weighted address (which translate to a specific row number) from the FPGA board to sixteen mutually exclusive outputs to drive the transistors with a maximum current drive of 20 mA.

High current driving (upto 2A) PNP transistors (NSS40200LT1G) that are also capable of accepting 20 mA as base current from the decoder with low saturation voltages (on resistance in mΩ range), was selected as high

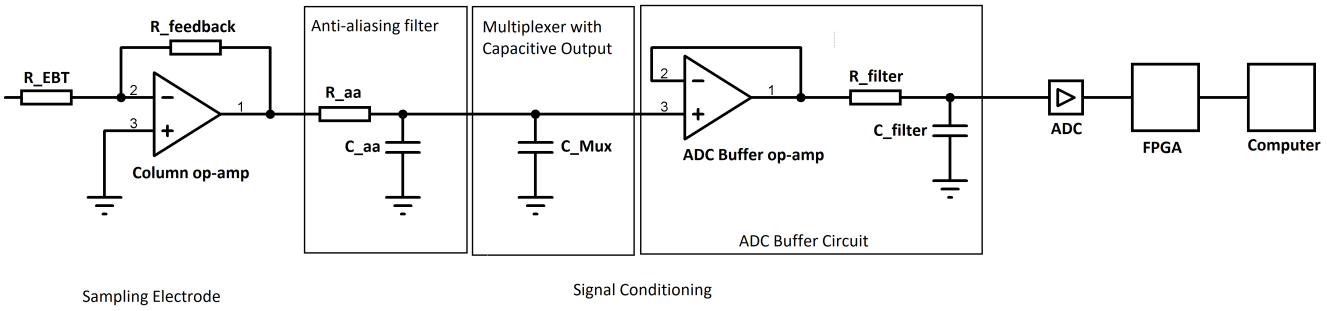

Fig. 3. Representation of the signal pathway of the sensor readout circuit. The voltage drop corresponding to the equivalent resistance across *R_EBT* (EBT = Element Being Tested) at any given time is measured across the feedback resistor (*R_feedback*) of the sampling electrode (op-amp) which will be filtered through an anti-aliasing filter and fed to a multiplexer with a capacitive output terminal. The multiplexed signal transverse through an ADC buffer circuit containing a voltage buffer and a low pass filter before reaching the ADC. Readings from the ADC is acquired using an FPGA and sent to a computer for further processing.

side switches that toggle the 5 V supply voltage connected to the emitter terminal and drive the transistor to saturation or cut-off.

B. Sampling Electrode System

The sampling electrode op-amp is the most critical unit in implementing the zero potential condition. This is because the inverting configuration of the op-amp ensures that, theoretically, all columns are virtually grounded while the non-inverting terminal is grounded. Therefore, a very low input offset voltages (maximum of 1.5 mV in the selected op-amp) ensured the best functionality of the proposed readout circuit. Besides, the op-amp should be unity gain stable to ensure oscillation free operation and possess a higher Gain Bandwidth Product (GBW), higher the slew rate, higher current sinking and sourcing ability and must provide a rail-to-rail output to ensure error free, smooth operation. Furthermore, higher slew rates can mitigate the effect of parasitic capacitances present in the piezoresisitve sensor array as these can worsen the time delay for stabilization even further. Accordingly, upon a careful investigation, we selected OPA2810 to serve this purpose.

As discussed in Section II D, the lowest measurable resistance of a sensel (*R_EBT* in Fig. 3) was 1 kΩ during the manufacturing process. After a series of pilot studies using several resistors with varying magnitude, it was apparent that 1 kΩ (part number: MCT06030C1001FP500) was the most suitable as the feedback resistor (*R_feedback*) for the application.

C. Multiplexer

Monolithic, ADG732 CMOS analog multiplexer with an on resistance of 4 Ω which switches one of its 32 inputs to a common output determined by 5 binary weighted address was selected for our application. Two such multiplexers are capable of addressing all 60 sampling electrodes of a cluster as depicted in Fig. 1. In addition, rail-to-rail operation with settling times in nanosecond range (23 ns) justifies the selection of this multiplexer further.

Consequently, to attain a sampling rate of 1 MSPS from the ADC, a low pass anti-aliasing filter with a cut off frequency of 500 kHz was required at the multiplexer output. However, our design proposes to incorporate anti-aliasing filters at the input stage of the multiplexer for each sampling electrode due to design constraints described in Section II C.

D. Anti-Aliasing Filter

Each of the two multiplexers belonging to a single cluster, addresses 30 of the 60 sampling electrodes. As we implemented the anti-aliasing filter at the input stage of the multiplexer rather than the output stage, the frequency of the implemented multiplexer input stage anti-aliasing filer should be 30 times less than that of a multiplexer output stage anti-aliasing filter which amounted to 16.67 kHz (500 kHz ÷ 30). Nevertheless, the targeted scanning frequency for the sensor array is 300 Hz (Section III), which is the maximum frequency of the voltage signal variation that is attainable from it, which is less than the cut off frequency of the anti-aliasing filter required. Therefore, band limiting of the signal and elimination of the risk of aliasing are both achieved if we are to adopt a low pass filter with a cutoff frequency of 300 Hz at the input of the multiplexer instead of 16.67 kHz. However, in order to obtain a cutoff frequency as low as 300 Hz using a passive RC filter, large capacitance and resistances are needed. Besides, as the filter is placed in between the op-amp output and multiplexer input, the resistor of the filter also act as a damping resistor for the op-amp output. Meanwhile, the filter capacitor adds to the capacitive load seen by the opamp. Therefore, having a large resistor facilitate the reduction of the required capacitance, yet, incorporating large resistors result in increased thermal noise. Considering all these constraints and trade-offs, it was decided to use a resistor (*R_aa*) of 820 Ω and capacitor (*C_aa*) of 1 μF for the anti-aliasing filter and attain a cutoff frequency of 194 Hz, which proved to be adequate for our application.

E. Analog to Digital Converter

Vidal-Verdú *et al.* [3] concludes that for slippage detection, which is the highest dynamic requirement expected of a piezoresisitive sensor array, it must be scanned with a frequency of at least 250 Hz. As our piezoresisitive sensor array response time was found to be 3 ms, the maximum scanning frequency we could target was 300 Hz. Based on that, we deduced that, in order to implement the proposed architecture, the ADC must sample at 1 MSPS.

According to the measurement range of the piezoresistive sensor array, it was evident that 12 bit resolution is adequate for encoding analog readings to digital at a sampling rate of 1 MSPS with minimum latency. Hence, ADS7883 which met the desired specifications was selected as the ADC for one cluster. Based on the recommendations in the manufacturer data sheet, a buffer was placed at the input stage of the ADC using a OPA365 to prevent the ADC from loading unnecessarily.

F. Power Supply

Proper component selection for signal acquisition and conditioning should be complemented with proper power supply. Almost all ICs, especially op-apms, require well bypassed power supply for optimum operation. Therefore, low ESR bypass capacitors were placed close to the power supply pins of the ICs without placing vias in between to act as charge banks. This is because, ICs tend to draw surge currents from the power supplies in which case the copper traces from the power supplies to the IC act as inductors and cause a drop in the supply voltage. This could result in oscillations in the power supply inducing oscillations in the IC operation too.

To establish ZPM a dual rail power supply is necessary. Commercial dual rail supplies based on Switch Mode Power Supplies (SMPS) generate switching noise inducing power line noise to the circuit. To avoid this, we used a combination of SMPS, Linear Low Dropout Regulators (LDOs) and power line filters to supply power to the readout circuit as shown in Fig. 4.

G. FPGA Controller

As the main controller of the system we have used a Xilinx Zynq (ZYBO) development platform built around the Xilinx Zynq-7000 family which integrates a dual-core ARM Cortex-A9 processor with Xilinx 7-series FPGA logic. It features 6 distinct I/O ports and operates at 3.3V logic. As a precautionary measure to prevent any voltage fluctuations and transients damaging the FPGA board, signals to and from the readout circuit (ADC readings, control signals for decoders and multiplexers) with capacitive signal isolators SI8660BA-B-IS1 (one-way isolator) and SI8662BB-B-IS1 (two-way isolator) as shown in Fig. 3.

IV. Design Validation of the Readout Circuit

Using the local electronics depicted in Fig. 3 and scanning approach depicted in Fig. 2, we implemented a readout circuit as shown in Fig. 5 that can scan two 50 × 60 clusters simultaneously ensuring resource sharing thus reducing the area of the readout circuit. Here, both clusters have a common set of driving electrodes (50) that power up 50 rows of the sensor array and a separate set of sampling electrodes and related signal conditioning electronics.

In literature, validation techniques of readout circuits are threefold; (i) testing with the actual sensor array, (ii) using circuit simulations [2] or (iii) analysis with a mathematical test model [6], [18]. Although, method (i) seems to be the most straightforward readout circuit validation method, non-idealities present in the actual sensor array (due to manufacturing defects such as mismatching between sensels)

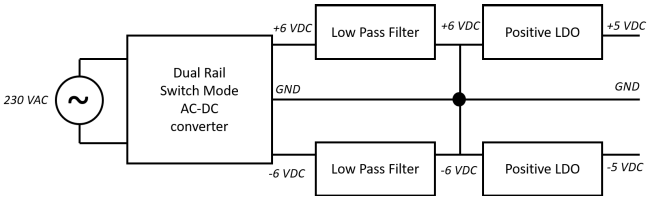

Fig. 4. Proposed power supply for the readout circuit using a combination of SMPS, LDOs and power line filters.

[1], [3] will not reflect the true performance of the readout circuit can not be evaluated. Therefore, we used the methods (ii) and (iii) to validate the realized readout circuit.

To perform a circuit simulation, we developed a miniaturized resistor array model as shown in Fig. 9 to verify the functionality of the realised readout circuit while providing a better approximation to the piezoresistive sensor array. It consists of 64 slots arranged into an 8×8 array onto which fixed resistors of arbitrary values could be inserted to simulate various loading conditions in the actual sensor array.

A similar approach has been undertaken by Saxena *et al.* where a miniaturized hardware model of 4×4 has been utilized to validate a 16×16 light dependent resistor sensor array [20]. Further, Saxena *et al.* has demonstrated that in a networked resistor array of identical sensors (having same resistance and uniform response to the same excitation), the current supplied for sensor reading is distributed evenly in four distinctive zones and each zone experiences a uniform parasitic current due to circuit symmetry [6]. Moreover, the parasitic currents experienced by elements without a direct connection to the currently scanned resistor (commonly referred as Element Being Tested (EBT)) decreases with the increase of the number of rows and columns in the array due to the attenuation of parasitic currents. In our application, we can assume that the EBT reading arises from the adjacent and nearest sensor elements based on Saxena *et al.* [6] given the facts; the actual pressure sensor array has been manufactured with identical piezoresistive sensors and the majority of the sensors are not directly connected to the EBT. Thus, a miniaturized 8×8 array is justified to be a better and a feasible solution for the present design validation.

As this resistor model allows accessing individual sensels of the array and all the adjacent sensels of the array which could be changed as desired, the effect of crosstalk suppression depending on the surrounding non-scanned sensels could be efficiently modeled and the performance of the readout circuit can be evaluated. For the purpose of the experimentation we selected resistors with a tolerance of $\pm 1\%$ within the range 1 kΩ to 10 kΩ which was identified to be the desired measurement range for pedobarographic assessment. However, the proposed resistor model could be adopted for any array size irrespective of the resistor range. Note that in this case the feedback resistor of the sampling electrode (*R_feedback* in Fig. 3) needs to be reconfigured. Moreover, the resolution of the accuracy of the readings beyond 10 kΩ were observed to reduce exponentially. Meanwhile measurements less than 1 kΩ drives the corresponding sampling op-amp to saturation. However, via a careful component selection process, desired measurement range can be configured.

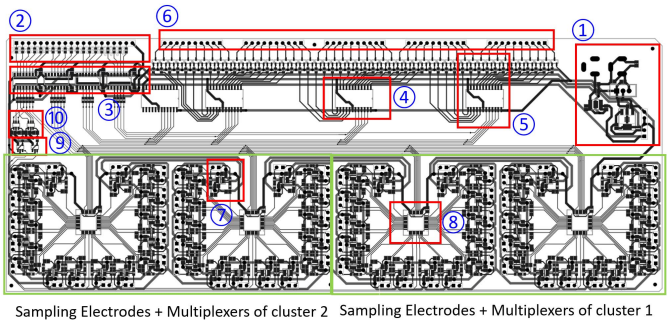

Fig. 5. The implemented readout circuit for scanning two 50 × 60 clusters simultaneously with 50 shared driving electrodes to drive rows and 60 × 2 sampling electrodes (for scanning each column). Note that each cluster requires two 32:1 multiplexers (control 60 input channels). The main components of the implemented readout circuit are: (1) Power supply and regulation to the readout circuit comprising of Linear Low Dropout Regulators and power line filters. (Refer Section III–D,(2) Header connections for interfacing controls signals from ZYNQ device to readout circuit, (3) Capacitive signal isolators SI8660BA-B-IS1 one-way isolator and SI8662BB-B-IS1 two-way isolator (Refer Section III–G), (4) active low decoder 74HC154 (Refer Section III–A), (5) decoder transistor driving electrode system based on 50 PNP transistors NSS40200LT1G (Refer 2 and Section III–A) (6) 50 headers for driving 50 rows. It is shared between two clusters. (7) Sampling electrode system consisting of 1 kΩ MCT06030C1001FP500 resistors and OPA2810 operational amplifiers. (Refer Section III–B), (8) ADG732 CMOS analog 32:1 multiplexer. 4 such multiplexers are available for 2 clusters. (Refer Section III–C), (9) OPA365 ADC buffers. Two buffers are available for the two ADCs. (Refer Section III–E), (10) ADS7883 ADCs for converting multiplexed readings from each cluster. (Refer Section III–E.

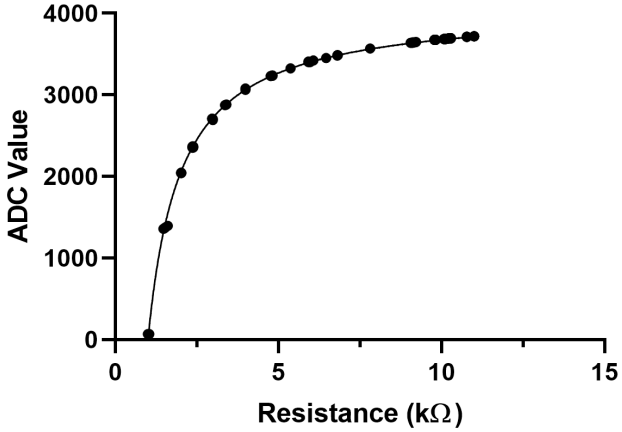

Fig. 6. The response (ADC reading) of the readout circuit for resistor range from 1 kΩ - 12 kΩ when crosstalk is absent (shown in dots). The obtained non-linear regression model (with a coefficient of determination of 0.99) for the data points is shown by the curve. It is evident that the data points are consistent with the estimated results from Equation (1). This curve also indicate the expected ADC value for any corresponding resistance value within the stated region and it is also useful for calibration of the piezoresistive sensor array.

As discussed in Section I B, the expected functionality of the designed readout circuit is to provide an improvement to measurement accuracy and shape accuracy simultaneously with minimum compromise when scanning a large sensor array. Hence, we developed two experiments which are explained in Section IV B, C using the miniaturized resistor model to verify these. Once the efficacy of the readout circuit was established using the resistor model, it will be a matter of scaling up the design to suit the increased number of rows and columns in the actual sensor array.

A. Readout Circuit Transfer Function

To map the actual resistance and the ADC reading in the readout circuit, we generated its transfer function of the readout circuit. This was done with a setup where crosstalk is not present in the resistor array. Since, crosstalk is a phenomena which occurs due to formation of parasitic parallel paths in the shared rows-column architecture, presence of a single resistor without any surrounding non scanned resistors in the array reflects a crosstalk free instance. We measured the actual resistance from a millimeter for a given resistor. Then the same resistor was mounted at row 1, column 1 location of the resistor array model and ADC reading from the FPGA was recorded.

Ten readings were taken from different resistors with the same nominal value to avoid any component bias. By repeating the same procedure, readings were taken for a resistor range from 1 kΩ - 12 kΩ. A non-linear regression model estimated the transfer function given in Equation (1) with a coefficient of determination of 0.99. The fitted curve and data points showing ADC value against the input resistance is shown in Fig. 6.

$$\text{ADC Value} = 4082.6906 - \frac{4071.3265}{\text{Resistor Value}} \quad (1)$$

B. Experiment 1: Measurement Accuracy

The measurement accuracy of the readout circuit, essentially reflects the degree of suppression of crosstalk. Mapping the readout circuit designed for the actual sensor array, 8 rows of the resistor model was connected to the first 8 driving electrodes of the readout circuit (maps to 50 rows in a cluster of the actual sensor array) and the 8 columns of the resistor model was connected to the first 8 sampling electrodes of the readout circuit (maps to 60 rows in a cluster of the actual sensor array). Then, we recorded the value of a resistor (the EBT), fixed at row 1 and column 1 while changing the surrounding non-scanned resistors increasing the array size. First, an EBT of nominal resistance 1.5 kΩ reaffirmed using a millimeter was fixed and recorded the reading from a serial terminal in the computer via the FPGA board functioning as the controller. Then, repeated readings were obtained by surrounding it with non-scanned resistors of same magnitude forming an array size of 2 × 2. Then, the array size was increased to 3 × 3 up to 8 × 8 while obtaining readings. Thereafter, the same procedure was repeated for the same 1.5 kΩ EBT, but with non-scanned resistors of 2.4 kΩ kΩ, 3 kΩ, 6 kΩ and 9.1 kΩ. Similarly, the same process was followed for EBTs of 2.4 kΩ kΩ, 3 kΩ, 6 kΩ and 9.1 kΩ deriving the relationship between EBT with surrounding non-scanned resistors and array size.

To obtain the expected measurements without any non-idealities, we developed a mathematical model for the resistor model taking a similar approach as in [15], [16], [18]. Expected resistance was calculated by a PSPICE circuit simulation derived from the developed mathematical model taking into account ±1% resistor tolerance and calculated the expected measurements for each recorded measurement

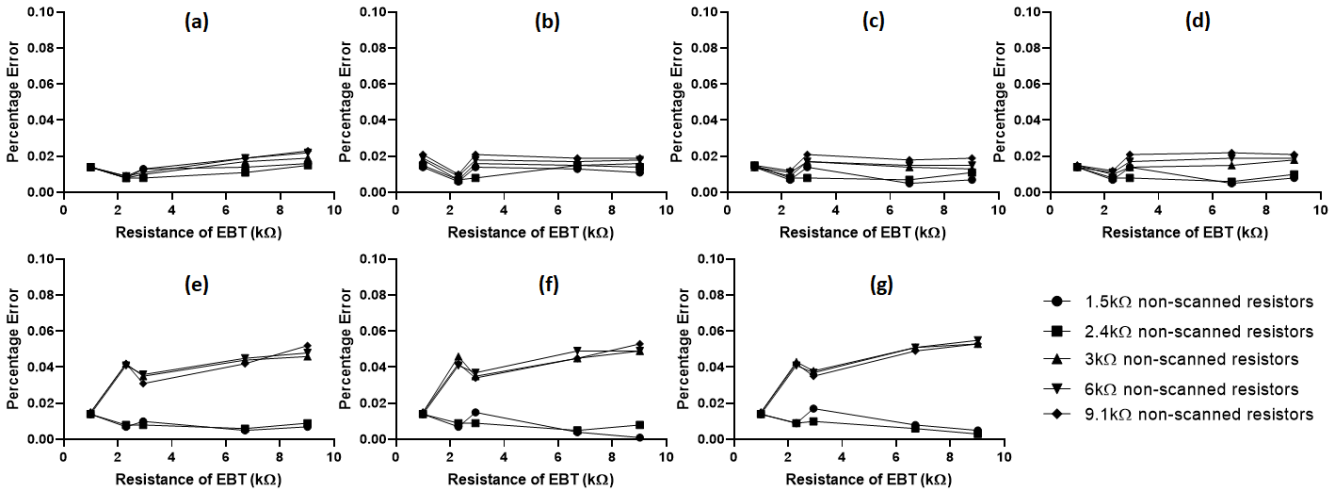

Fig. 7. Percentage variation of error for the miniaturized RSA model when EBTs are varying from 1.5 kΩ to 9.1 kΩ for non-scanned resistors also in the range from 1.5 kΩ to 9.1 kΩ for a fixed array size of **(a)** 2 × 2 **(b)** 3 × 3 **(c)** 4 × 4 **(d)** 5 × 5 **(e)** 6 × 6 **(f)** 7 × 7 **(g)** 8 × 8.

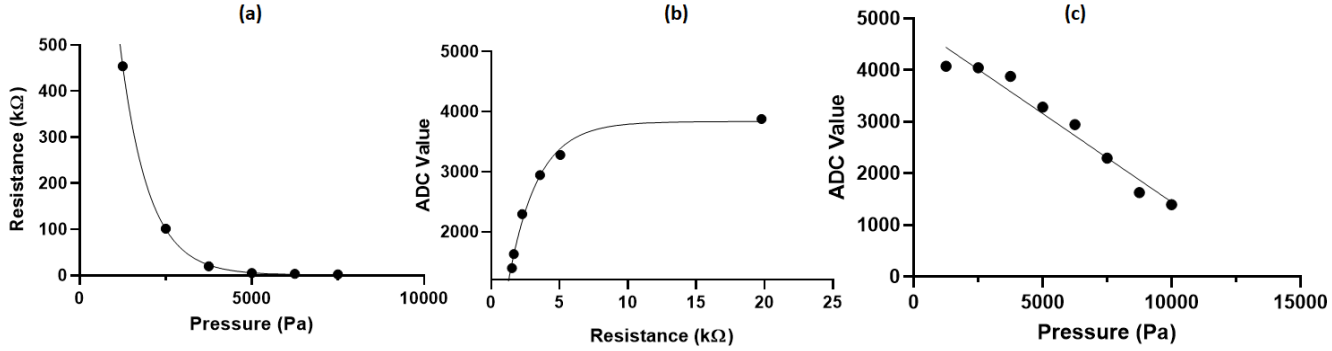

Fig. 8. (a) The non-linear relationship between the system input (Pressure) and sensor response (Resistance) for the range of interest (b) The non-linear relationship between the readout circuit input (Resistance) and its output response (ADC value) also for the range of interest (c) The linearity correction provided by the two non-linear relationships two the system input and the system output from the proposed readout technology.

from the readout circuit and FPGA assembly. Intuitively, the difference between the mathematically calculated measurement (expected measurement) and the averaged readout circuit measurement (measured resistance) reflects the measurement accuracy of the proposed readout circuit. Hence, we quantified this parameter into a percentage error using the Equation (2).

$$\text{error}(\%) = \left[\frac{\text{Expected Resistance}(\text{k}\Omega) - \text{Measured Resistance}(\text{k}\Omega)}{\text{Expected Resistance}(\text{k}\Omega)}\right] \times 100\% \quad (2)$$

The results of this measurement is in Fig. 7 illustrating the deviation of each averaged readout circuit measurement for a given resistor value in the desired measurement range from 1 kΩ to 10 kΩ, when the adjacent non scanned resistance varied within same range while the array size increased from 2 × 2 to 8 × 8. It is evident that the percentage error between the mathematical model and the readings from the readout circuit remains well below 0.1% (reflecting 10 Ω) irrespective of the array size, EBT value or the non-scanned resistor value. Therefore, the readout circuit has been able to effectively mitigate parasitic resistances and suppress crosstalk to achieve an impressive measurement accuracy as indicated by the measurement results. Besides, sufficient isolation of the EBT from the non-scanned resistors of the resistor array has also been achieved.

A gradual increase in the measurement error was observed with the increase of the array size, especially 6 × 6 onward indicating a slight deviation. Nevertheless, it is important to note that this variation was apparent only when evaluating readings up to 4 decimal places with respect to Equation (1). Subsequent extrapolating of the PSPICE simulations for the proposed circuit model showed that the measurement error is well within 1% for an array size up to 50 × 60. In terms of the end application of the resistive sensor array, measurement errors below 2% has a negligible impact on the measurement.

The proposed solution provides a significant improvement to the measurement accuracy compared to most of the existing systems which undergo errors 10% [20], 20% [20], and 30.7% [15]. Besides, the measurement error attained by our readout circuit has also been in par with the readout circuit realized by Kim *et al.*, [15] with an array size of 4 × 4. While providing a further improvement to the scanning mechanism and fine tuning for large sensor array scanning, our readout circuit has also been able to record measurement errors not greater than 0.1%.

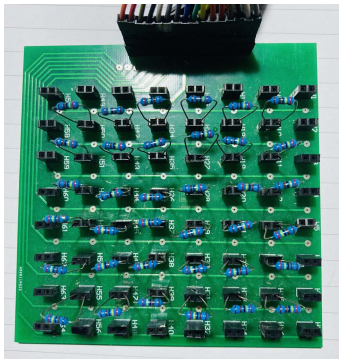

Fig. 9. The designed 8 × 8 miniaturized sensor array model to which resistors could be mounted to simulate, model and validate the functionality of the developed readout circuit.

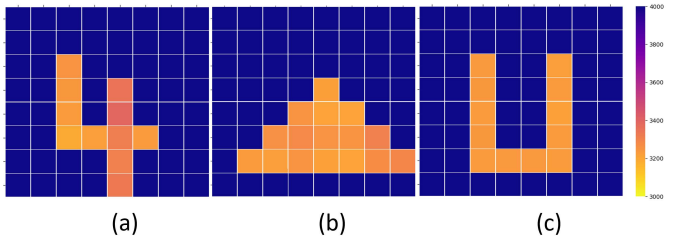

Fig. 10. Shapes replicated on the resistor array model using resistors of 6 kΩ to visualize the degree of shape accuracy attainable from the readout circuit in terms of a (a) number (b) shape and (c) a alphabetical letter.

C. Experiment 2: Shape Accuracy

Upon successful validation of the measurement accuracy, we further evaluated the shape accuracy of the readout circuit to corroborate the effectiveness of the readout circuit and the FPGA board assembly. By populating resistors of varying magnitudes forming numerous shapes on the resistor model circuit, their corresponding readout circuit measurements were obtained via UART interface of the FPGA board with a baud rate of 115200 bits/second and by manipulating the serial stream from the FPGA, we visualized the response of the system using a custom designed Python based program. Thus, a number (4), a basic shape (triangle) and a letter (U) was arbitrarily visualized successfully without any crosstalk as shown in Fig. 10. In addition a compound shape, representing all the resistors used in the Experiment 1, was visualized using resistors range from 1.5 kΩ to 10 kΩ to qualitatively and quantitatively evaluate the measurement and shape accuracy simultaneously. This is shown in Fig. 11 and it is clear that there exist a notable distinction among all resistor value ranges including the open circuit reading.

D. Linear Correction to the System Input

Although, Fig. 6 may imply a gradual decrease in sensitivity of the readout circuit, it was modelled intentionally to provide a linearity correction to the piezoresistive sensor array input. Conductive polymer sheet fabrication technology which manipulate a conductive ink to sense pressure variations have an inherent non-linear relationship between pressure and resistance [1], [3]. Meanwhile, as emphasised by the Equation (1), the readout circuit output, i.e. ADC reading, also

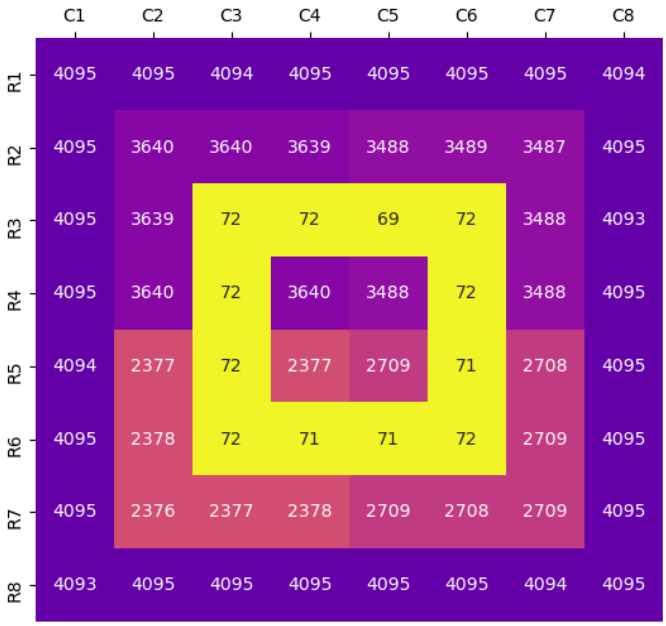

Fig. 11. Visualisation of the compound resistor array model using resistors in the range of 1.5 kΩ - 9.1 kΩ generated via a python program. Dark blue outer perimeter (ADC values 4093-4095) represents the open circuit condition and the inner yellow perimeter (ADC values 69-72) represents 1.5 kΩ, Similarly ADC values 2376-2378, 2708-2709, 3487-3489 and 3639-3640 represents 2.4 kΩ, 3 kΩ, 6 kΩ and 9.1 kΩ respectively.

has a non-linear relationship with the input resistance. Hence, we devised a simple experiment followed by a regression analysis to determine the relationship between the system input (Pressure) and system output (ADC value). We measured the resultant resistances while loading the piezoresistive sensor array with known pressure values (Fig. 8(a)). Then these recorded resistance values were simulated on the resistor array model we developed, with the same resistors used for Experiment 1 and 2, and their corresponding ADC readings were recorded (Fig. 8(b)). The regression analysis conducted subsequently for the recorded ADC values against the corresponding pressure values from loading, indicated a negative linear relationship with a coefficient of determination of −0.95 (Fig. 8(c)), thus proving that the system input and output are almost linear.

V. Conclusion

Although conductive polymer sheet piezoresistive sensor arrays are on high demand, the existing software based readout mechanisms are error prone, delivering either inaccurate measurements or erroneous shapes. As the existing hardware compensations for the inherent crosstalk suppression are adequate for smaller sensor array operations, scaling them up is greatly inefficient due to power considerations, design complexities, wiring complexities, lower scanning rates and cost of implementation. As a result, we implemented a readout circuit that could scan two 50 × 60 clusters with optimizations to the driving electrodes with a novel implementation using a decoder-transistor unit. The overall cost of implementation of the readout circuit was approximately USD 545.00. However, this readout circuit needs to be tested for higher scanning rates. The excellent match between the results yielded using a

miniature resistor model alongside circuit simulations, implies that the proposed readout circuit can achieve both measurement accuracy and shape accuracy simultaneously. Sufficient isolation of the EBT from the non-scanned sensels as indicated by efficient crosstalk suppression (via high measurement accuracy) further strengthens the argument of scaling up the number of rows and columns to fit the desired application.

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